About College

Geethanjali College of Engineering and Technology (GCET) was established in the year 2005 with the sole objective of providing quality technical education affordable to youth of our nation. The college has excellent infrastructural facilities and modern laboratories. GCET is recognized as an R&D centre by Scientific and Industrial Research Organization (SIRO). The college was conferred **"Autonomous"** status by UGC with effect from Academic Year 2016-17 for a period of six years. The college was accredited by NAAC with Grade "A" in May 2017. It also received ISO 9000:2008 certification.

About ECE Department

The Department of Electronics and Communication Engineering (ECE) was started in the year 2005 and is continuously striving to impart quality education and promoting competitive spirit among students for academic excellence. The department has experienced faculty and well equipped laboratories. The B.Tech program in ECE was accredited by NBA in 2012 and 2015.

The Department was sanctioned a DST project entitled "Design and Development of Multi wavelength Laser Radar" (LIDAR) with an overall budget of Rs.34.58 Lakhs in the AY 2010-11, which was successfully completed in AY 2014-15. One more project entitled "Investigation of Linear Combinations of GNSS Measurements to Mitigate the Effect of Ionosphere and Multipath" was also sanctioned by DST with a grant of Rs. 21.5 Lakhs and is in progress. A Consultancy project entitled "Development of High Density Electron Emitter for use in Defense" is in progress for M/s VEM Technologies from November 2016. The department was sanctioned by DRDO a major research project entitled "Development of novel carbon nano tube/polymer nano composite materials for EMI applications" in April 2018 with an overall budget of Rs.45.81 Lakhs.

Joint Chapter of CAS/EDS Societies, IEEE Hyderabad Section

IEEE Hyderabad Section was established in 1980 and has been a very active section in Asia Pacific region. It was awarded the large section award in year 2015. There are 10 Technical Societies, 2 affinity groups and one Technology management council in the Hyderabad section. The Joint Chapter of IEEE Circuits and Systems/ Electron Device Societies was established in 2011 by a team of dedicated volunteers from Industry and Academia. IEEE CAS/EDS Hyderabad has successfully hosted PrimeAsia 2012, PrimeAsia 2013 and PrimeAsia 2015. The Chapter has established good rapport with IEEE CAS Japan, Singapore, Malaysia, Indonesia and Sri Lanka over the last three years utilizing the CASS Networking initiative and has conducted workshops and conferences in collaboration with these countries. The CAS chapter is motivated to place Hyderabad section on the map of Circuits world by organizing distinguished conferences like APCCAS, ISCAS and others.

Aim of the Program

Chip Design in India has grown by leaps and bounds, thanks to the presence of several multinationals, design services companies and product companies. It translates to a plethora of opportunities for quality VLSI-trained talent. This FDP is intended for young faculty members working in engineering colleges and research scholars to make them familiar with latest trends in VLSI Design/Technology and to enrich them with depth and breadth of knowledge. In VLSI design, the methodology makes extensive use of CAD techniques for all the tasks that span design through layout to finally "sign-off the design database" for chip fabrication.

In addition to theoretical knowledge, the aim of this FDP is to equip the participants with hands-on experience in the state-of-art Cadence EDA tools for VLSI Design supporting Analog and Digital Front End and Back End.

Topics to be Covered

- Overview of VLSI Design Flow, Tools and Methodology; System Architecture Design.
- Latest trends in ASIC Design, Design for Verification, DFT, Constraint driven Synthesis, STA
- Physical Design, Timing Driven P&R, Physical Verification, DFM etc.
- Challenges involved in design of Digital/Analog/Mixed Signal circuits for IP and System on Chip (SoC).
- Analog Design Modeling using Verilog-A and Simulation; Analog IC Design using Cadence Virtuoso; Lab Sessions on Verilog-AMS.
- Emerging Applications of VLSI in IoT, Artificial Intelligence, DSP, Wireless Communications etc.
- Opportunities for Research in VLSI Design.

Resource Persons

Experts from industry and prestigious academic institutions namely RCI, ANURAG (DRDO), AMD, Redpine Signals, AMS, NIT Warangal and SNIST.

Industrial Visit

A visit to **GAETEC**, a Chip Fabrication Unit, is scheduled for the participants during FDP.

Eligibility

Faculty with ECE, EEE and EIE background and Research Scholars in this domain.

Schedule

Registration to be completed on or before: June 14, 2018
Intimation of final list of participants: June 16, 2018
Program Dates: June 18-23, 2018
Timings: 9:30AM to 4:00PM
Venue**:** Seminar Hall, Block 1

Check the web page for more details of FDP at: http://vlsifdp.gcet.edu.in

One Week
Faculty Development Program
On
"Latest Trends in VLSI Design and hands-on Implementation using Cadence EDA tools"

June 18-23, 2018

Registration Form

Registration Fee:
For Faculty Members/Research Scholars: Rs. 1000/-
For IEEE Members Rs. 800/-

Google Form for Online Payment and Registration is at https://goo.gl/forms/hXN3WBaTjrWxzVoB2
Note: Send payment receipt to Coordinator's email

Name: ……...
Designation: …….
Organization: ……..
Professional Experience:
Mobile:…….....
E-mail:…….

Declaration

The information furnished above is true to the best of my knowledge. I agree to abide by the rules and regulations governing the FDP.

Place:
Date: Signature of the Applicant

SPONSORSHIP

Mr./Mrs./Dr…….. is an employee of our institution and is hereby sponsored for attending the above FDP.

Place:
Date: Signature of the Principal

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Organized
By
Department
of
Electronics and Communication Engineering

In technical collaboration with IEEE CAS/EDS Chapter, Hyderabad Section

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