ECA

COURSE FILE

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GEETHANJALICOLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF *Electronics and Communication Engineering*

(Name of the Subject) : Electronic Circuit Analysis **Course file**

(JNTU CODE –A40412) **Programme : *UG***

Branch: ECE

Year: II ECE – A/B/C/D ***II*Document No. GCET/ECE/----/-----**

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2) Sign :

3) Date :

2. Syllabus:

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

II Year B.Tech. ECE-II Sem	**L**	**T/P/D**	**C**
	4	**-/-/-**	**4**

(A40412) ELECTRONIC CIRCUIT ANALYSIS

Course Objective:

- To familiarize the student with the analysis and design of basic transistor amplifier circuits and their frequency response characteristics, feedback amplifiers, oscillators, large signal amplifiers and tuned amplifiers

UNIT -I:

Single Stage and Multi Stage Amplifiers

Single Stage Amplifiers: Classification of Amplifiers – Distortion in Amplifiers, Analysis of CE, CC, and CB Configurations with simplified Hybrid Model, Analysis of CE amplifier with Emitter Resistance and Emitter follower, Miller's Theorem and its dual, Design of Single Stage RC Coupled Amplifier using BJT.

Multi Stage Amplifiers: Analysis of Cascaded RC Coupled BJT amplifiers, Cascode Amplifier, Darlington Pair, Different Coupling Schemes used in Amplifiers - RC Coupled Amplifier, Transformer Coupled Amplifier, Direct Coupled Amplifier.

UNIT –II:

BJT Amplifiers and MOS Amplifiers

BJT Amplifiers - Frequency Response: Logarithms, Decibels, General frequency considerations, Frequency response of BJT Amplifier, Analysis at Low and High frequencies, Effect of coupling and bypass Capacitors, The Hybrid- pi (p) - Common Emitter Transistor Model, CE Short Circuit Current Gain, Current Gain with Resistive Load, Single Stage CE Transistor Amplifier Response, Gain-Bandwidth Product, Emitter follower at higher frequencies.

MOS Amplifiers [3]: Basic concepts, MOS Small signal model, Common source amplifier with Resistive load.

UNIT –III:

Feedback Amplifiers and Oscillators

Feedback Amplifiers: Concepts of Feedback, Classification of Feedback Amplifiers, General characteristics of Negative Feedback Amplifiers, Effect of Feedback on Amplifier Characteristics, Voltage Series, Voltage Shunt, Current Series and Current Shunt Feedback Configurations, Illustrative Problems.

Oscillators: Classification of Oscillators, Conditions for Oscillations, RC Phase Shift Oscillator, Generalized analysis of LC oscillators - Hartley, and

Colpitts Oscillators, Wien-Bridge & Crystal Oscillators, Stability of Oscillators.

UNIT –IV:

Large Signal Amplifiers : Classification, Class A Large Signal Amplifiers, Transformer Coupled Class A Audio Power Amplifier, Efficiency of Class A Amplifier, Class B Amplifier, Efficiency of Class B Amplifier, Class-B Push-Pull Amplifier, Complementary Symmetry Class B Push-Pull Amplifier, Distortion in Power Amplifiers, Thermal Stability and Heat Sinks.

UNIT –V:

Tuned Amplifiers: Introduction, Q-Factor, Small Signal Tuned Amplifiers, Effect of Cascading Single Tuned Amplifiers on Bandwidth, Effect of Cascading Double Tuned Amplifiers on Bandwidth, Stagger Tuned Amplifiers, Stability of Tuned Amplifiers.

TEXT BOOKS:

1. Integrated Electronics - Jacob Millman and Christos C Halkias, 1991 Ed., 2008, TMH.
2. Electronic Devices and Circuits, B. P. Singh, Rekha Singh, Pearson, 2013.
3. Design of Analog CMOS Integrated Circuits – Behzad Razavi, 2008, TMH.

REFERENCE BOOKS:

1. ElectronicCircuit Analysis – Rashid, Cengage Learning, 2013
2. Electronic Devices and Circuit Theory - Robert L.Boylestad, Louis Nashelsky, 9 Ed., 2008 PE.
3. Microelectric Circuits – Sedra and Smith – 5 Ed., 2009, Oxford University Press.
4. Electronic Circuit Analysis – K. Lal Kishore, 2004, BSP.
5. Electronic Devices and Circuits - S. Salivahanan, N.Suresh Kumar, A Vallavaraj, 2 Ed., 2009, TMH.

Course Outcomes:

Upon completion of the subject, students will be able to:

- Design and analyse the DC bias circuitry of BJT and FET.
- Analyse the different types of amplifiers, operation and its characteristics
- Design circuits like amplifiers, oscillators using the transistors diodes and oscillators.

3. VISION OF THE DEPARTMENT

To impart quality technical education in Electronics and Communication Engineering emphasizing analysis, design/synthesis and evaluation of hardware/embedded software using various Electronic Design Automation (EDA) tools with accent on creativity, innovation and research thereby producing competent engineers who can meet global challenges with societal commitment.

4. MISSION OF THE DEPARTMENT

i. To impart quality education in fundamentals of basic sciences, mathematics, electronics and communication engineering through innovative teaching-learning processes.
ii. To facilitate Graduates define, design, and solve engineering problems in the field of Electronics and Communication Engineering using various Electronic Design Automation (EDA) tools.
iii. To encourage research culture among faculty and students thereby facilitating them to be creative and innovative through constant interaction with R & D organizations and Industry.
iv. To inculcate teamwork, imbibe leadership qualities, professional ethics and social responsibilities in students and faculty

5. PEO'S AND PO'S

5.1 Program Educational Objectives of B. Tech (ECE) Program :

I. To prepare students with excellent comprehension of basic sciences, mathematics and engineering subjects facilitating them to gain employment or pursue postgraduate studies with an appreciation for lifelong learning.
II. To train students with problem solving capabilities such as analysis and design with adequate practical skills wherein they demonstrate creativity and innovation that would enable them to develop state of the art equipment and technologies of multidisciplinary nature for societal development.

To inculcate positive attitude, professional ethics, effective communication and interpersonal skills which would facilitate them to succeed in the chosen profession exhibiting creativity and innovation through research and development both as team member and as well as leader.

5.2 Program Outcomes of B.Tech ECE Program:

1. An ability to apply knowledge of Mathematics, Science, and Engineering to solve complex engineering problems of Electronics and Communication Engineering systems.
2. An ability to model, simulate and design Electronics and Communication Engineering systems, conduct experiments, as well as analyze and interpret data and prepare a report with conclusions.
3. An ability to design an Electronics and Communication Engineering system, component, or process to meet desired needs within the realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability and sustainability.
4. An ability to function on multidisciplinary teams involving interpersonal skills.
5. An ability to identify, formulate and solve engineering problems of multidisciplinary nature.
6. An understanding of professional and ethical responsibilities involved in the practice of Electronics and Communication Engineering profession.
7. An ability to communicate effectively with a range of audience on complex engineering problems of multidisciplinary nature both in oral and written form.
8. The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental and societal context.
9. A recognition of the need for, and an ability to engage in life-long learning and acquire the capability for the same.
10. A knowledge of contemporary issues involved in the practice of Electronics and Communication Engineering profession
11. An ability to use the techniques, skills and modern engineering tools necessary for engineering practice.

12. An ability to use modern Electronic Design Automation (EDA) tools, software and electronic equipment to analyze, synthesize and evaluate Electronics and Communication Engineering systems for multidisciplinary tasks.
13. Apply engineering and project management principles to one's own work and also to manage projects of multidisciplinary nature.

6. Course objectives and outcomes:

Course objectives

1. To develop the basic understanding of amplifier designing and its analysis using hybrid model

2. To make students aware of amplifier operation at low and high frequency and its frequency responses.

3. To make students learn about different types of feedback amplifiers and oscillators.

4. To make students aware of large signal amplifiers.

5. To make students learn about different types of Tuned amplifiers.

Course outcomes:

After finishing the course, the students are able to:

CO1: Explain classification of amplifiers and analyze the CE, CB, CC amplifiers using small signal hybrid model and derive the voltage gain, current gain, input impedance and output impedance.
CO2: Design and analyze the cascaded RC coupled BJT amplifier and different types of the coupled amplifiers.
CO3: Design and analyze single stage amplifiers and their frequency response, its gain band width product and effect of coupling and bypass capacitors in amplifiers.
CO4: Design and analyze different types of the MOS amplifiers and their frequency response by using the small signal model.
CO5: Design and analyze the different types of feedback amplifiers.
CO6: Explain the condition for oscillations in oscillators, design and analyze different types of oscillators.
CO7: Design and analyze different types of power amplifiers and compare them in terms of efficiency.
CO8: Design and analyze the effects of cascading on single, double tuned amplifiers on bandwidth and explain their stability.

7.Brief note on the course & how it fits into the curriculum

This course is a one of the core courses of this program . In order to study VLSI Design, various Analog Design in IV-year I-sem and M.Tech level, it will help to understand the concepts of analog communication subject in III-B.Tech I- sem and also will help to under stand the concepts of IC Applications in III-B.Tech I- sem.

8. Prerequisite, if any

Student should know the basic concepts of Electronics Devices and Circuits and Electrical circuits.

9. INSTRUCTIONAL LEARNING OUTCOMES

After the completition of the each lecture,the students will be able to

1. Analyse different types of single stage amplifiers by using small signal model.
2. Design different types of single stage amplifiers.
3. Identify and calculate different types of distortions and percentage of distortions in amplifiers.
4. Analyse different types of multi stage amplifiers by using small signal model.
5. Design different types of multi stage amplifiers.
6. Distinguish between the different types of cascading schemes in multi stage amplifiers.
7. Analyse different types of single stage amplifiers by using hybrid-pi model.
8. Calculate 3-dB frequencies in multi stage amplifiers.
9. Analyse and design different types of MOS amplifiers by using small signal model.
10. Distinguish between negative and positive feedback in amplifiers.
11. Analyse and Design different types of feedback amplifiers.
12 .Analyse and Design different types of Oscillators.
13. Analyse and Design different types of Power amplifiers and calculate their efficiency.
14. Analyse and Design different types of Tuned amplifiers.

10. Course mapping with PEOs and POs

Relationship of the course to program outcomes :

1.An ability to apply knowledge of Mathematics, Science, and Engineering to solve complex engineering problems of Electronics and Communication Engineering	

systems.	
2.An ability to model, simulate and design Electronics and Communication Engineering systems, conduct experiments, as well as analyze and interpret data and prepare a report with conclusions	✓
3. An ability to design an Electronics and Communication Engineering system, component, or process to meet desired needs within the realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability and sustainability.	✓
4. An ability to function on multidisciplinary teams involving interpersonal skills.	
5. An ability to identify, formulate and solve engineering problems of multidisciplinary nature.	
6.An understanding of professional and ethical responsibilities involved in the practice of Electronics and Communication Engineering profession	
7. An ability to communicate effectively with a range of audience on complex engineering problems of multidisciplinary nature both in oral and written form.	
8.The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental and societal context	
9. A recognition of the need for, and an ability to engage in life-long learning and acquire the capability for the same.	
10.A knowledge of contemporary issues involved in the practice of Electronics and Communication Engineering profession	
11.An ability to use the techniques, skills and modern engineering tools necessary for engineering practice.	
12.An ability to use modern Electronic Design Automation (EDA) tools, software and electronic equipment to analyze, synthesize and evaluate Electronics and Communication Engineering systems for multidisciplinary tasks.	✓
13. Apply engineering and project management principles to one's own work and also to manage projects of multidisciplinary nature	

Relationship of the course to the program educational objectives :

I. To prepare students with excellent comprehension of basic sciences, mathematics and engineering subjects facilitating them to gain employment or pursue postgraduate studies with an appreciation for lifelong learning.	
2. To train students with problem solving capabilities such as analysis and design with adequate practical skills wherein they demonstrate creativity and innovation that would enable them to develop state of the art equipment and technologies of multidisciplinary nature for societal development.	✓
3.To inculcate positive attitude, professional ethics, effective communication and interpersonal skills which would facilitate them to succeed in the chosen profession exhibiting creativity and innovation through research and development both as team member and as well as leader	

Class Time Table

11.Class time table

Time table of concerned classes

Department of Electronics & Communication Engineering								
Year/Sem/Sec: II-B. Tech-I Sem-C Section				Room no.: LH-17		Acad Year 2014-15, WEF: 29-12-2014		
Class Incharge:								
Time	09.30-10.20	10.20-11.10	11.10-12.00	12.00-12.50	12.50-13.30	13.30-14.20	14.20-15.10	15.10-16.00
Period	1	2	3	4	LUNCH	5	6	7
Monday								
Tuesday								
Wednesday								
Thursday								
Friday								
Saturday								

No	Subject(T/P)	Faculty Name	Subject Code	Periods/Week
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				

12.Individual Time table

Individual time table

ECA-II ECE- 2-2 A

Hard copy available

Name: Dr.C.Venkata Narasimhulu			Work Load: 11				W.E.F: 29/12/14	
Day/Hour	**I**	**II**	**III**	**IV**		**V**	**VI**	**VII**
MON								
TUE					**LUNCH**			
WED								
THU								
FRI								
SAT								

13. Lecture schedule with methodology being used/adopted.

UNIT-I: Singlestage and Multistage Amplifiers

(a) Single stage Amplifiers:

(b) Multistage Amplifiers

UNIT-II: BJT Amplifiers and MOS Amplifiers

(a) BJT Amplifiers:

(b) MOS Amplifiers:

UNIT-III: Feedback Amplifiers and Oscillators

(a) Feedback Amplifiers:

(b) Oscillators:

UNIT-IV: Large Signal Amplifiers

UNIT-IV: Tuned Amplifiers

Introduction:

Electronic circuit analysis subject teaches about the basic knowledge required to design an amplifier circuit, oscillators etc..It provides a clear and easily understandable discussion of designing of different types of amplifier circuits and their analysis using hybrid model, to find out their parameters. Fundamental concepts are illustrated by using small examples which are easy to understand. It also covers the concepts of MOS amplifiers ,oscillators and large signal amplifier.

MICROPLAN

Sl.no	Unit	Topics to be covered	Additional topics
1.	**1**	**(a)Single Stage Amplifiers:** classification of amplifiers , Distortion in Amplifiers.	
2.		Analysis of CE configuration using simplified hybrid model.	
3.		Analysis of CB & CC configuration using simplified hybrid model.	
4.		Analysis of CE Amplifier with Emitter resistance.	
5.		Analysis of Emitter follower.	
6.		Millers Theorem and its Dual.	
7.		Design of single stage RC coupled amplifier using BJT.	
8.		Design of single stage RC coupled amplifier using BJT	
9.		Revision class with problems	
10.		Assignment Test	
11.		**(b)Multi Stage Amplifiers:** Analysis of Cascaded RC coupled BJT amplifiers.	Effect of cascading on Bandwidth in multistage amplifiers.
12.		Cascode Amplifier, Darlington pair.	
13.		RC coupled Amplifier, Direct coupled amplifier	
14.		Transformer coupled amplifier.	
15.		Solving University papers- problems.	
16.		Assignment test	
17.	**II**	**(a)BJT Amplifiers Frequency Response:** Logarithims, Decibles, General frequency considerations.	
18.		Frequency response of BJT Amplifier,	
19.		Effect of Coupling capacitor and B ypass capacitor.	
20.		The Hybrid pi- common emitter transistor model.	
21.		CE short circuit current gain, current gain with resistive load.	
22.		Single stage CE transistor amplifier response,Gain bandwidth product.	
23.		Emitter follower at high frequencies.	
24.		Tutorial class	
25.		**(b)MOS Amplifiers:**Basic concepts, MOS small signal model.	Characteristics of MOS transistor to obtain small signal equivalent model
26.		Common Source amplifier with resistive load.	
27.		Diode Connected load and current source load.	
28.		Source follower, folded cascode amplifier and their frequency response.	
29.		Common stage gate cascode amplifier	
30.		Tutorial Class	
31.		Solving University papers	
32.		Assignment test	
33.	**III**	**(a)Feedback Amplfiers:** concepts of feedback and	

		classification of feedback amplifiers	
34.		General charactersistics of negative feedback amplifiers.	
35.		Effect of feed back on amplifier characteristics.	
36.		Voltage shunt and voltage series feedback configurations.	
37.		Current shunt and current series feedback configurations.	Concept of positive feedback its characteristics
38.		Problems	
39.		University papers	
40.		Assignment test.	
41.		**(c)Oscillators:**introduction	
42.		Classification of oscillators	
43.		Conditions for oscillations	
44.		RC phase shift oscillator	
45.		Generalized analysis of LC oscillators	
46.		Hartley and colpitts oscillators	
47.		Wein bridge & crystal oscillators	
48.		Stability of oscillators	
		University papers	
		Assignment test	
49.	**IV**	**Large signal amplifiers**	
50.		Classification ,class A large signal amplifiers	
51.		Transformer coupled class A audio power amplifier,efficiency of class A amplifier	
52.		class B amplifier,efficiency of class B amplifier	
53.		Complementary symmetry class B push pull amplifier	
54.	**V**	**Tuned amplifiers**	
55.		Introduction, Q-factor	Tuned circuits its working principle used in tuned amplifiers
56.		Small signal tuned amplifiers	
57.		Effect of cascading single tuned amplifiers on band width	
58.		Effect of cascading double tuned amplifiers on band width	
59.		Stagger tuned amplifiers,	
60.		Stability of tuned amplifiers	
61.		Solving University papers	
62.		Assignment test	

Unit wise Summary

S.no	Unit	Total no of Periods	Topics to be covered	Reg/ Additional	Teaching aids used LCD/OHP /BB	Remarks
1.	**1**	13	**Single Stage Amplifiers:**classification of amplifiers , Distortion in Amplifiers.	Regular	,BB	
2.			Analysis of CE configuration using simplified hybrid model.	Regular	BB	
3.			Analysis of CB & CC configuration using simplified hybrid model.	Regular	BB	
4.			Analysis of CE Amplifier with Emitter resistance.	Regular	BB	
5.			Analysis of Emitter follower.	Regular	BB	
6.			Millers Theorem and its Dual.	Regular	BB	
7.			Design of single stage RC coupled amplifier using BJT.	Regular	BB	
8.			Design of single stage RC coupled amplifier using BJT		BB	
9.			Revision class with problems	Regular	OHP,BB	
10.			Assignment Test			
11.			**Multi Stage Amplifiers:**Analysis of Cascaded RC coupled BJT amplifiers.	Regular	BB	
12.			Cascode Amplifier, Darlington pair.	Regular	BB	
13.			RC coupled Amplifier, Direct coupled amplifier	Regular	BB	
14.			Transformer coupled amplifier.	Regular	BB	
15.			Effect of cascading on Bandwidth in multistage amplifiers.	**Additional**	BB	
16.			Assignment test			
17.	**II**	14	**BJT Amplifiers Frequency Response:**Logarithims,Decibles, General frequency considerations.	Regular	BB	
18.			Frequency response of BJT Amplifier,	Regular		
19.			Effect of Coupling capacitor and	Regular	BB	

			B y pass capacitor.			
20.			The Hybrid pi- common emitter transistor model.	Regular	OHP,BB	
21.			CE short circuit current gain, current gain with resistive load.	Regular	BB	
22.			Single stage CE transistor amplifier response,Gain bandwidth product.	Regular	BB	
23.			Emitter follower at high frequencies.	Regular	OHP,BB	
24.			Tutorial class	Regular	BB	
25.			**MOS Amplifiers:**Basic concepts, MOS small signal model.	Regular	OHP,BB	
26.			Common Source amplifier with resistive load.	Regular	OHP,BB	
27.			Diode Connected load and current source load.	Regular	BB	
28.			Source follower, folded cascode amplifier and their frequency response.	Regular	OHP,BB	
29.			Common stage gate cascode amplifier	Regular	OHP,BB	
30.			Tutorial Class	Regular	BB	
31.			**Characteristics of MOS transistor to obtain small signal equivalent model**	**Additional**	OHP,BB	
32.			Assignment test			
33.	**III**	15	**Feedback Amplfiers:** concepts of feedback and classification of feedback amplifiers	Regular	BB	
34.			General charactersistics of negative feedback amplifiers.	Regular	OHP,BB	
35.			Effect of feed back on amplifier characteristics.	Regular	OHP,BB	
36.			Voltage shunt and voltage series feedback configurations.	Regular	BB	
37.			Current shunt and current series feedback configurations.		BB	
38.			**Concept of positive feedback its characteristics**	**Additional**	BB	
39.			Problems	Regular	BB	
40.			University papers	Regular	BB	
41.			Assignment test.	Regular	OHP,BB	
42.			**Oscillators:**introduction	Regular	BB	

43.			Classification of oscillators	Regular	BB	
44.			Conditions for oscillations	Regular	BB	
45.			RC phase shift oscillator	Regular	BB	
46.			Generalized analysis of LC oscillators	Regular	BB	
47.			Hartley and colpitts oscillators	Regular	BB	
48.			Wein bridge & crystal oscillators	Regular	BB	
49			Stability of oscillators	Regular	BB	
50			University papers		BB	
51.			Assignment test			
52.	**IV**	12	**Large signal amplifiers:** Classification ,class A large signal amplifiers	Regular	BB	
53.			Transformer coupled class A audio power amplifier,efficiency of class A amplifier	Regular	BB	
54.			class B amplifier,efficiency of class B amplifier	Regular	BB	
55			Complementary symmetry class B push pull amplifier	Regular	OHP,BB	
56.	**V**	10	**Tuned amplifiers:** Introduction, Q-factor	Regular	OHP,BB	
57.			Small signal tuned amplifiers	Regular	OHP,BB	
58.			Effect of cascading single tuned amplifiers on band width	Regular		
59.			Effect of cascading double tuned amplifiers on band width	Regular	BB	
60.			Stagger tuned amplifiers	Regular	BB	
61			**Tuned circuits its working principle used in tuned amplifiers**	**Additional**	BB	
62.			Stability of tuned amplifiers	Regular	BB	
63.			Solving University papers	Regular	OHP,BB	
64.			Assignment test			

GUIDELINES

Distribution of periods:

No. of classes required to cover JNTU syllabus : 64
No. of classes required to cover Additional topics : 4
No. of classes required to cover Assignment tests (for every 2 units 1 test) : 3
No. of classes required to cover tutorials: 8
No. of classes required to cover Mid tests: 2
No of classes required to solve University: 2

14. Detailed notes

UNIT I

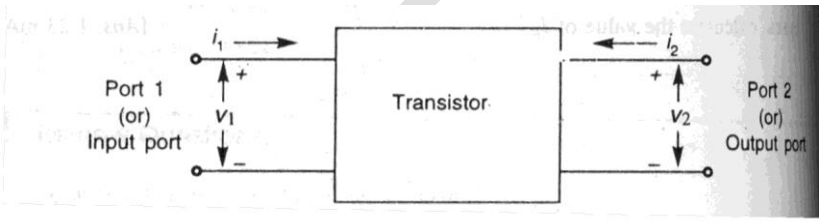
H – Parameter model :-

→ The equivalent circuit of a transistor can be dram using simple approximation by retaining its essential features.

→ These equivalent circuits will aid in analyzing transistor circuits easily and rapidly.

Two port devices & Network Parameters:-

→ A transistor can be treated as a two part network. The terminal behaviour of any two part network can be specified by the terminal voltages V_1 & V_2 at parts 1 & 2 respectively and current i_1 and i_2, entering parts 1 & 2, respectively, as shown in figure.



Two port network

→ Of these four variables V_1, V_2, i_1 and i_2, two can be selected as independent variables and the remaining two can be expressed in terms of these independent variables. This leads to various two part parameters out of which the following three are more important.

1. Z – Parameters (or) Impedance parameters
2. Y – Parameters (or) Admittance parameters
3. H – Parameters (or) Hybrid parameters.

Hybrid parameters (or) h – parameters:-

→ If the input current i_1 and output Voltage V_2 are takes as independent variables, the input voltage V_1 and output current i_2 can be written as

$$V_1 = h_{11}\, i_1 + h_{12}\, V_2$$

$$i_2 = h_{21}\, i_1 + h_{22}\, V_2$$

The four hybrid parameters h_{11}, h_{12}, h_{21} and h_{22} are defined as follows.

$h_{11} = [V_1 / i_1]$ with $V_2 = 0$

= Input Impedance with output part short circuited.

$h_{22} = [i_2 / V_2]$ with $i_1 = 0$

= Output admittance with input part open circuited.

$h_{12} = [V_1 / V_2]$ with $i_1 = 0$

= reverse voltage transfer ratio with input part open circuited.

$h_{21} = [i_2 / i_1]$ with $V_2 = 0$

= Forward current gain with output part short circuited.

The dimensions of h – parameters are as follows:

h_{11} - Ω

h_{22} – mhos

h12, h21 – dimension less.

→ as the dimensions are not alike, (ie) they are hybrid in nature, and these parameters are called as hybrid parameters.

I = 11 = input ; 0 = 22 = output ;

F = 21 = forward transfer ; r = 12 = Reverse transfer.

Notations used in transistor circuits:-

$h_{ie} = h_{11e}$ = Short circuit input impedance

$h_{0e} = h_{22e}$ = Open circuit output admittance

$h_{re} = h_{12e}$ = Open circuit reverse voltage transfer ratio

$h_{fe} = h_{21e}$ = Short circuit forward current Gain.

The Hybrid Model for Two-port Network:-

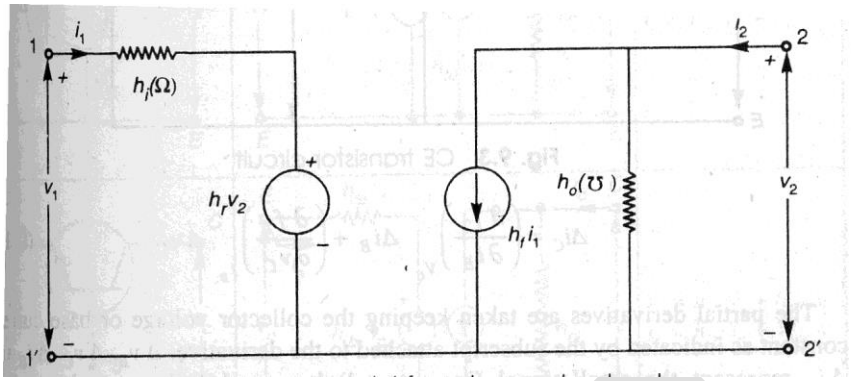
$$V_1 = h_{11} i_1 + h_{12} V_2$$

$$I_2 = h_1 i_1 + h_{22} V_2$$

↓

$V_1 = h_1 i_1 + h_r V_2$

$I_2 = h_f i_1 + h_0 V_2$

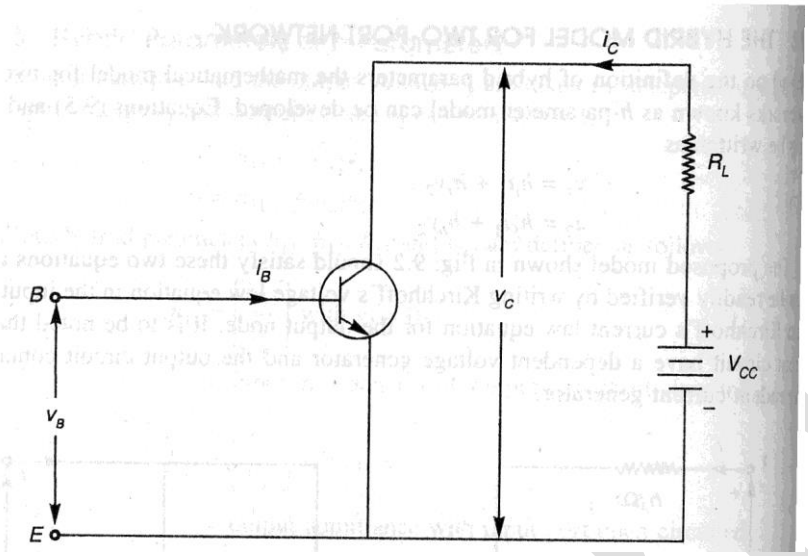


The Hybrid Model for Two-port Network

Transistor Hybrid model:-

Use of h – parameters to describe a transistor have the following advantages.

1. h – parameters are real numbers up to radio frequencies .
2. They are easy to measure
3. They can be determined from the transistor static characteristics curves.
4. They are convenient to use in circuit analysis and design.
5. Easily convert able from one configuration to other.
6. Readily supplied by manufactories.



CE Transistor Circuit

To Derive the Hybrid model for transistor consider the CE circuit shown in figure.The variables are i_B, i_c, $v_{B(=V_{BE})}$ and $v_{c(=V_{CE})}$. i_B and v_c are considered as independent variables.

Then , $v_B = f_1(i_B, v_c)$ ----------(1)

$i_C = f_2(i_B, v_c)$ ----------(2)

Making a Taylor's series expansion around the quiescent point I_B, V_C and neglecting higher order terms, the following two equations are obtained.

$$\Delta v_B = \left(\partial f_1/\partial i_B\right)_{v_c} . \Delta i_B + \left(\partial f_1/\partial v_c\right)_{I_B} . \Delta v_C \quad \text{----------(3)}$$

$$\Delta i_C = \left(\partial f_2/\partial i_B\right)_{v_c} . \Delta i_B + \left(\partial f_2/v_c\right)_{I_B} . \Delta v_C \quad \text{----------(4)}$$

The partial derivatives are taken keeping the collector voltage or base current constant as indicated by the subscript attached to the derivative.

Δv_B , Δv_C , Δi_C , Δi_B represent the small signal(increment) base and collector voltages and currents,they are represented by symbols v_b , v_c , i_b and i_c respectively.

Eqs (3) and (4) may be written as

$$V_b = h_{ie}\, i_b + h_{re}\, V_c$$

$$i_c = h_{fe}\, i_b + h_{oe}\, V_c$$

Where $h_{ie} = \left(\partial f_1/\partial i_B\right)_{v_c} = \left(\partial v_B/\partial i_B\right)_{v_c} = \left(\Delta v_B/\Delta i_B\right)_{v_c} = \left(v_b/i_b\right)_{v_c}$

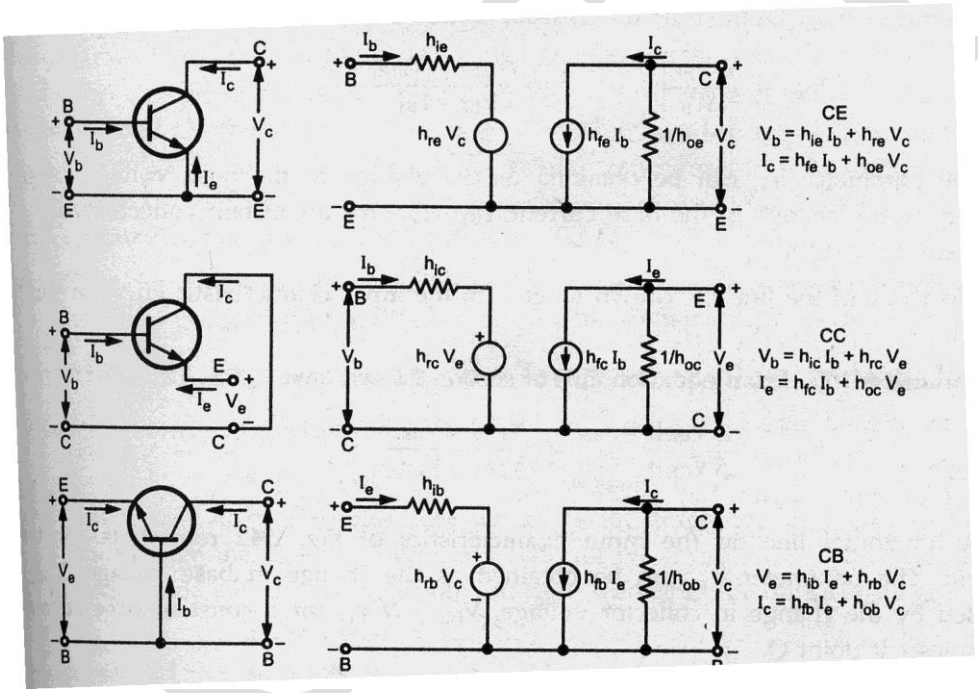
$$h_{re} = \left(\partial f_1/\partial v_c\right)_{I_B} = \left(\partial v_B/\partial v_c\right)_{I_B} = \left(\Delta v_B/\Delta v_c\right)_{I_B} = \left(v_b/v_c\right)_{I_B}$$

$$h_{fe} = \left(\partial f_2/\partial i_B\right)_{v_c} = \left(\partial i_c/\partial i_B\right)_{v_c} = \left(\Delta i_c/\Delta i_B\right)_{v_c} = \left(i_c/i_b\right)_{v_c}$$

$$h_{oe} = \left(\partial f_2/\partial v_c\right)_{I_B} = \left(\partial i_c/\partial v_c\right)_{I_B} = \left(\Delta i_c/\Delta v_c\right)_{I_B} = \left(i_c/v_c\right)_{I_B}$$

The above equations define the h-parameters of the transistor in CE configuration.The same theory can be extended to transistors in other configurations.

Hybrid Model and Equations for the transistor in three different configurations are are given below.



MULTISTAGE AMPLIFIER

- Introduction to feedback (block diagram and types of feedback), Analysis at mode, low and high frequency of multistage amplifier with RC coupling and direct coupling, cascade amplifiers-Darlington Pair.

Concept of multistage / cascade amplifier.

The performance obtainable from a single stage amplifier is often insufficient for many applications, hence several stages may be combined forming a multistage amplifier. These stages may be combined forming a multistage amplifier. These stages are connected in cascade, i.e. output of the first stage is connected to form input of second stage, whose output becomes input of third stage, and so on.

The overall gain of a multistage amplifier is the product of the gains of the individual stage (ignoring potential loading effects):

Gain (A) = $A_1 * A_2 * A_3 * A_4 * \ldots\ldots * A_n$.

Alternately, if the gain of each amplifier stage is expressed in decibels (dB), the total gain is the sum of the gains of the individual stages :

Gain in dB (A) = $A_1 + A_2 + A_3 + A_4 + \ldots\ldots + A_n$.

When we want to achieve higher amplification than a single stage amplifier can offer, it is a common practice to cascade various stages of amplifiers, as it is shown in Fig.1.a. In such a structure the input performance of the resulted multistage amplifier is the input performance of the first amplifier while the output performance is that of the last amplifier. It is understood that combining amplifiers of various types we can create those characteristics that are necessary to fulfill the specifications of a specific application. In addition, using feedback techniques in properly chosen multistage amplifiers can further increase this freedom of the design.

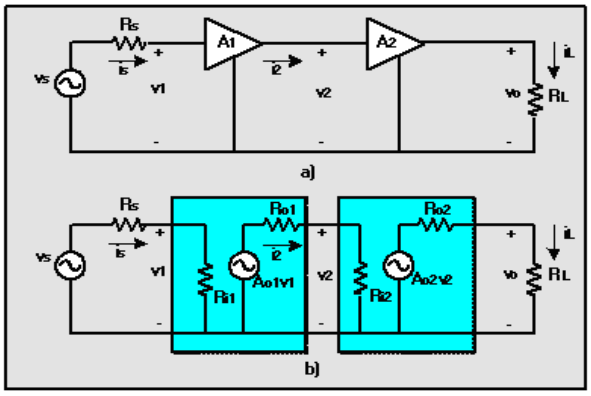


Fig.1 a) A Multistage amplifier configuration **b)** Small-signal equivalent of the amplifier in Fig.1a

According to the small signal equivalent circuit of a two stage amplifier shown in Fig.1.b, we can calculate the ac performance of the circuit.

Voltage amplification:

$$A_v = \frac{v_o}{v_1} = \frac{v_o}{v_2} \cdot \frac{v_o}{v_1} = A_{v2} \cdot A_{vl}$$

Current amplification:

$$A_i = \frac{i_L}{i_s} = \frac{i_L}{i_2} \cdot \frac{i_2}{i_s} = A_{i2} \cdot A_{il}$$

Power amplification:

$$A_p = A_v \cdot A_i = (A_{v2} \cdot A_{12}) \cdot (A_{vl} \cdot A_{il}) = A_{p2} \cdot A_{pl}$$

In conclusion, the gain is the product of the gains of the individual stages (properly terminated).

Analysis of multistage amplifier.

i) RC coupling configuration

One way to connect various stages of a multistage amplifier is via capacitors, as indicated in the two-stage amplifier in Fig.3. where two stages of common emitter amplifiers are coupled to each other by the capacitor C_3.

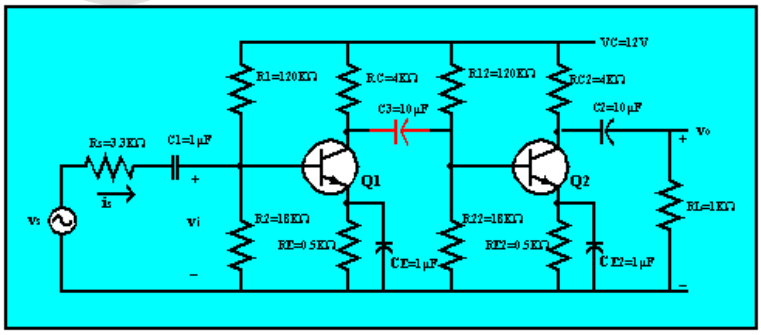
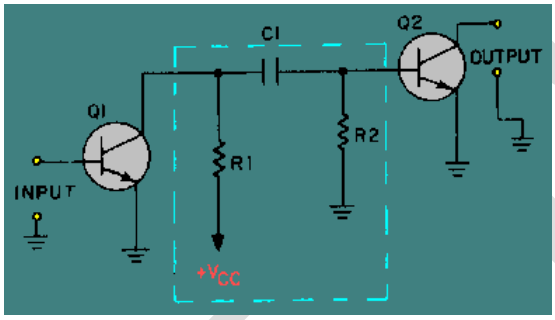


Fig.3 A typical configuration of an RC-coupled amplifier

In RC-coupled amplifiers:

- The various stages are DC isolated. This feature facilitates the biasing of individual stages.
- The various stages can be similar. Hence the design of the amplifier is simplified.
- The coupling capacitors influence the responses of the amplifier.
- A great number of biasing resistors is necessary.



RC-coupled transistor amplifier.

The most commonly used coupling in amplifiers is RC coupling. An RC-coupling network is shown in the illustration above.

The network of R1, R2, and C1 enclosed in the dashed lines of the figure is the coupling network. You may notice that the circuitry for Q1 and Q2 is incomplete. That is intentional so that you can concentrate on the coupling network. R1 acts as a load resistor for Q1 (the first stage) and develops the output signal of that stage. Do you remember how a capacitor reacts to ac and dc? The capacitor, C1, "blocks" the dc of Q1's collector, but "passes" the ac output signal. R2 develops this passed, or coupled, signal as the input signal to Q2 (the second stage).

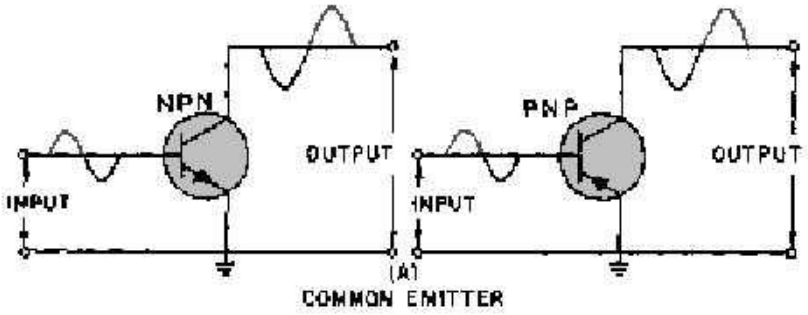
This arrangement allows the coupling of the signal while it isolates the biasing of each stage. This solves many of the problems associated with direct coupling.

ii) Direct coupling configuration

a) The CE-CC configuration

The **COMMON-EMITTER CONFIGURATION (CE)** is the most frequently used configuration in practical amplifier circuits, since it provides good voltage, current, and power gain. The input to the CE is applied to the base-emitter circuit and the output is taken from the collector-emitter circuit, making the emitter the element

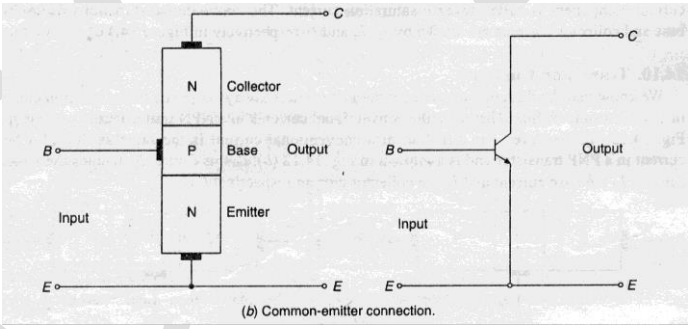
"common" to both input and output. The CE is set apart from the other configurations, because it is the only configuration that provides a phase reversal between input and output signals.



Common emitter configuration:

In this configuration emitter terminal is conncted as a common terminal.

The input is applied between the base and emitter terminals.The output is taken between the collector and base terminals.



Input characteris

The output voltage V_{CE} is maintained constant and the input voltage V_{BE} is set at several convenient levels.For each level of input voltage, the input current I_B is recorded.

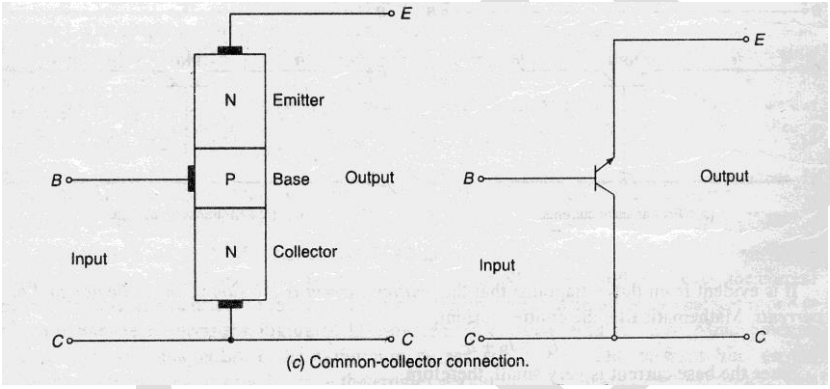
I_B is then plotted versus V_{BE} to give the common-base input character

Output characteristic

The Base current I_B is held constant at each of several fixed levels. For each fixed value of I_B , the output voltage V_{CE} is adjusted in convenient steps and the corresponding levels of collector current I_C are recorded

For each fixed value of I_B, I_C level is Recorded at each V_{CE} step.For each I_B level, I_C is plotted versus V_{CE} to give a family of characteristics.

Common collector configuration:



(c) Common-collector connection.

In this configuration collector terminal is conncted as a common terminal.

The input is applied between the base and collector terminals.The output is taken between the emitter and collector t

Input characteristics:

The common-collector input characteristics are quite different from either common base or common-emitter input characteristics.

The difference is due to the fact that the input voltage **(V_{BC})** is largely determined by **(V_{EC})** level .

$$V_{EC} = V_{EB} + V_{BC}$$

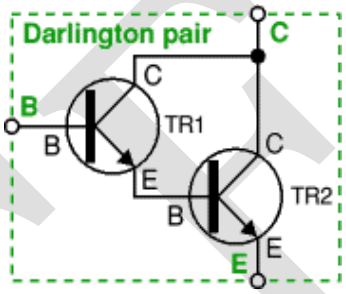
$$V_{EB} = V_{EC} - V_{BC}$$

Output characteristics:

The operation is much similar to that of C-E configuration.When the base current is I_{CO}, the emitter current will be zero and consequently no current will flow in the load.

When the base current is increased, the transistor passes through active region and eventually reaches saturation. Under the saturation conditions all the supply voltage, except for a very small drop across the transistor will appear across the load resistor.

b) The Darlington Pair



This is two transistors connected together so that the amplified current from the first is amplified further by the second transistor. This gives the Darlington pair a very high current gain such as 10000. Darlington pairs are sold as complete packages containing the two transistors. They have three leads (**B**, **C** and **E**) which are equivalent to the leads of a standard individual transistor.

The overall current gain is equal to the two individual gains multiplied together:

Darlington pair current gain, $h_{FE} = h_{FE1} \times h_{FE2}$
(h_{FE1} and h_{FE2} are the gains of the individual transistors)

This gives the Darlington pair a very high current gain, such as 10000, so that only a tiny base current is required to make the pair switch on.

A Darlington pair behaves like a single transistor with a very high current gain. It has three leads (B, C and E) which are equivalent to the leads of a standard individual transistor. To turn on there must be 0.7V across both the base-emitter junctions which are connected in series inside the Darlington pair, therefore it requires 1.4V to turn on.

Darlington pairs are available as complete packages but you can make up your own from two transistors; TR1 can be a low power type, but normally TR2 will need to be high power. The maximum collector current Ic(max) for the pair is the same as Ic(max) for TR2.

A Darlington pair is sufficiently sensitive to respond to the small current passed by your skin and it can be used to make a **touch-switch** as shown in the diagram. For this circuit which just lights an LED the two transistors can be any general purpose low power transistors. The 100kΩ resistor protects the transistors if the contacts are linked with a piece of wire.
Two transistors may be combined to form a configuration known as the Darlington pair which behaves like a single transistor with a current gain equivalent to the product of the current gain of the two transistors. This is especially useful where very high currents need to be controlled as in a power amplifier or power-regulator circuit. Darlington transistors are available whereby two transistors are combined in one single package. The base-emitter volt-drop is twice that of a

small transistor.

ii) The transformer coupling configuration

Figure 3 shows a transformer-coupling network between two stages of amplification. The transformer action of T1 couples the signal from the first stage to the second stage. In figure 1-12, the primary of T1 acts as the load for the first stage (Q1) and the secondary of T1 acts as the developing impedance for the second stage (Q2). No capacitor is needed because transformer action couples the signal between the primary and secondary of T1.

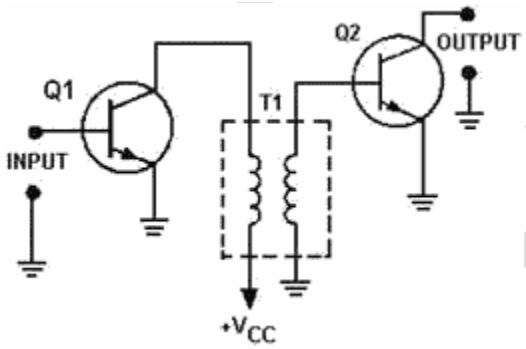
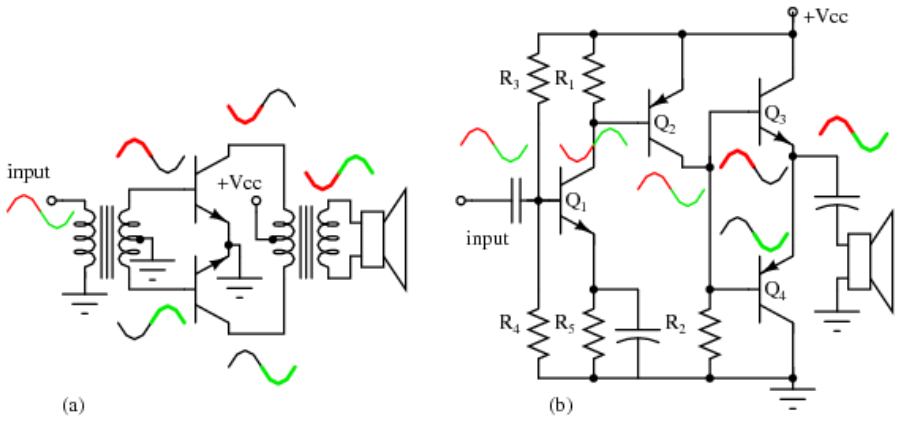


Figure 3.—Transformer-coupled transistor amplifier.

The inductors that make up the primary and secondary of the transformer have very little dc resistance, so the efficiency of the amplifiers is very high. Transformer coupling is very often used for the final output (between the final amplifier stage and the output device) because of the impedance-matching qualities of the transformer. The frequency response of transformer-coupled amplifiers is limited by the inductive reactance of the transformer just as it was limited in impedance coupling.
The circuit in Figure below (a) is a simplified transformer coupled *push-pull* audio amplifier. In push-pull, pair of transistors alternately amplify the positive and negative portions of the input signal. Neither transistor nor the other conducts for no signal input. A positive input signal will be positive at the top of the transformer secondary causing the top transistor to conduct. A negative input will yield a positive signal at the bottom of the secondary, driving the bottom transistor into conduction. Thus the transistors amplify alternate halves of a signal. As drawn, neither transistor in Figure below (a) will conduct for an input below 0.7 Vpeak. A practical circuit connects the secondary center tap to a 0.7 V (or greater) resistor divider instead of ground to bias both transistor for true class B.



(a) Transformer coupled push-pull amplifier. (b) Direct coupled complementary-pair amplifier replaces transformers with transistors.

The circuit in Figure above (b) is the modern version which replaces the transformer functions with transistors. Transistors Q_1 and Q_2 are common emitter amplifiers, inverting the signal with gain from base to collector. Transistors Q_3 and Q_4 are known as a *complementary pair* because these NPN and PNP transistors amplify alternate halves (positive and negative, respectively) of the waveform. The parallel connection the bases allows phase splitting without an input transformer at (a). The speaker is the emitter load for Q_3 and Q_4. Parallel connection of the emitters of the NPN and PNP transistors eliminates the center-tapped output transformer at (a) The low output impedance of the emitter follower serves to match the low 8 Ω impedance of the speaker to the preceding common emitter stage. Thus, inexpensive transistors replace transformers. For the complete circuit see“ Direct coupled complementary symmetry 3 w audio amplifier.

REVIEW:

- Capacitive coupling acts like a high-pass filter on the input of an amplifier. This tends to make the amplifier's voltage gain decrease at lower signal frequencies. Capacitive-coupled amplifiers are all but unresponsive to DC input signals.
- Direct coupling with a series resistor instead of a series capacitor avoids the problem of frequency-dependent gain, but has the disadvantage of reducing amplifier gain for all signal frequencies by attenuating the input signal.
- Transformers and capacitors may be used to couple the output of an amplifier to a load, to eliminate DC voltage from getting to the load.
- Multi-stage amplifiers often make use of capacitive coupling between stages to eliminate problems with the bias from one stage affecting the bias of another.

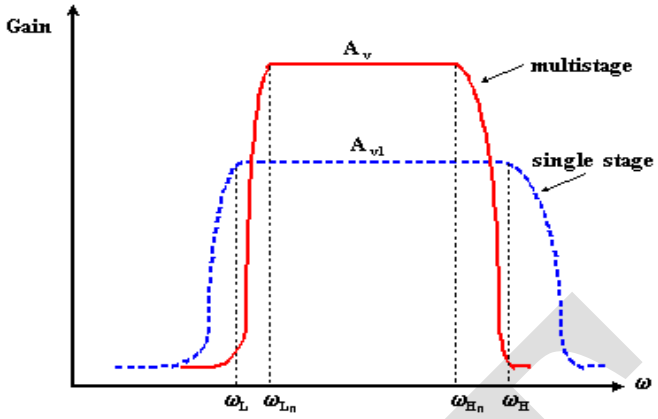
iv) Frequency response curve of multistage amplifier

For a multistage amplifier that consists of n similar stages, the corner cut-off frequencies are given by,

$$\omega_{Ln} = \frac{\omega_L}{(2^{1/n} - 1)^{1/2}} \quad \Rightarrow \quad \omega_{Ln} > \omega_L$$

$$\omega_{Hn} = (2^{1/n} - 1)^{1/2}\,\omega_H \quad \Rightarrow \quad \omega_{Hn} < \omega_H$$

where, ω_L and ω_H are the low and high corner frequencies of the individual stages.



Frequency response

Noise:

- The noise produced by the first stage of a multistage amplifier is the one that dominates the total noise figure of the amplifier.
- Single ended noiseless amplifiers retain the same S/N ratio at the input and output of the amplifier
- Noisy amplifiers have a worst S/N ratio at the output compared to the input

Frequency Response of BJT Amplifiers

All amplifiers typically exhibit a band-pass frequency response as in Figure 1. The cut-off frequency on the low end is usually determined by the coupling and bypass capacitors (if there are no such capacitors the low end extends all of the way to DC). The high frequency limit is typically determined by internal capacitances in the transistor itself.

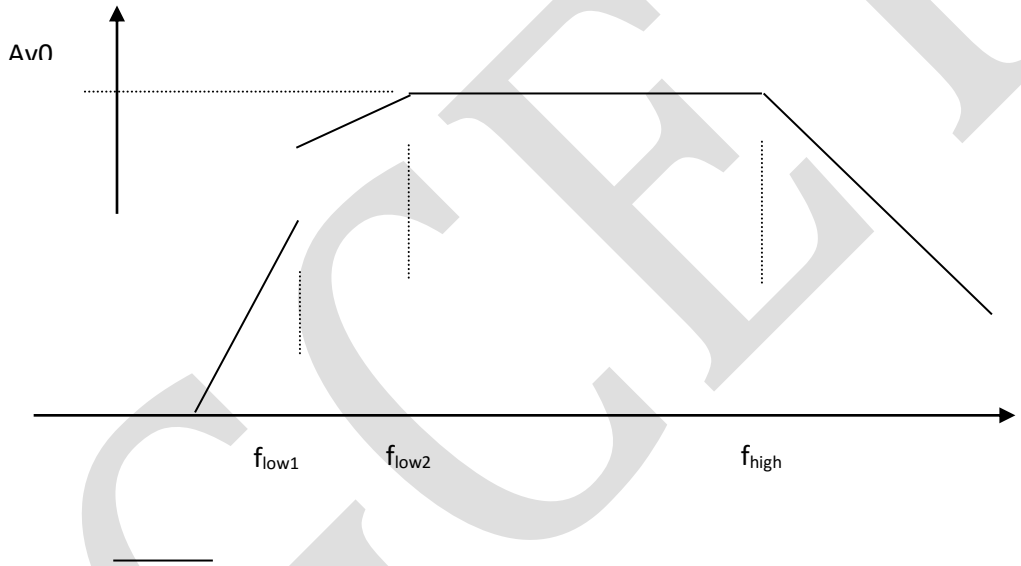


Figure 1 – Frequency response of a typical amplifier.

Low frequency response

If an amplifier does not have coupling or bypass capacitors, then in general the low frequency response goes all of the way down to DC. However, as we discussed in class, it is desirable to have these capacitors in the circuit to isolate the amplifiers DC bias point from the outside world.

In the most general case (Figure 2), the input and output coupling capacitors lead to a high-pass filter response determined by the resistances they see:

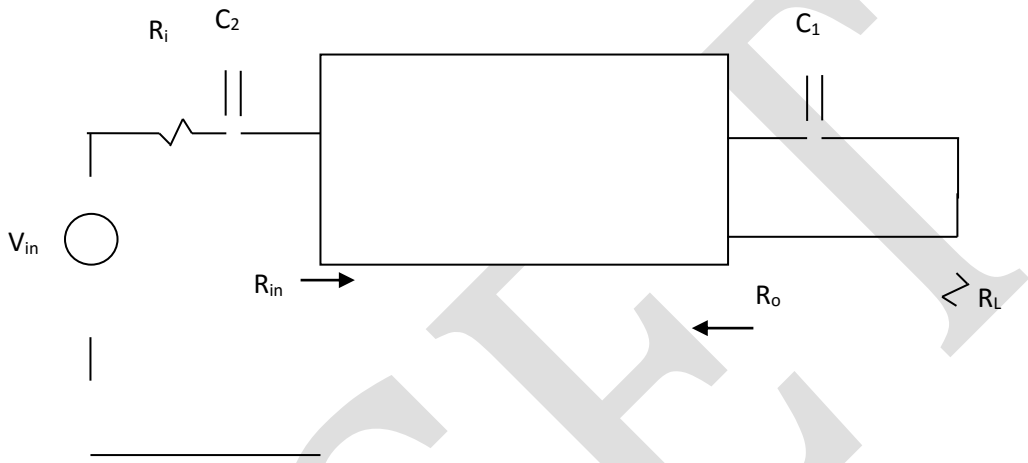


Figure 2 – Two port model of a general amplifier.

In general, we can calculate their cutoff frequencies using the following formulas:

$$f_{Low\_C2} = \frac{1}{2\pi\tau_2} = \frac{1}{2\pi C_2(R_i + R_{in})}$$

$$f_{Low\_C1} = \frac{1}{2\pi\tau_1} = \frac{1}{2\pi C_1(R_o + R_L)}$$

Where R_i is the source resistance, R_L is the load resistance, R_{in} is the input resistance for your amplifier and R_o is the output resistance for your amplifier. These last two are calculated based on the type of amplifier you are working with (See the handout on small signal amplifier calculations).

Once you have calculated the frequencies due to C_1 and C_2, the cutoff is determined by the following rules:

1) If the two frequencies are more than a decade apart then f_{low2} in Figure 1 (the 3db point of the amp) is simply the higher of the two values.
2) If the two frequencies are closer than one decade, then the actual cutoff frequency of the amp is somewhat larger than either of the two calculated frequencies.
3) If the amplifier has a bypass capacitor, then it can also influence the cutoff frequency. Typical, emitter bypass capacitors are chosen large enough so that their effects are negligible.

High Frequency Response

As previously stated, the high frequency response of a discrete transistor amp is determined by the internal capacitances of the transistor itself (Figure 3).

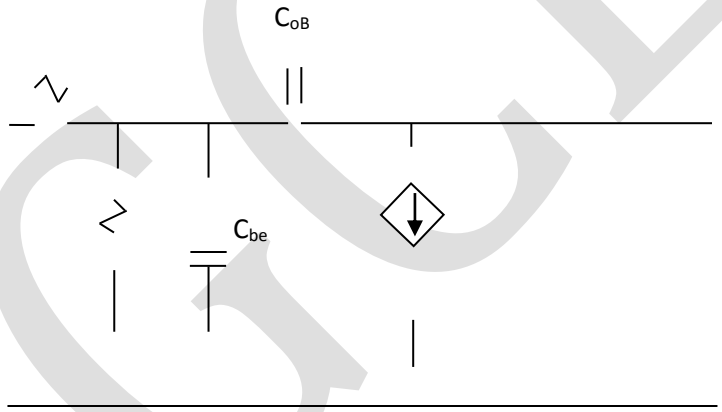


Figure 3 – High frequency model of a BJT

If either C_{be} or C_{oB} short out at high frequencies, then the transistor stops acting as an amplifier and so the response is cut off. The values of C_{be} and C_{oB} can be found or calculated from the transistor spec sheet. Typically, C_{oB} is on the spec sheet and C_{be} is calculated from f_T (the gain-bandwidth product) also found on the spec sheet using:

$$C_{be} = \frac{1}{2\pi f_T h_{ib}} = \frac{\left|I_{CQ}\right|}{52\pi f_T x10^{-3}}$$

Once the capacitance values are known, the high frequency cutoff value can be calculated from the following formulas:

Common Emitter Amp

$$f_{High} = \frac{1}{2\pi(R_{in} \| R_i)(C_{be} + C_{oB}(1 - A_v))}$$

Common Collector Amp

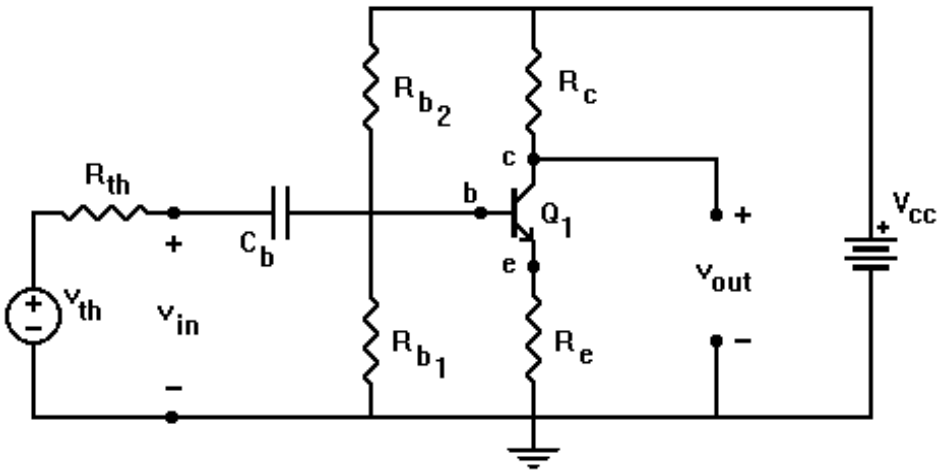
$$f_{High} = \frac{1}{2\pi C_{oB}\left[(R_B \| \beta(R_E \| R_L)\right] \| R_i}$$

Common Base Amp

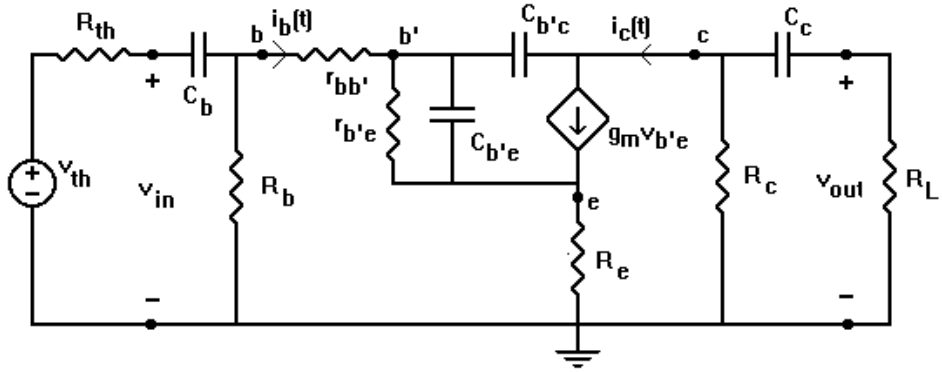
$$f_{High} = \frac{1}{2\pi C_{be}(h_{ib} \| R_E \| R_i)}$$

BJT CE Amplifiers at High Frequencies

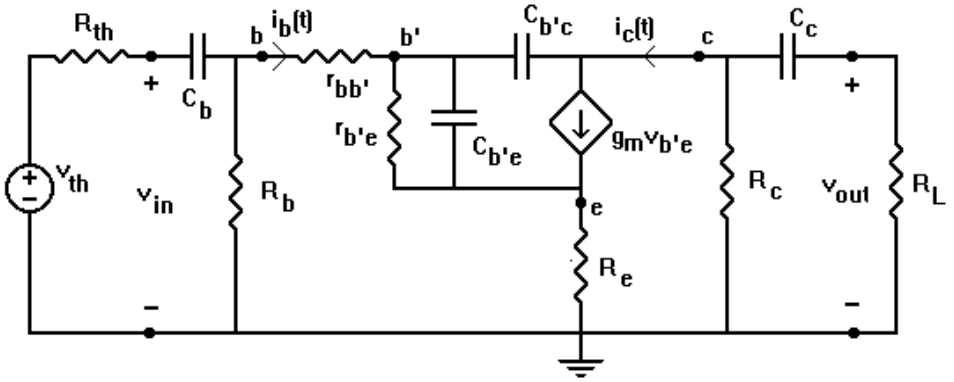
Recall the following common emitter *BJT* amplifier:



If we add a load resistor, R_L, across the amplifier output, the signal equivalent circuit (using the hybrid pi equivalent for the *BJT* and neglecting g_{ce}) is



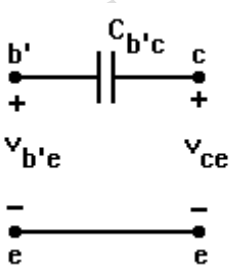
The capacitors $C_{b'c}$ and $C_{b'e}$ represent small capacitances internal to the transistor that are negligible at midband and low frequencies, but which begin to short out and reduce the gain of the amplifier at the upper limit of the midband range of frequencies. Specifically, note that $C_{b'e}$ reduces $v_{b'e}$ as it begins to short out as the frequency increases and hence reduces the size of the dependent source and, thereby, the amplifier gain. The coupling capacitors, C_b and C_c, remember, become short circuits as the frequency increases into the midband range. They certainly are short circuits at the still higher frequencies at which the much smaller capacitors, $C_{b'c}$ and $C_{b'e}$, begin to short out. As we investigate the effects of $C_{b'c}$ and $C_{b'e}$ on high frequency performance, therefore, we can work with the following slightly simpler equivalent circuit:



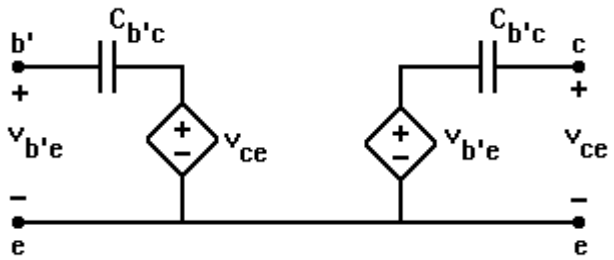
The capacitor, $C_{b'c}$, complicates the analysis of the circuit considerably. Actually, it is not so much that it adds so much complexity that we cannot analyze the circuit. Rather, it clutters the results of the analysis with relatively insignificant terms that make it hard to sort out the essential behavior of the circuit. We, therefore, simplify the circuit before begin the analysis so that we can concentrate on the most important aspects of the circuit's behavior.

We begin by noting that the capacitor, $C_{b'c}$, connects the base and collector circuits of the *BJT*. In effect, it lets part of the base current leak into the collector circuit and, more importantly, lets part of the collector current leak into the base circuit. This perspective suggests, correctly as it turns out, that $C_{b'c}$, affects the base circuit much more than it does the collector circuit. Let's consider this point more carefully.

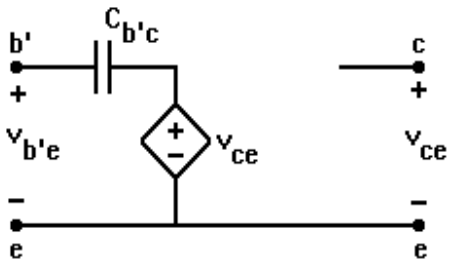
Consider the capacitor, $C_{b'c}$, that connects the base and collector circuits:



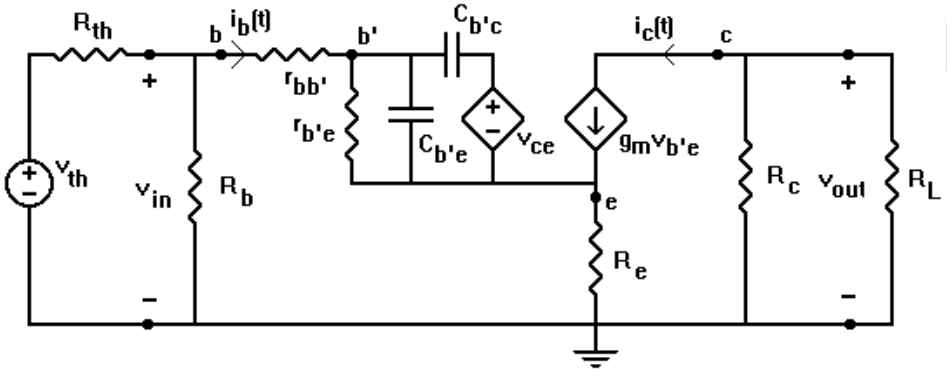
The following circuit presents exactly the same *i-v* characteristics to any circuit(s) connected to terminal pairs *b'e* and *ce*:



Although we know from the original configuration that the current into nodes *b'* and *c* is equal but opposite, the current in the collector circuit is very much larger (roughly β times larger) than the current in the base circuit. As a consequence, we neglect the right hand controlled source and the right hand copy of $C_{b'c}$ and approximate the effects of $C_{b'c}$ by the following simpler equivalent circuit:



Our modified signal equivalent circuit thus becomes:



From this equivalent circuit, we can determine v_{ce} in terms of $v_{b'e}$. We can safely ignore the base current contribution to the current through the emitter resistor, R_e. Thus, we can write:

$$v_{ce}(t) = -\left(R_e + R_c \| R_L\right) g_m \, v_{b'e}(t)$$

Thus the current through the capacitor $C_{b'c}$ is given by

$$i_{C_{b'c}}(t) = C_{b'c} \frac{d\left(v_{b'e} - v_{ce}\right)}{dt} = C_{b'c} \frac{d}{dt}\left[v_{b'e}(t) + \left(R_e + R_c \| R_L\right) g_m \, v_{b'e}(t)\right]$$

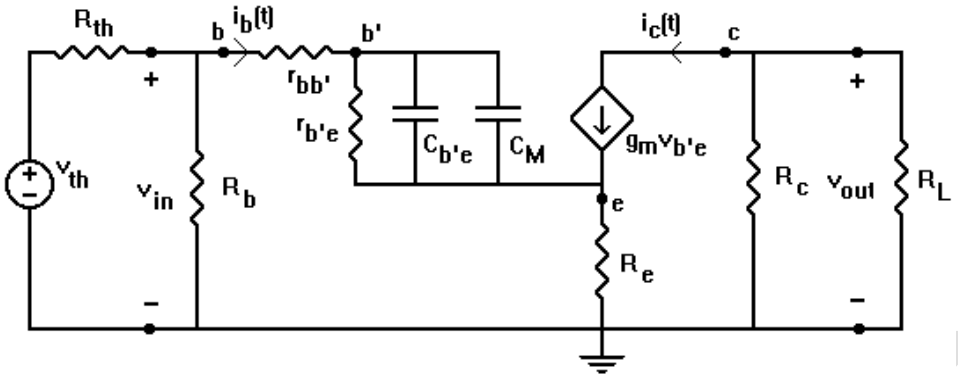
$$i_{C_{b'c}}(t) = \left[1 + g_m\left(R_e + R_c \| R_L\right)\right] C_{b'c} \frac{dv_{b'e}(t)}{dt}$$

Note that the current through $C_{b'c}$, driven by v_{ce} and $v_{b'e}$ in the base circuit, is equal to the current through a capacitor with value

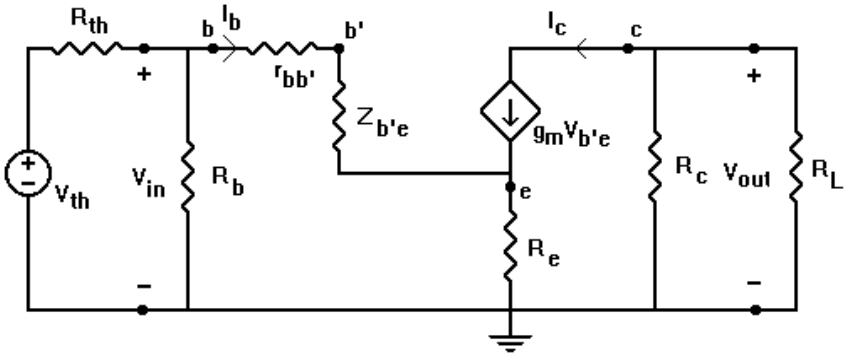
$$C_M \equiv \left[1 + g_m \left(R_e + R_c \| R_L\right)\right] C_{b'c}$$

driven only by $v_{b'e}$. Effectively, $C_{b'c}$, acts like a much larger capacitor in the base circuit because one end is driven by a voltage, v_{ce} that is much larger than $v_{b'e}$. The enhancement of the capacitance is called the *Miller effect*.

We can now draw the equivalent circuit as follows:



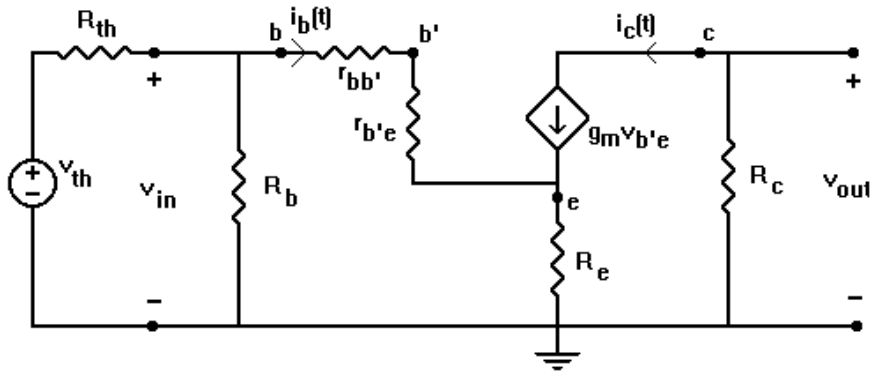
If we convert to phasor representation of the currents and voltages, the equivalent circuit can be redrawn as follows:



where

$$\frac{1}{Z_{b'e}} \equiv \frac{1}{r_{b'e}} + j\omega\left(C_{b'e} + C_M\right)$$

For comparison, recall the signal equivalent circuit for the midband case (with $g_{ce} = 0$ and $R_L \to \infty$):



Note that the high frequency signal equivalent circuit, expressed in phasor notation, is identical in form to the midband signal equivalent circuit, expressed in the time domain. We exploit this identical form, plus the fact that real and complex quantities obey essentially identical rules of algebra, to adapt some of our earlier results for the midband case to the current high frequency case.

First, recall the result for the open-circuit voltage gain at midband:

$$A_{voc} = \frac{v_c}{v_{in}} = \frac{-g_m R_c}{1 + \frac{r_{bb'}}{r_{b'e}} + R_e\left(\frac{1}{r_{b'e}} + g_m\right)}$$

The output Thevenin resistance of the amplifier was found to be simply R_c. These two results mean that the midband gain when the amplifier is loaded with a resistor, R_L, across its output is given by:

$$A_{R_L} = -\frac{R_L}{R_L + R_c}\frac{g_m R_c}{1 + \frac{r_{bb'}}{r_{b'e}} + R_e\left(\frac{1}{r_{b'e}} + g_m\right)}$$

or

$$A_{R_L} = -\frac{g_m R_c \| R_L}{1 + \frac{r_{bb'}}{r_{b'e}} + R_e\left(\frac{1}{r_{b'e}} + g_m\right)}$$

To carry this result over to the high frequency case, we make the following substitutions:

$$A_{R_L} \rightarrow A_{R_L}$$
$$r_{b'e} \rightarrow Z_{b'e}$$

Thus, we see that

$$A_{R_L} = -\frac{g_m R_c \| R_L}{1 + \frac{r_{bb'}}{Z_{b'e}} + R_e\left(\frac{1}{Z_{b'e}} + g_m\right)}$$

$$A_{R_L} = -\frac{g_m R_c \| R_L Z_{b'e}}{Z_{b'e} + r_{bb'} + R_e\left(1 + g_m Z_{b'e}\right)}$$

$$A_{R_L} = -\frac{g_m R_c \| R_L Z_{b'e}}{R_e + r_{bb'} + Z_{b'e}\left(1 + g_m R_e\right)}$$

$$A_{R_L} = -\frac{g_m R_c \| R_L}{1 + g_m R_e} \frac{Z_{b'e}}{\frac{R_e + r_{bb'}}{1 + g_m R_e} + Z_{b'e}}$$

$$A_{R_L} = -\frac{g_m R_c \| R_L}{1 + g_m R_e} \frac{1}{1 + \frac{1}{Z_{b'e}} \frac{R_e + r_{bb'}}{1 + g_m R_e}}$$

$$A_{R_L} = -\frac{g_m R_c \| R_L}{1 + g_m R_e} \frac{1}{1 + \left[\frac{1}{r_{b'e}} + j\omega\left(C_{b'e} + C_M\right)\right] \frac{R_e + r_{bb'}}{1 + g_m R_e}}$$

$$A_{R_L} = -\frac{g_m R_c \| R_L}{1 + g_m R_e} \frac{1}{1 + \frac{1}{r_{b'e}} \frac{R_e + r_{bb'}}{1 + g_m R_e} + j\omega\left(C_{b'e} + C_M\right) \frac{R_e + r_{bb'}}{1 + g_m R_e}}$$

$$A_{R_L} = -\frac{g_m R_c \| R_L}{1 + g_m R_e} \frac{1}{1 + \frac{R_e + r_{bb'}}{r_{b'e} + r_{b'e} g_m R_e} + j \frac{\omega}{\frac{1 + g_m R_e}{\left(C_{b'e} + C_M\right)\left(R_e + r_{bb'}\right)}}}$$

We can simplify this expressions considerably. Recall that

$$g_m = \frac{\beta}{r_{b'e}}$$

and that, for our biasing system,

$$r_{b'e} \approx h_{ie} \approx \frac{0.026\beta}{I_{cq}}$$

$$R_e = \frac{2}{I_{cq}}$$

Then, we see that

$$g_m R_e = \frac{\beta}{\frac{0.026\beta}{I_{cq}}} \frac{2}{I_{cq}} = \frac{2}{0.026} \approx 77 >> 1$$

We can therefore simplify our result for the complex high frequency gain, as follows:

$$A_{R_L} \approx -\frac{R_c \| R_L}{R_e} \frac{1}{1 + j\frac{\omega}{\omega^*}}$$

where

$$\omega^* \equiv \frac{g_m}{(C_{b'e} + C_M)}$$

$$\omega^* \equiv \frac{g_m}{\left(C_{b'e} + \left[1 + g_m\left(R_e + R_c \| R_L\right)\right]C_{b'c}\right)}$$

The frequency, ω^*, marks the upper end of midband. For $\omega \square \omega^*$ (midband), the gain of the amplifier with a load resistance of value R_L is $-\left(R_c \| R_L\right)/R_e$, a value consistent with the open circuit midband gain of $-R_c/R_e$ that we found during our midband analysis of the amplifier. Note that the bandwidth of the amplifier is $\omega^* - \omega_c \approx \omega^*$ which depends on the load resistor, R_L, as well as parameters of the *BJT*. Specifically, note that the gain increases as $R_c \| R_L$ increases but that the bandwidth decreases as $R_c \| R_L$ increases.

It is informative to calculate the product of the magnitude of the midband gain and the bandwidth to obtain the *gain-bandwidth product*, or *GBW*:

$$GBW \approx \frac{R_c \| R_L}{R_e}\omega^* \equiv \frac{R_c \| R_L}{R_e} \frac{g_m}{\left(C_{b'e} + \left[1 + g_m\left(R_e + R_c \| R_L\right)\right]C_{b'c}\right)}$$

where

$$A_{mb} = \frac{R_c \| R_L}{R_e}$$

As we noted above, varying $R_c \| R_L$ permits the designer to trade off gain for bandwidth, and vice versa. Ideally, *GBW* would remain constant as we trade off gain and bandwidth. For this particular amplifier, unfortunately, such usually is not the case. Note, however, that

$$\begin{aligned} GBW &\approx \frac{R_c \| R_L}{R_e} \frac{g_m}{\left(C_{b'e} + \left[1 + g_m \left(R_e + R_c \| R_L \right) \right] C_{b'c} \right)} \\ &< \frac{R_c \| R_L}{R_e} \frac{g_m}{\left[1 + g_m \left(R_e + R_c \| R_L \right) \right] C_{b'c}} \\ &< \frac{R_c \| R_L}{R_e} \frac{1}{\left[\left(R_e + R_c \| R_L \right) \right] C_{b'c}} \\ &< \frac{R_c \| R_L}{R_e} \frac{1}{\left[R_c \| R_L \right] C_{b'c}} \end{aligned}$$

or

$$GBW < \frac{1}{R_e C_{b'c}}$$

Recall that for our biasing approach,

$$g_m R_e \approx 77$$

so that

$$GBW < \frac{1}{77} \frac{g_m}{C_{b'c}} = \frac{1}{77} \frac{C_{b'c} + C_{b'e}}{C_{b'c}} \frac{g_m}{C_{b'c} + C_{b'e}} = \frac{1}{77} \left(1 + \frac{C_{b'e}}{C_{b'c}} \right) \omega_T$$

where quantity

$$\omega_T \equiv 2\pi f_T \equiv \frac{g_m}{C_{b'c}} = \frac{\beta}{r_{b'e} C_{b'c}}$$

is termed the *gain-bandwidth product* of the *BJT* and depends only on the *BJT* parameters. (On specification sheets for *BJT*s, the gain-bandwidth product is usually expressed as f_T, in *Hz*, rather than as ω_T, in *rad/sec*.) In typical small *BJT*s,

$$C_{b'e} \approx 10 C_{b'c}$$

so that

$$GBW < \frac{1}{77}\left(1 + \frac{C_{b'e}}{C_{b'c}}\right)\omega_T \approx \frac{1}{7}\omega_T$$

or, for the common emitter amplifier,

$$GBW << \omega_T$$

Thus, the gain-bandwidth product for the common emitter *BJT* amplifier configuration is substantially less than ω_T, the gain-bandwidth product for the *BJT*. In contrast, a (*BJT*) emitter follower amplifier (with a voltage gain of nearly one) has a gain-bandwidth product only slightly less than ω_T. In some sense, then, the common emitter *BJT* amplifier configuration is wasteful of the gain-bandwidth product of the *BJT*. This feature of the configuration may, or may not, be important to a designer for a particular situation.

It turns out that any amplifier built with an amplifying device (*FET*, *BJT*, opamp or vacuum tube) with a gain-bandwidth product, ω_T, has a gain-bandwidth product that is no more than ω_T.

Conveniently for designers, some amplifier configurations, including operational amplifiers, maintain a constant *GBW* as negative feedback is used to trade off gain and bandwidth. By adjusting the amount of negative feedback, therefore, a designer can trade gain and bandwidth to meet the specific requirements of particular design problem.

Proceeding as before, we can find the Bode plot for the high frequency end of midband to be given by:

$$G_{db} \equiv 20 \log_{10}\left|A_{R_L}\right| \approx \begin{cases} 20 \log_{10}\left(A_{mb}\right) & \omega \square \ \omega^* \\ 20 \log_{10}\left(A_{mb}\right) - 20 \log_{10}\left(\frac{\omega}{\omega^*}\right) & \omega \square \ \omega^* \end{cases}$$

where

$$A_{mb} = \frac{R_c \| R_L}{R_e}$$

and

$$\phi \approx \begin{cases} -\frac{\pi}{2} & \omega \ll \omega^* \\ 0 & \omega \gg \omega^* \end{cases}$$

Proceeding as in the analysis for the midband case, we find that the output Thevenin resistance is, once again, R_c. The input Thevenin resistance, again, is approximately R_b.

MOSFET Amplifiers

The Basic Principles of Common Source NMOS Amplifiers

In Fig. 2.1-1, we show an NMOS circuit with its I-V curves and a load line.

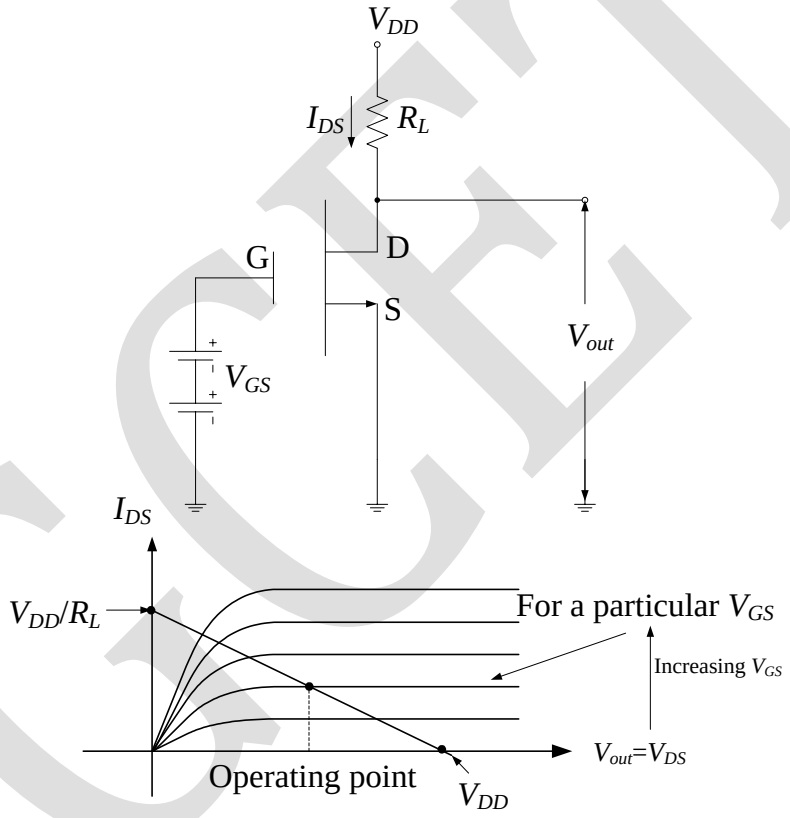


Fig. 2.1-1 An NMOS circuit without any AC

In Fig. 2.1-2, an input signal v_{in} is added to V_{GS}. We shall show later that V_{in} will be amplified. Since the source is signal grounded, we shall call this kind of amplifiers common source amplifiers. It must be noted that the signal is a small signal and is also an alternating current (AC) signal. It will become clear that this kind of amplifiers can hardly amplify large signals.

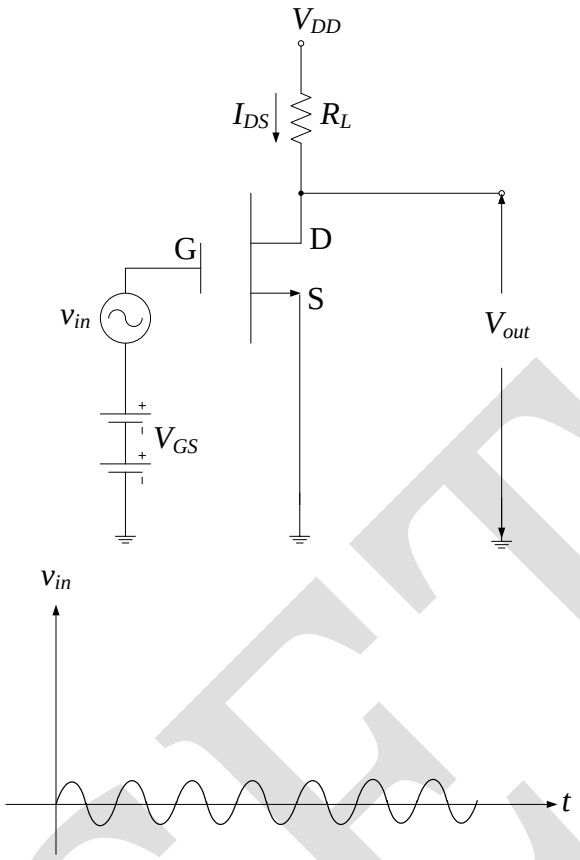


Fig 2.1-2 An NMOS circuit with an AC signal

Consider Fig. 2.1-3. As shown in Fig. 2.1-3, the input signal induces an AC voltage between gate and source. Let us denote this AC voltage by v_{gs}. Throughout this lecture notes, we shall use small letters to denote AC parameters. Obviously, $v_{gs} = v_{in}$. In Fig. 2.1-2, we can see that

$$V_{in} = V_{GS} + v_{in} = V_{GS} + v_{gs}$$
$$V_{out} = V_{DS} + v_{out}$$
$$I_{out} = I_{DS} + i_{out}$$

Since the amplitude of v_{out} is larger than that of v_{in}, this circuit functions as an amplifier. It is important to note that the DC voltage V_{DS} still exists. In some sense, we may say that v_{out} (AC) rides on V_{DS} (DC). But, so far as amplification is concerned, we are only interested in the AC output voltage signal v_{out}. Note that the polarity of v_{out} id opposite to that of v_{in}. In other words, the input is inverted.

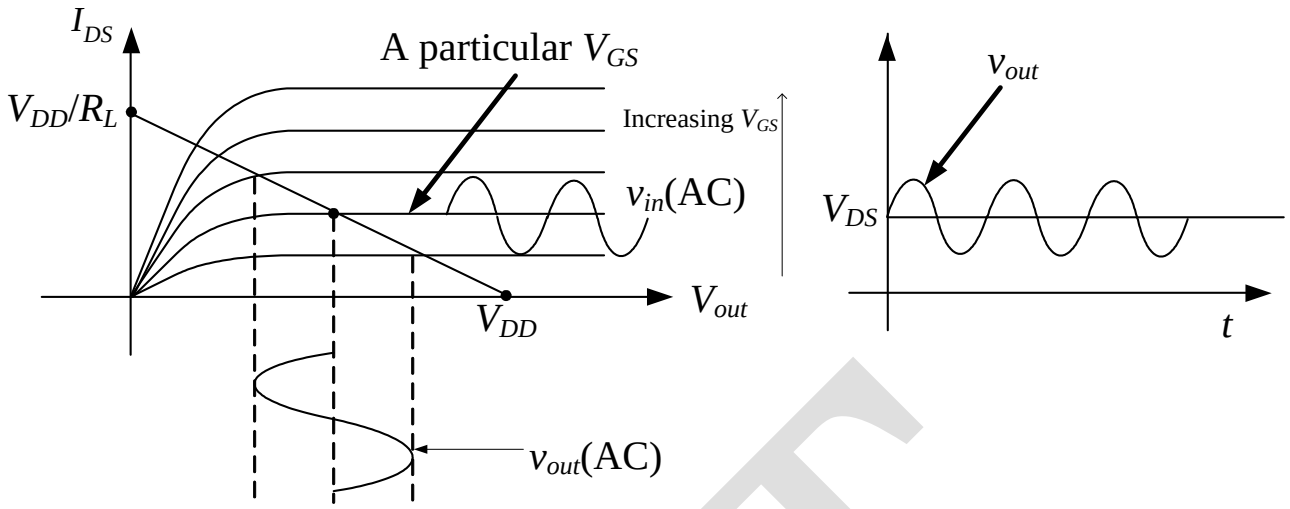


Fig. 2.1-3 The amplification of v_{in}

Suppose a smaller load R_L is used, as shown in Fig. 2.1-4. This amplifier will not function very well now because v_{out} is not significantly different from v_{in}.

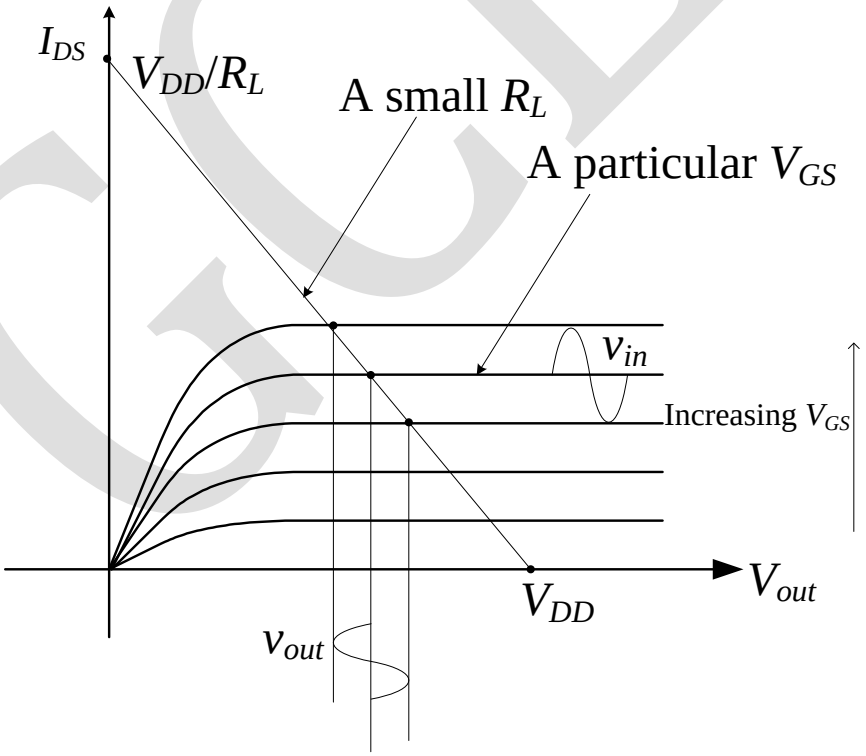


Fig. 2.1-4 The behavior of an amplifier with a small load

It will be shown later that a large load is usually desirable and needed. But, this may drive the transistor out of saturation, as shown in Fig. 2.1-5. Once the transistor is out of saturation, the output signal will be distorted and the circuit is no longer an amplifier any more.

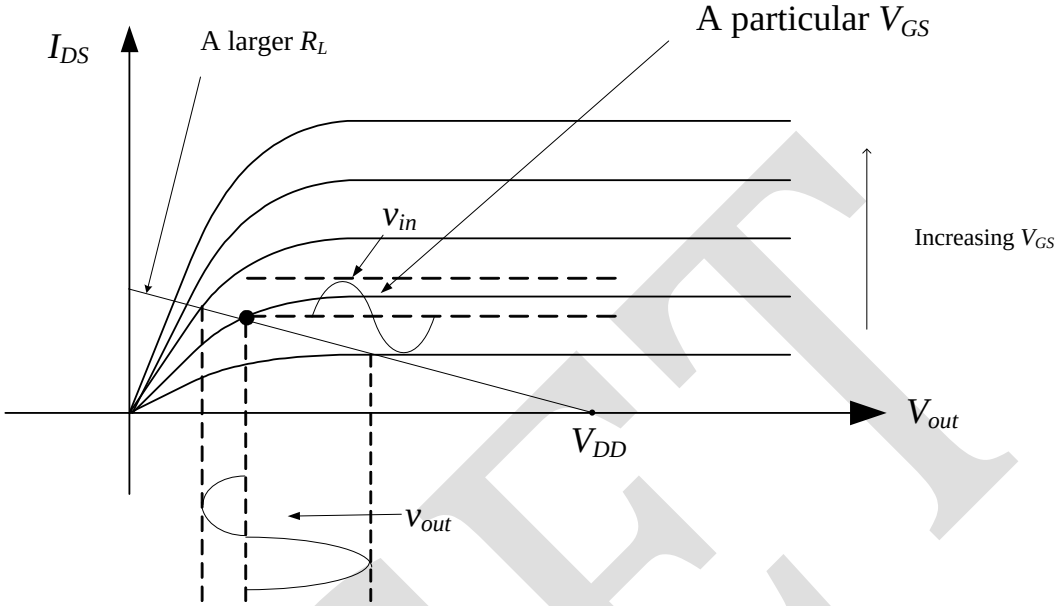


Fig. 2.1-5 A large R_L driving the transistor out of saturation

On the other hand, if V_{GS} is not proper, the output signal will also be distorted, as shown in Fig.2.1-6.

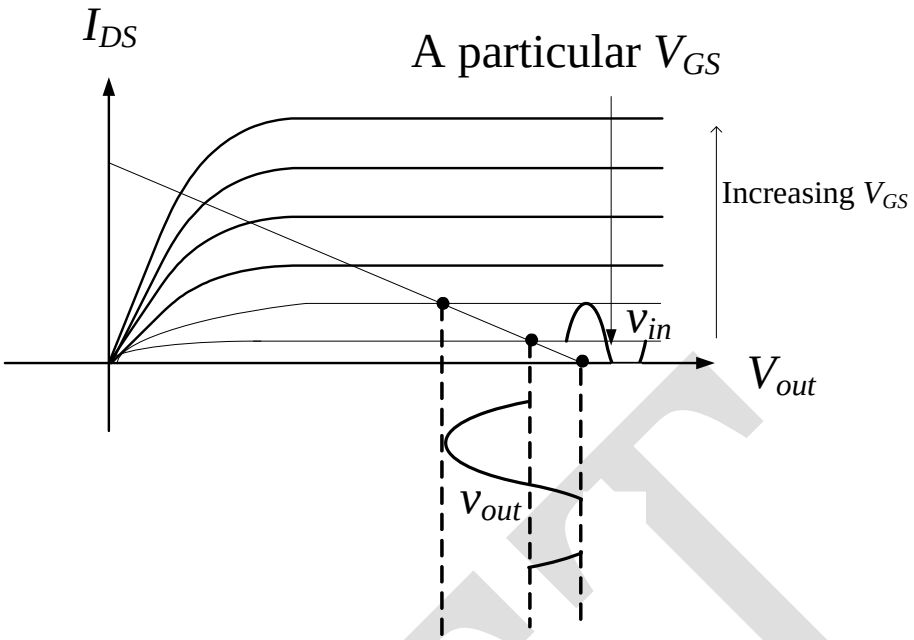


Fig. 2.1-6 An improper V_{GS} causing the distortion of v_{out}

The DC Analysis of An NMOS Common e Amplifier

In this section, we shall show that the performance of an amplifier can be easily understood by having a DC analysis of the circuit. That is, we temporarily ignore the existence of the AC input signal and concentrate our mind on the DC parameters.

Consider Fig. 2.2-1.

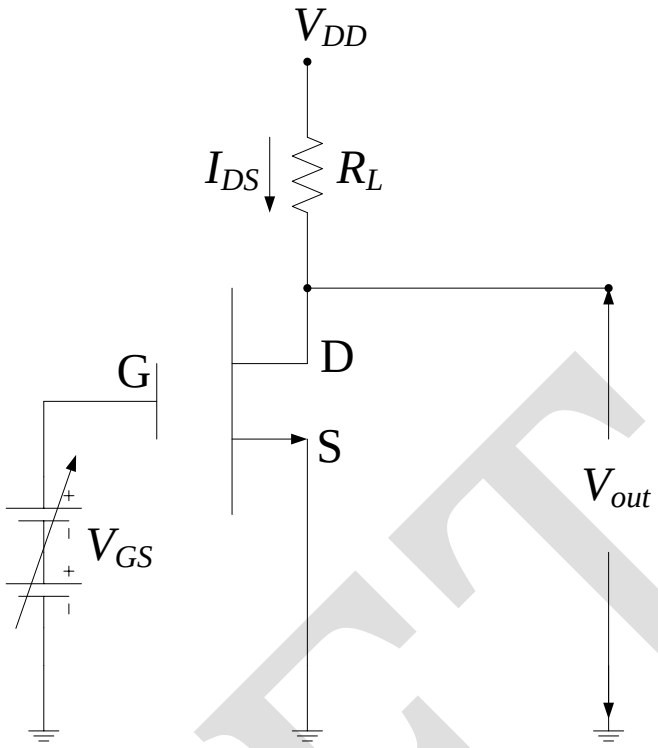


Fig. 2.2-1 An amplifier circuit

We shall first see how the value of the load R_L affects the performance of the amplifier. Fig. 2.2-2 shows three possible cases of R_L. As we showed before, if the load R_L is small, the change of V_{GS} will induce only a small change of V_{DS}, which is also V_{out} in our case. On the other hand, for a large R_L, even a small change of V_{GS} will induce a large change of V_{out}.

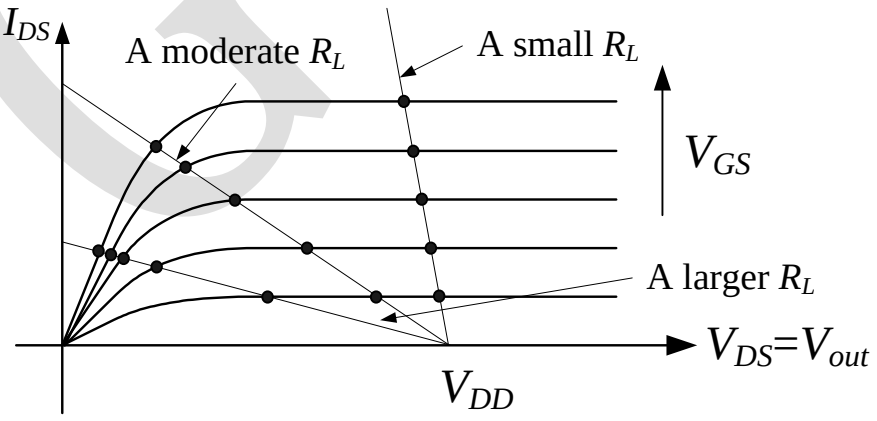


Fig. 2.2-2 I-V curves and different load lines for the circuit in Fig. 2.2-1

Let us assume that the load R_L is small. Fig. 2.2-3 shows the relationship between V_{GS} and V_{out}. In this case, V_{out} falls slowly as V_{GS} rises. We added the AC small signals onto the diagram. It can be seen that v_{out} is quite small. Thus the amplifier does not function well as an amplifier.

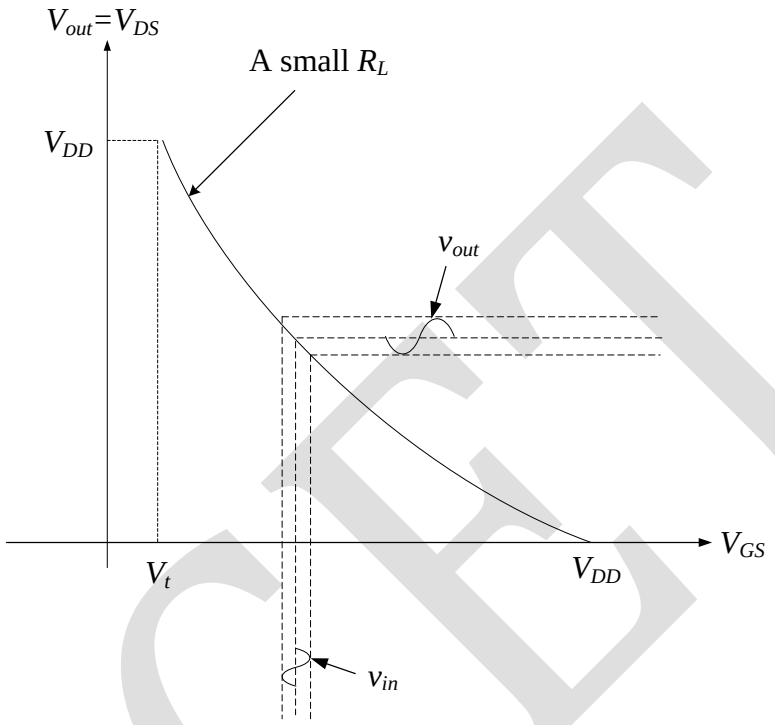


Fig. 2.2-3 V_{out} vs V_{GS} for small R_L

Fig. 2.2-4 shows the situation where R_L is large. It can be seen that the sharp drop of V_{out} will induce a large output v_{out} and thus a large amplification.

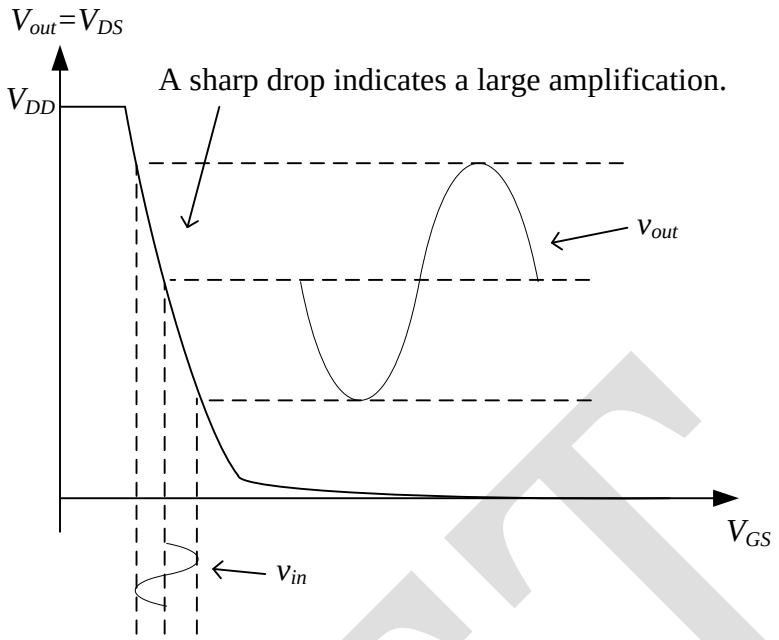


Fig. 2.2-4 V_{out} vs V_{GS} for large R_L

It should also be seen from Fig. 2.2-5 that in this case, there is a very narrow region for the proper biasing voltage V_{GS}. In other words, we must be very careful in selecting the biasing voltage. We shall see later in many experiments that a slight deviation from a proper V_{GS} may cause great trouble for the amplifier. Thus we may say that a DC analysis of an amplifier is always important as it gives us information about how to set the gate bias voltage.

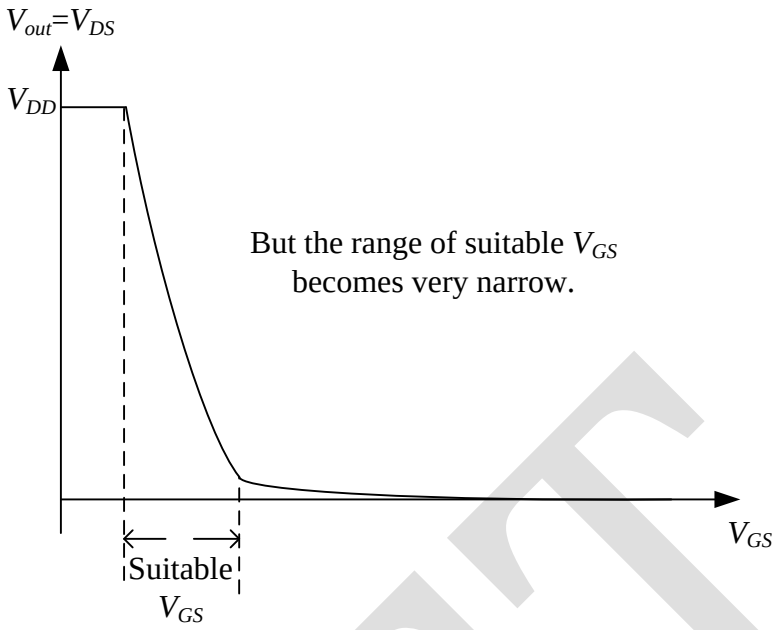


Fig. 2.2-5 The proper selection of the gate biasing voltage

The Creation of the AC Current i_{out} in the Transistor

In the above section, we presented the DC analysis of an amplifier. This explains why the circuit works as an amplifier. But, it does not give us any idea about the gain of the amplifier. In other words, it does not let us know how much the input signal voltage is amplified. To find the gain, an AC analysis is needed.

An amplifier behaves as an amplifier because an AC current is created because of the input voltage v_{in}, which is also v_{gs}. In the following, we shall first explain how this AC current, namely i_{out}, is produced. We then proceed to show how this i_{out} affects v_{out}.

We first point out that the transistor must be in the saturation region and the load line cannot interest the I-V curve at the boundary between the linear tregion and the saturation region. Let us assume that the gate bias voltage is V_{gs} and the operating point V_{DS} is V_{op}. Let the input signal be v_{in}. Then the gate voltage swings from $V_{gs}-v_{in}$ to $V_{gs}+v_{in}$. This causes V_{DS} to swing from $V_{op}+\Delta v_1$ to $V_{op}-\Delta v_2$ where $V_{op}+\Delta v_1 (V_{op}-\Delta v_2)$ is the intersection of the load line and the I-V curve corresponding to $V_{gs}-v_{in} (V_{gs}+v_{in})$. Suppose the load line intersects at the boundary between the

linear region and the saturation region of the I-V curve corresponding to V_{gs}. Then most likely $\Delta v_1 > \Delta v_2$. This will cause distortion of the output signal v_{out}. This can be easily seen in Fig. 2.3-1.

It can be easily seen that if the load is too large, both Δv_1 and Δv_2 will be very small. In such a situation, there will be almost no amplification.

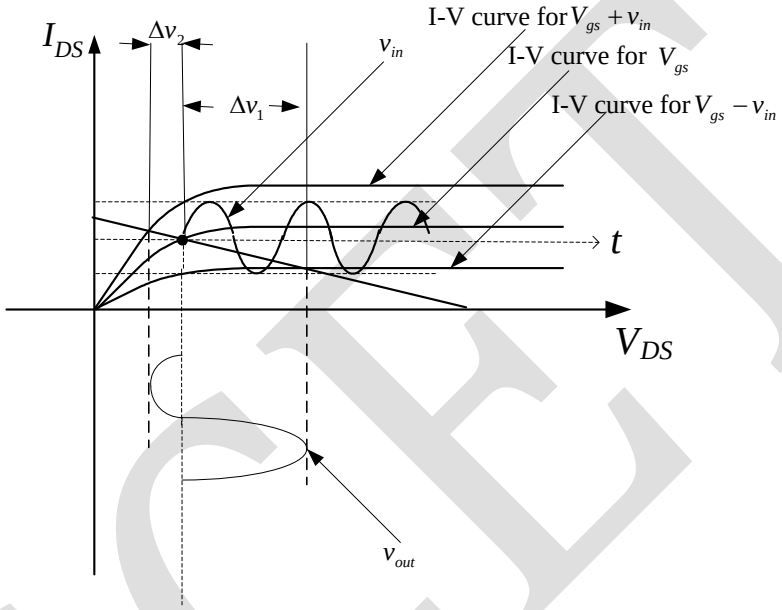


Fig. 2.3-1 The case where the transistor is out of saturation and distortion occurs

Once the transistor is in the saturation region, we may use Equation (1.2-3) which we display again as follows:

$$\begin{aligned} I_{out} &= \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS} + v_{in} - V_t)^2 \\ &= \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2 + k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)v_{in} + \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{in}^2 \end{aligned} \quad (2.3\text{-}1)$$

In the above equation, the third term is very small because v_{in} is very small and the first term is a DC term. Thus so far as AC signal is concerned, we have

$$i_{out} = k_n' \left(\frac{W}{L} \right) (V_{GS} - V_t) v_{in} \qquad (2.3\text{-}2)$$

We define

$$g_m = \frac{i_{out}}{v_{in}} = k_n' \left(\frac{W}{L} \right) (V_{GS} - V_t) \qquad (2.3\text{-}3)$$

Equivalently, we have

$$i_{out} = g_m v_{in} = g_m v_{gs} \qquad (2.3\text{-}4)$$

Equation (2.3-4) indicates that the input voltage v_{in} creates an AC current i_{out} linearly because g_m is a constant once V_{GS} is fixed. It should be noted that there is still a DC current I_{DS}. We may say that i_{out} (AC) rides on this I_{DS} (DC) as shown in Fig. 2.3-2.

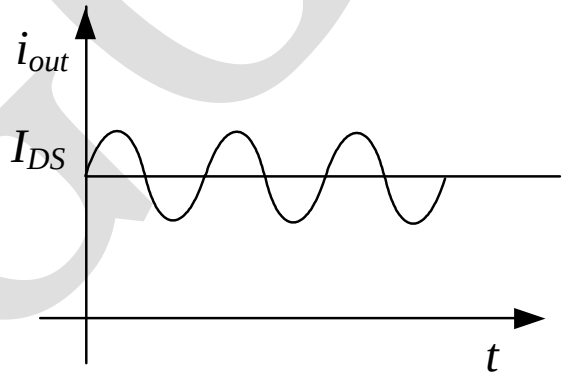


Fig. 2.3-2 i_{out} riding on I_{DS}

The Determination of v_{out}

In the above section, we showed that the input voltage v_{in} creates an AC current i_{out}. This current of course would in turn create an AC output voltage v_{out}. We shall explain its mechanism in this section.

Let us redraw again the amplifier circuit as shown in Fig. 2.4-1.

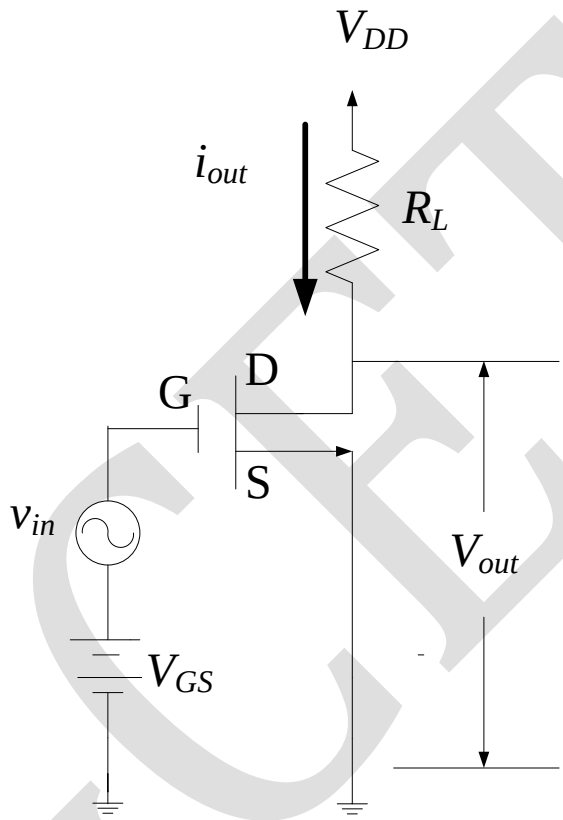


Fig. 2.4-1 An amplifier circuit

We first show that the i_{out} will affect the output voltage because of the existence of R_L. This can be seen by examining Fig. 2.4-2 which illustrates how i_{out} affects v_{out}.

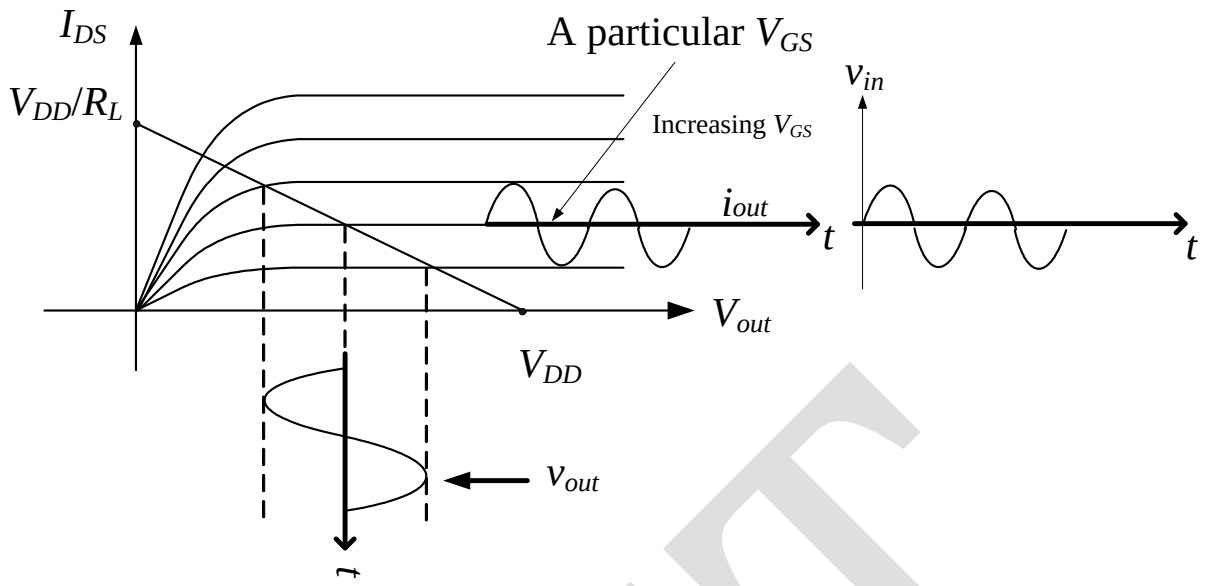


Fig. 2.4-2 The inducing of v_{out} by i_{out}

Note the following:

(1) The input signal v_{in} changes V_{GS}. That is, v_{in} induces an AC voltage v_{gs}.

(2) This voltage v_{gs} in turn induces a change of current I_{DS}. That is, the AC voltage v_{gs} induces an AC output current labeled as i_{out}.

(3) **As can be seen from Fig. 2.4-2, i_{out} finally changes V_{DS}. That is, it induces an AC output voltage, labeled as v_{out}.**

As can be from Fig. 2.4-2, when i_{out} rises, v_{out} falls and when i_{out} falls, v_{out} rises. Thus, the polarity of v_{out} is opposite to the polarity of i_{out}. From Fig. 2.4-1, we have

$$\begin{aligned} V_{out} &= V_{DD} - I_{out}R_L \\ &= V_{DD} - (I_{DS} + i_{out})R_L \end{aligned} \qquad (2.4\text{-}1)$$

This shows that there is an AC output voltage caused by the existence of R_L. However, we shall not let the AC output voltage simply be equal to -$i_{out}R_L$ at this moment because there is another factor which will affect v_{out}, as we will explain below.

We usually assume that in the saturation region, the I-V curve of the transistor is rather flat. In reality, it is not so flat, as illustrated in Fig. 2.4-3.

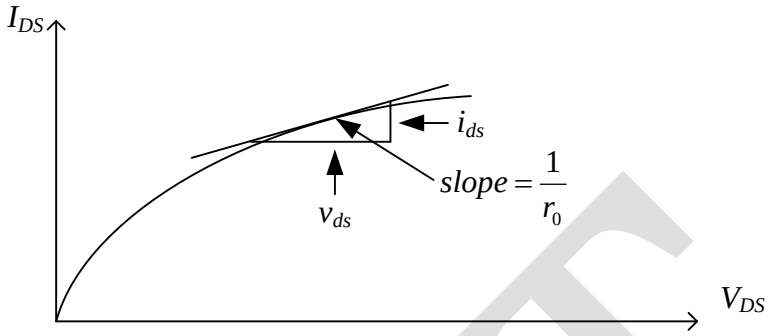


Fig. 2.4-3 The meaning of r_0

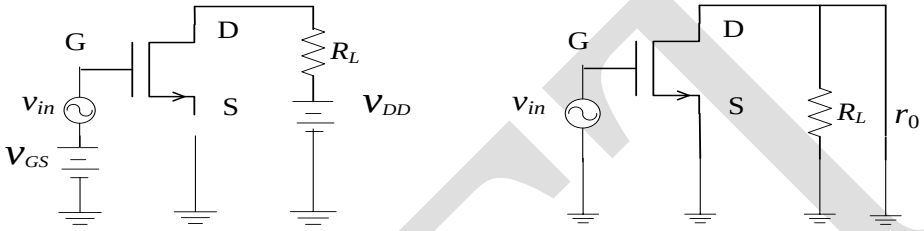
Traditionally, we are familiar with the fact that the change of voltage will cause a change of current. In this case, it is opposite. **If there is a small signal AC current i_{ds}, a small signal AC voltage v_{ds} will be induced.** In other words, the AC current i_{ds} will induce an AC voltage v_{ds}. Thus, we may define the output impedance r_0 as

$$r_0 = \frac{v_{ds}}{i_{ds}} \qquad (2.4\text{-}2)$$

to illustrate the relationship between i_{ds} and v_{ds}. **It must be noted that this r_0 exists because of the I-V curves, not because of the load R_L. If the slope of the $I-V$ curve is very flat, r_0 will be quite large; otherwise, it will be quite small. A large r_0 indicates that a small i_{ds} will induce a large v_{ds}. To put this in another word, we may that a more flat $I-V$ is desirable for us to obtain a better amplifier.**

From the above discussion, we know that v_{out} will be affected by i_{out}, R_L and r_0. In the following, we shall explain how v_{out} is determined.

Let us take a look at the amplifier circuit in Fig. 2.4-1. There are DC voltages in the circuits. They are V_{GS} and V_{DD}. If they are not proper, the amplifier will not work. On the other hand, if they are proper, since v_{out} is an AC voltage, it will not be affected by the existence of these DC voltages. We therefore first short-circuit all of the DC voltages, namely V_{GS} and V_{DD}. One must note that one terminal of V_{DD} is connected to R_L and another terminal is connected to ground, as shown in Fig. 2.4-4(a). Once we short-circuit V_{DD}, R_L will be connected to ground and the amplifier circuit becomes that shown in Fig. 2.4-4(b). In Fig 2.4-4(b), there is also an r_0 connected between D and S(ground).



(a) An amplifier circuit with DC voltage (b)The amplifier circuit with DC voltages short-circuited

Fig. 2.4-4 The short-circuiting of DC voltages in an amplifier circuit

As we discussed before, a small signal input voltage $v_{in} = v_{gs}$ induces a small signal current i_{ds}. The relationship between v_{gs} and i_{ds} can be found in Equation (2.3-4), namely $i_{ds} = g_m v_{gs}$. As shown in Equation (2.3-4), v_{gs} and i_{ds} are of the same polarity. This is illustrated in Fig. 2.4-5. Note that there is no connection between Node G and Node S as there is no current flowing into the gate. That is, there is a voltage between G and S, but no current from G.

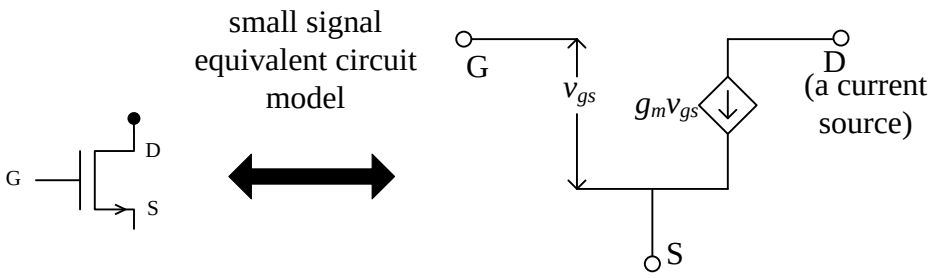
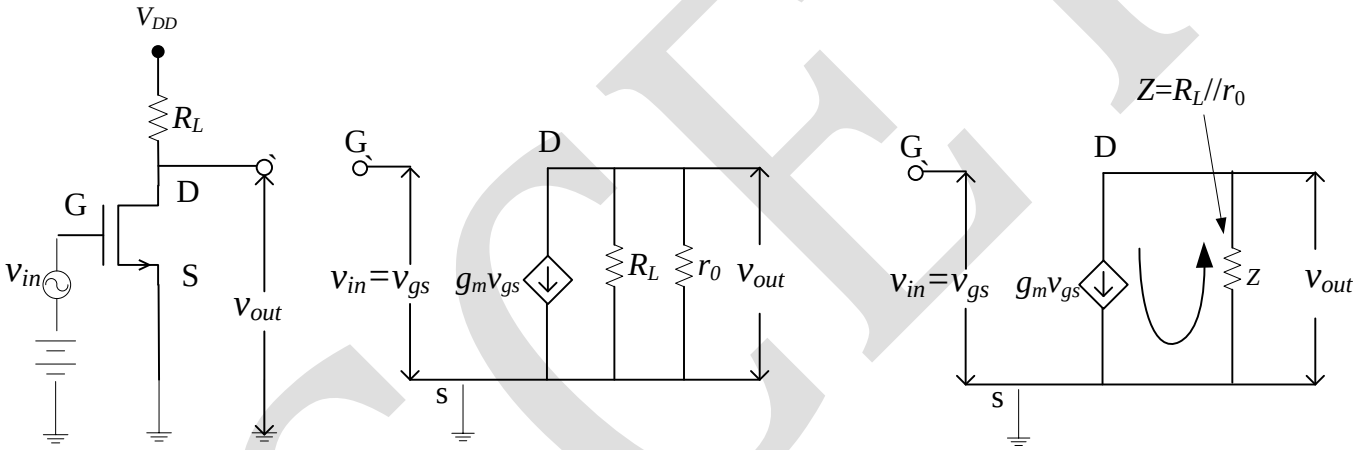


Fig. 2.4-5 Small signal equivalent circuit of a transistor

Because of the short-circuiting of DC voltages, R_L is across D and S as shown in Fig. 2.4.4(b). So is r_0. The entire small signal equivalent circuit of the amplifier is shown in Fig.2.4-6(b).



(a) An amplifier circuit (b) The small signal equivalent circuit (c) The small signal equivalent circuit further simplified

Fig. 2.4-6 The small signal equivalent circuit of an amplifier circuit

From Fig. 2.4-6(c), we can see that the current will flow through the parallel connection of R_L and r_0, which is expressed as $Z = R_L // r_0$. The value of Z can be found as follows:

$$\frac{1}{Z} = \frac{1}{R_L} + \frac{1}{r_0}$$

$$Z = \frac{R_L r_0}{R_L + r_0}$$

$$\begin{aligned} v_{out} &= -g_m v_{in} (R_L \,//\, r_0) \\ &= -g_m v_{in} \frac{R_L r_0}{R_L + r_0} \end{aligned} \qquad (2.4\text{-}3)$$

Note that the polarity of v_{out} is opposite to that of v_{in}, as expected by examining Fig. 2.4-2. The meaning of the opposition of polarity is illustrated in Fig. 2.4-7.

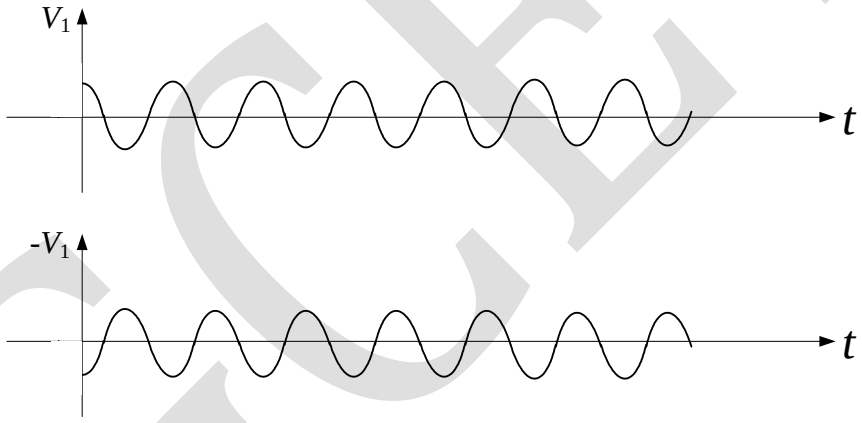


Fig. 2.4-7 The meaning of polarity of AC signals

Let us note that r_0 is usually much larger than R_L because in reality, the I-V curves of a transistor are rather flat and a flat I-V curve produces a large r_0. On the other hand, as we pointed out before, R_L cannot be too large because a large R_L will drive the transistor into the non-saturation region. When a large resistor is in parallel with another resistor, it can be ignored. Thus, r_0 is usually ignored and we have

$$v_{out} = -g_m R_L v_{in} \qquad (2.4\text{-}4)$$

We denote the gain of the amplifier by A_v. Then

$$A_v = \frac{v_{out}}{v_{in}} = -g_m R_L \qquad (2.4\text{-}5)$$

That a large R_L will produce a better amplifier can also be seen by the DC analysis. The reader should go back to Section 2.2 again. Take a look at the figures from Fig. 2.2-2 to Fig. 2.2-5. As seen in these figures, we can see that a large R_L will produce a sharp input-output relationship and thus a high gain. Of course, it must be under the condition that the load will not drive the transistor out of saturation.

In the above sections, we only talked about NMOS amplifiers. The same discussion can be used to explain how a PMOS amplifier works. A typical PMOS amplifier is shown in Fig. 2.4-8.

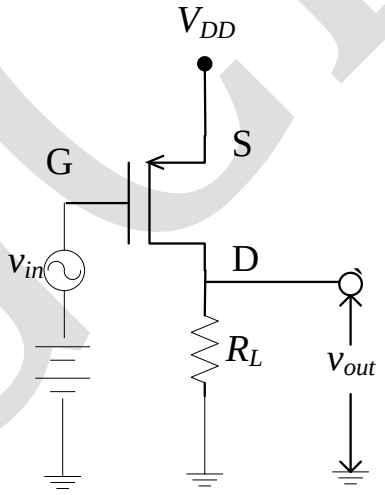


Fig. 2.4-8 A PMOS amplifier

We pointed out before that R_L cannot be too small. We now will give more interpretation of r_0. Let us consider Equation (2.4-3) which is displaced again below::

$$v_{out} = -g_m v_{in} \frac{R_L r_0}{R_L + r_0}$$

We may rewrite the above equation as follows:

$$v_{out} = -g_m v_{in} \frac{R_L}{\frac{R_L}{r_0} + 1} \qquad (2.4\text{-}6)$$

From Equation (2.4-6), we can see that the larger r_0 is, the larger v_{out} is. It can also be seen that a small r_0 will produce a very small v_{out}. Let us consider Fig. 2.4-9.

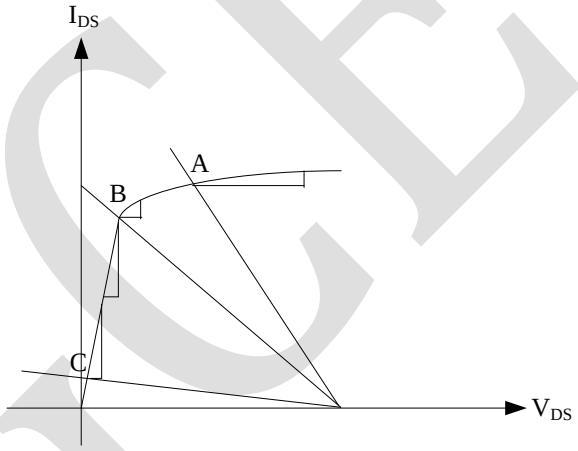


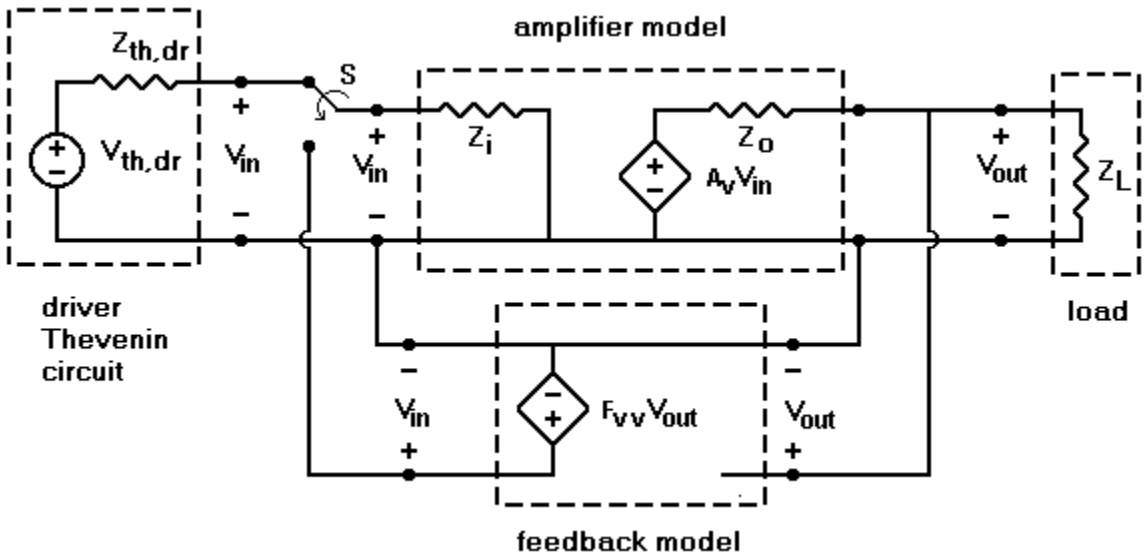
Fig. 2.4-9 A further interpretation of r_0

For Location A in Fig. 2.4-9, r_0 is large. If R_L is not too small, then Location A is suitable to be the operating point of an amplifier. For Location C in Fig. 2.4-9, r_0 is small and it is not suitable to be the operating point of an amplifier. If a circuit has such an operating point, it will not be an amplifier because the gain may be even smaller than 1. In other words, v_{out} may be smaller than v_{in}. As for Location *B*, we can see that r_0 changes from small to large and we can expect distortion to occur.

Sinusoidal Oscillators

Here we consider the principles of oscillators that produce approximately sinusoidal waveforms. (Other oscillators, such as multivibrators, operate somewhat differently.) Because the waveforms are sinusoidal, we use phasor analysis.

A sinusoidal oscillator ordinarily consists of an amplifier and a feedback network. Let's consider the following idealized configuration to begin understanding the operation of such oscillators.



We begin consideration of sinusoidal oscillators by conducting a somewhat artificial thought experiment with this configuration. Suppose that initially, as shown in the figure, the switch, *S*, connects the input of the amplifier is connected to the driver. Suppose, furthermore, that the complex constant, $\mathbf{F}_{vv}$ in the feedback network is adjusted (designed) to make the output of the feedback network exactly equal $\mathbf{V}_{in}$, the input voltage provided by the driver circuit. Then suppose that, instantaneously (actually, in a time negligible in comparison to the period of the sinusoids), the switch *S* disconnects the driver circuit from the input of the amplifier and immediately connects the identical voltage, $\mathbf{V}_{in}$, supplied by the feedback network to the input of the amplifier. A circuit, of course, cannot distinguish between two identical voltages and, therefore, the amplifier continues to behave as before. Specifically, it continues to produce a sinusoidal output. Now, however, it produces the sinusoidal output without connection to a driver. The amplifier is now self-driven, or self-excited, and functions as an oscillator.

We now analyze the behavior of the amplifier when it is connected to produce self-excited oscillations to develop a consistency condition that must be satisfied if such operation is to be possible. First, we note that the output voltage of the amplifier can be written in terms of the input voltage, $\mathbf{V}_{in}$:

$$\mathbf{V}_{out} = \frac{\mathbf{Z}_L}{\mathbf{Z}_L + \mathbf{Z}_o} \mathbf{A}_v \mathbf{V}_{in} \equiv \mathbf{A}\mathbf{V}_{in}$$

where we have written the gain, $\mathbf{A}$, of the amplifier, under load, as

$$\mathbf{A} \equiv \frac{\mathbf{Z}_L}{\mathbf{Z}_L + \mathbf{Z}_o} \mathbf{A}_v$$

But the output of the feedback network is $\mathbf{F}_{vv}\mathbf{V}_{out}$ where $\mathbf{F}_{vv}$ has been chosen so that

$$\mathbf{F}_{vv}\mathbf{V}_{out} = \mathbf{V}_{in}$$

If we substitute this result into our earlier result for $\mathbf{V}_{out}$, we find

$$\mathbf{V}_{out} = \mathbf{A}\mathbf{V}_{in} = \mathbf{A}\mathbf{F}_{vv}\mathbf{V}_{out}$$

or

$$\left(1 - \mathbf{A}\mathbf{F}_{vv}\right)\mathbf{V}_{out} = 0$$

Of course, $\mathbf{V}_{out} \neq 0$ for a useful oscillator so we must have

$$\mathbf{A}\mathbf{F}_{vv} = 1$$

Although it is usually summarized as requiring the complex loop gain to be unity as a condition of oscillation, let's examine this condition, known as the Barkhausen condition for oscillation, to gain a better understanding of what it means. To begin with, $\mathbf{A}$ and $\mathbf{F}_{vv}$ are complex numbers that can be written in polar form:

$$\mathbf{A} = \left|\mathbf{A}\right| e^{j\phi}$$

$$\mathbf{F}_{vv} = \left|\mathbf{F}_{vv}\right| e^{j\theta}$$

Thus, the Barkhausen condition can be written as

$$\mathbf{A}\mathbf{F}_{vv} = \left|\mathbf{A}\right| e^{j\phi} \left|\mathbf{F}_{vv}\right| e^{j\theta} = \left|\mathbf{A}\right|\left|\mathbf{F}_{vv}\right| e^{j(\phi+\theta)} = 1$$

or

$$\left|\mathbf{A}\right|\left|\mathbf{F}_{vv}\right| e^{j(\phi+\theta)} = 1$$

This equation, being complex, gives two real equations, one from the magnitude and one from the angle:

Magnitude: $|\mathbf{A}||\mathbf{F}_{vv}|=1$

Angle: $\phi+\theta=n2\pi, \quad n=0, \pm1, \pm2, ...$

The magnitude portion of the Barkhausen condition requires a signal that enters the amplifier and undergoes amplification by some factor to be attenuated by the same factor by the feedback network before the signal reappears at the input to the amplifier. The magnitude condition therefore ensures that the amplitude of oscillation remains constant over time. If it were true that $|\mathbf{A}||\mathbf{F}_{vv}|<1$, then the amplitude of the oscillations would gradually decrease each time the signal passed around the loop through the amplifier and the feedback network. Similarly, if it were true that $|\mathbf{A}||\mathbf{F}_{vv}|>1$, then the amplitude of the oscillations would gradually increase each time the signal passed around the loop through the amplifier and the feedback network. Only if $|\mathbf{A}||\mathbf{F}_{vv}|=1$ does the amplitude of the oscillations remain steady.

The angle portion of the Barkhausen condition requires that the feedback network complement any phase shift experienced by a signal when it enters the amplifier and undergoes amplification so that the total phase shift around the signal loop through the amplifier and the feedback network totals to 0, or to what amounts to the same thing, an integral multiple of 2π. Without this condition, signals would interfere destructively as they travel around the signal loop and oscillation would not persist because of the lack of reinforcement. Because the phase shift around the loop usually depends on frequency, the angle part of the Barkhausen condition usually determines the frequency at which oscillation is possible. In principle, the angle condition can be satisfied by more than one frequency. In laser feedback oscillators (partially reflecting mirrors provide the feedback), indeed, the angle part of the Barkhausen condition is often satisfied by several closely spaded, but distinct, frequencies. In electronic feedback oscillators, however, the circuit usually can satisfy the angle part of the Barkhausen condition only for a single frequency.

Although the Barkhausen condition is useful for understanding basic conditions for oscillation, the model we used to derive it gives an incomplete picture of how practical oscillators operate. For one thing, it suggests that we need a signal source to start up an oscillator. That is, it seems that we need an oscillator to make an oscillator. Such a circumstance would present, of course, a very inconvenient version of the chicken-and-the-egg dilemma. Second, the model suggests that the amplitude of the oscillations can occur at any amplitude, the amplitude apparently being determined by the amplitude at which the amplifier was operating when it was switched to self-excitation. Practical oscillators, in contrast, start by themselves when we flip on a switch, and a particular oscillator always gives approximately the same output amplitude unless we take specific action to adjust it in some way.

Let's first consider the process through which practical oscillators start themselves. The key to understanding the self-starting process is to realize that in any practical circuit, a variety of processes produce noise voltages and currents throughout the circuit. Some of the noise, called

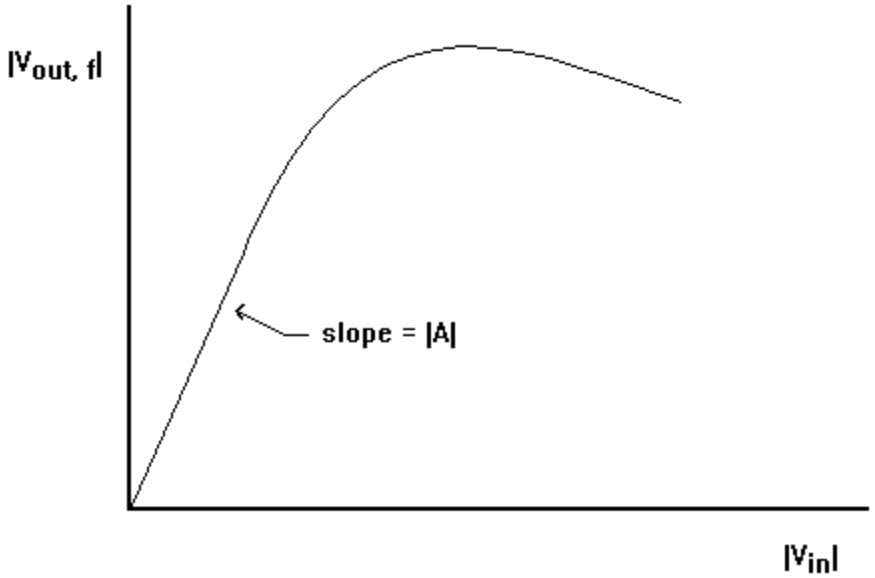
Johnson noise, is the result of the tiny electric fields produced by the random thermal motion of electrons in the components. Other noise results during current flow because of the discrete charge on electrons, the charge carriers. This noise is analogous to the acoustic noise that results from the dumping a shovel-full of marbles onto a concrete sidewalk, in comparison to that from dumping a shovel-full of sand on the same sidewalk. The lumpiness of the mass of the marbles produces more noise than the less lumpy grains of sand. The lumpiness of the charge on the electrons leads to electrical noise, called *shot noise*, as they carry electrical current. Transient voltages and currents produced during start-up by power supplies and other circuits also can produce noise in the circuit. In laser feedback oscillators, the noise to initiate oscillations is provided by spontaneous emission of photons. Amplification in lasers occurs through the process of stimulated emission of photons.

Whatever the source, noise signals can be counted upon to provide a small frequency component at any frequency for which the Barkhausen criterion is satisfied. Oscillation begins, therefore, as this frequency component begins to loop through the amplifier and the feedback network. The difficulty, of course, is that the amplitude of the oscillations is extremely small because the noise amplitude at any particular frequency is likely to be measured in microvolts. In practice, therefore, we design the oscillator so that loop gain, $|\mathbf{A}||\mathbf{F}_{vv}|$, is slightly greater than one:

$$|\mathbf{A}||\mathbf{F}_{vv}| > 1$$

With the loop gain slightly greater than one, the small noise component at the oscillator frequency is amplified slightly each time it circulates around the loop through the amplifier and the feedback network, and hence gradually builds to useful amplitude. A problem would occur if the amplitude continued to build toward infinite amplitude as the signal continued to circulate around the loop. Our intuition tells us, of course, that the amplitude, in fact, is unlikely to exceed some fraction of the power supply voltage (without a step-up transformer or some other special trick), but more careful consideration of how the amplitude is limited in practical oscillators provides us with some useful additional insight.

Initially, let's consider the amplifier by itself, without the feedback network. Suppose that we drive the amplifier with a sinusoidal generator whose frequency is the same as that of the oscillator in which the amplifier is to be used. With the generator, suppose we apply sinusoids of increasing amplitude to the amplifier input and observe its output with an oscilloscope. For sufficiently large inputs, the output becomes increasingly distorted as the amplitude of the driving sinusoid becomes larger. For large enough inputs, we expect the positive and negative peaks of the output sinusoids to become clipped so that the output might even resemble a square wave more than a sinusoid. Suppose we then repeat the experiment but observe the oscillator output with a tuned voltmeter set to measure the sinusoidal component of the output signal at the fundamental oscillator frequency, the only frequency useful for maintaining self-excited oscillations when the amplifier is combined with the feedback circuit. Then, we would measure an input/output characteristic curve for the amplifier at the fundamental oscillator frequency something like that shown in the following sketch.



From the curve above, note that, at low levels of input amplitude, $|\mathbf{V}_{in}|$, the output amplitude, $|\mathbf{V}_{out,\,f}|$, of the sinusoidal component at the fundamental frequency increases in direct proportion to the input amplitude. At sufficiently high output levels, however, note that a given increment in input amplitude produces a diminishing increase in the output amplitude (at the fundamental frequency). Physically, as the output becomes increasingly distorted at larger amplitudes, harmonic components with frequencies at multiples of the fundamental frequency necessarily increase in amplitude. Because the total amplitude is limited to some fraction of the power supply voltage, the sinusoidal component at the fundamental frequency begins to grow more slowly as the input amplitude increases and causes the amplitude of the distortion components to increase, as well. Thus, the amplitude of the component of the output at the fundamental frequency eventually must decrease as the input amplitude increases to accommodate the growing harmonic terms that accompany the rapidly worsening distortion. Effectively, the magnitude of the voltage gain, $|\mathbf{A}|$, for the fundamental frequency decreases at large amplitudes.

Now let's reconsider the amplifier in its oscillator environment, that is, with the feedback network designed so that $|\mathbf{A}||\mathbf{F}_{vv}| > 1$. As the oscillations build up from noise and increase to larger and larger amplitudes, they eventually reach amplitudes at which the magnitude of the voltage gain, $|\mathbf{A}|$, begins to decrease. As a consequence, the loop gain, $|\mathbf{A}||\mathbf{F}_{vv}|$, begins to decrease. The amplitude of the oscillations grows until the decreasing $|\mathbf{A}|$ reduces the loop gain, $|\mathbf{A}||\mathbf{F}_{vv}|$, to unity:

$$|\mathbf{A}||\mathbf{F}_{vv}| = 1$$

At that point, the oscillations cease growing and their amplitude becomes stable, at least as long as the gain characteristic of the amplifier shown in the curve above do not change.

In summary, the small signal loop gain in practical amplifiers is chosen so that $|\mathbf{A}||\mathbf{F}_{vv}| > 1$ and oscillations grow from small noise components at the oscillator frequency. The output climbs along the input/output characteristic curve of the amplifier at the fundamental frequency until the voltage gain drops enough to make $|\mathbf{A}||\mathbf{F}_{vv}| = 1$, at which point the oscillator amplitude stops growing and maintains a steady level. The amplifier input/output characteristic curve therefore explains why practical oscillators operate at approximately the same amplitude each time we turn them on. Note designers sometimes add nonlinearities, voltage-limiting circuits with diodes, for example, to gain more direct control of the oscillator amplitude.

The analysis of oscillator operation based on the input/output characteristic of the amplifier at the fundamental frequency can help illuminate one more aspect of the operation of practical sinusoidal oscillators: distortion in the output waveform. From the discussion above, it is clear that the higher the oscillations climb along the input/output characteristic curve, the more distortion in the output worsens. In addition, it is clear that the more the loop gain, $|\mathbf{A}||\mathbf{F}_{vv}|$, exceeds unity at small amplitudes, the higher the oscillations climb along the curve, and the more distorted the output will become, before the amplitude of the oscillations stabilizes. Thus, it is clear that, in the design process, $|\mathbf{A}||\mathbf{F}_{vv}|$ should not be chosen to exceed unity very much, even at small signals. On the other hand, if $|\mathbf{A}||\mathbf{F}_{vv}|$ is chosen too close to unity in an effort to reduce distortion, then even small changes in the amplification characteristics at some later time can preclude oscillation if they cause the loop gain, $|\mathbf{A}||\mathbf{F}_{vv}|$, to drop below unity. Such changes can easily be caused by, for example, changes in temperature or aging of components. The designer must therefore choose a compromise value of $|\mathbf{A}||\mathbf{F}_{vv}|$ to realize low distortion, but reliable operation, as well. If the oscillator is to operate at a single frequency, it may be possible to have our cake and eat it too by choosing the value of $|\mathbf{A}||\mathbf{F}_{vv}|$ well above unity to achieve reliable operation and then purifying the oscillator output with a tuned filter, such as an LC resonant circuit. This solution is not very convenient if the oscillator must operate over a wide range of frequencies, however, because a band pass filter with a wide tuning range can be difficult to realize in practice.

As a final perspective on the Barkhausen condition, we note that when

$$\mathbf{A}\mathbf{F}_{vv} = 1$$

or

$$\frac{\mathbf{Z}_L}{\mathbf{Z}_L + \mathbf{Z}_o}\mathbf{A}_v\mathbf{F}_{vv} = 1$$

then our earlier result for the voltage gain, $\mathbf{G}_v$, with feedback,

$$\mathbf{G}_v = \frac{\mathbf{A}_v}{1 - \mathbf{A}_v\mathbf{F}_{vv}} \left\{ \frac{\mathbf{Z}_i + \dfrac{\mathbf{Z}_{th,dr}}{\left[1 - \dfrac{\mathbf{Z}_L}{\mathbf{Z}_o + \mathbf{Z}_L}\mathbf{A}_v\mathbf{F}_{vv}\right]}}{\mathbf{Z}_i + \dfrac{\mathbf{Z}_{th,dr}}{\left[1 - \mathbf{A}_v\mathbf{F}_{vv}\right]}} \right\}$$

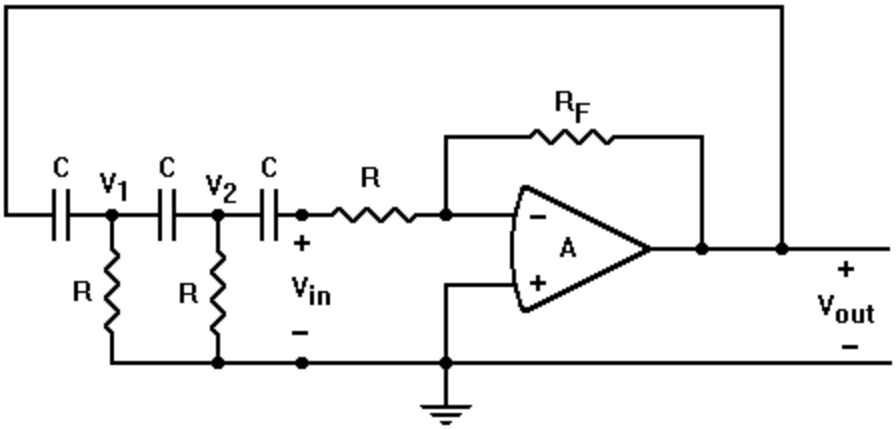
is infinite because the denominator in the numerator of the curly brackets is zero. In a naïve sense, then, we can say that the gain with feedback becomes infinite when the Barkhausen criterion is satisfied. The naïve perspective, then, is that oscillation corresponds to infinite gain with feedback.

This perspective is not particularly useful, except that it emphasizes that the feedback in sinusoidal oscillators is positive and, thereby, increases the gain of the amplifier instead of decreasing it, as negative feedback does. It is interesting to note, however, that positive feedback need not produce oscillations. If the feedback is positive, but $|\mathbf{A}||\mathbf{F}_{vv}| < 1$, then oscillations die out and are not sustained. In this regime, the gain of the amplifier can be increased considerably by positive feedback. Historically, Edwin H. Armstrong, the person who first understood the importance of DeForest's vacuum triode as a dependent or controlled source, used positive feedback to obtain more gain from a single, costly, vacuum triode in a high frequency amplifier before Black applied negative feedback to audio amplifiers. As vacuum triodes became more readily available at reasonable cost, however, the use of positive feedback to obtain increased gain fell out of favor because the increased gain it produced was accompanied by enhanced noise in the output, in much the same way that the decreased gain produced by negative feedback was accompanied by reduced noise in the amplifier output. In practice, you got better results at a reasonable cost by using amplifiers with negative feedback, even though they required more vacuum triodes than would be necessary with positive feedback.

We now analyze a variety of sinusoidal oscillator circuits in detail to determine the frequency of possible oscillation and the condition on circuit components necessary to achieve slightly more than unity loop gain and, thereby, useful oscillations.

Phase shift Oscillator

We begin our consideration of practical oscillators with the phase shift oscillator, one that conforms fairly closely to our idealized model of sinusoidal oscillators.



The phase shift oscillator satisfies Barkhausen condition with an angle of 2π. The inverting amplifier provides a phase shift of π. The three identical RC sections (recall that the inverting input to the operational amplifier is a virtual ground so that $\mathbf{V}_{-} \approx 0$) each provide an additional phase shift of $\pi/3$ at the frequency of oscillation so that the phase shift around the loop totals to 2π.

We begin the analysis by using the usual result for an inverting opamp configuration to express the output voltage, $\mathbf{V}_{out}$, in terms of the input voltage, $\mathbf{V}_{in}$, to the inverting amplifier:

$$\mathbf{V}_{out} = -\frac{R_F}{R}\mathbf{V}_{in} = -A\mathbf{V}_{in}$$

where

$$A \equiv \frac{R_F}{R}$$

Next, we write node equations to find the output of the feedback network in terms of the input to the feedback network. Oddly enough, the figure shows that the input to the feedback network is $\mathbf{V}_{out}$ and that the output of the feedback network is $\mathbf{V}_{in}$. To achieve a modest increase in notational simplicity, we use Laplace transform notation, although we will neglect transients and eventually substitute $s = j\omega$ and specialize to phasor analysis because we are interested only in the steady-state sinusoidal behavior of the circuit.

(1) $$\left[V_1(s) - V_{out}(s)\right]Cs + \frac{V_1(s)}{R} + \left[V_1(s) - V_2(s)\right]Cs = 0$$

(2) $$\left[V_2(s) - V_1(s)\right]Cs + \frac{V_2(s)}{R} + \left[V_2(s) - V_{in}(s)\right]Cs = 0$$

(3) $$\left[V_{in}(s) - V_2(s)\right]Cs + \frac{V_{in}(s)}{R} = 0$$

Collecting terms, we find:

$$(1)' \qquad \left[2Cs + \frac{1}{R}\right]V_1(s) + [-Cs]V_2(s) + [0]V_{in}(s) = sC\,V_{out}(s)$$

$$(2)' \qquad [-Cs]V_1(s) + \left[2Cs + \frac{1}{R}\right]V_2(s) + [-Cs]V_{in}(s) = 0$$

$$(3)' \qquad [0]V_1(s) + [-Cs]V_2(s) + \left[Cs + \frac{1}{R}\right]V_{in}(s) = 0$$

In matrix form,

$$\begin{bmatrix} 2Cs+\frac{1}{R} & -Cs & 0 \\ -Cs & 2Cs+\frac{1}{R} & -Cs \\ 0 & -Cs & Cs+\frac{1}{R} \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \\ V_{in}(s) \end{bmatrix} = \begin{bmatrix} sC\,V_{out}(s) \\ 0 \\ 0 \end{bmatrix}$$

We calculate Cramer's delta as a step towards calculating the output of the feedback network, $V_{in}(s)$, in terms of the input to the feedback network, $V_{out}(s)$.

$$\Delta = \begin{vmatrix} 2Cs+\frac{1}{R} & -Cs & 0 \\ -Cs & 2Cs+\frac{1}{R} & -Cs \\ 0 & -Cs & Cs+\frac{1}{R} \end{vmatrix}$$

$$\Delta = \left(2Cs+\frac{1}{R}\right)\begin{vmatrix} 2Cs+\frac{1}{R} & -Cs \\ -Cs & Cs+\frac{1}{R} \end{vmatrix} + Cs\begin{vmatrix} -Cs & 0 \\ -Cs & Cs+\frac{1}{R} \end{vmatrix}$$

$$\Delta = \left(2Cs+\frac{1}{R}\right)\left[\left(2Cs+\frac{1}{R}\right)\left(Cs+\frac{1}{R}\right) - (-Cs)^2\right] + Cs\left[-Cs\left(Cs+\frac{1}{R}\right)\right]$$

$$\Delta = \left(2Cs+\frac{1}{R}\right)\left[2(Cs)^2 + \frac{3}{R}Cs + \frac{1}{R^2} - (Cs)^2\right] - (Cs)^3 - \frac{(Cs)^2}{R}$$

$$\Delta = 2(Cs)^3 + \frac{6}{R}(Cs)^2 + \frac{2}{R^2}(Cs) + \frac{1}{R}(Cs)^2 + \frac{3}{R^2}(Cs) + \frac{1}{R^3} - (Cs)^3 - \frac{1}{R}(Cs)^2$$

$$\Delta = (Cs)^3 + \frac{6}{R}(Cs)^2 + \frac{5}{R^2}(Cs) + \frac{1}{R^3}$$

We now use this result in Cramer's rule to solve our set of equations for $V_{in}(s)$ in terms of $V_{out}(s)$.

$$V_{in}(s) = \frac{1}{\Delta}\begin{vmatrix} 2Cs+\frac{1}{R} & -Cs & sCV_{out}(s) \\ -Cs & 2Cs+\frac{1}{R} & 0 \\ 0 & -Cs & 0 \end{vmatrix}$$

$$V_{in}(s) = sCV_{out}(s)\frac{1}{\Delta}\begin{vmatrix} -Cs & 2Cs+\frac{1}{R} \\ 0 & -Cs \end{vmatrix}$$

$$V_{in}(s) = \frac{(Cs)^3}{(Cs)^3 + \frac{6}{R}(Cs)^2 + \frac{5}{R^2}(Cs) + \frac{1}{R^3}}V_{out}(s)$$

$$V_{in}(s) = \frac{s^3}{s^3 + \frac{6}{(RC)}s^2 + \frac{5}{(RC)^2}s + \frac{1}{(RC)^3}}V_{out}(s)$$

For an alternative solution with MATLAB, enter the following commands:

```
syms s R C V1 V2 Vin V Vout


A=[2*C*s+1/R -C*s 0; -C*s 2*C*s+1/R -C*s; 0 -C*s C*s+1/R];

b=[s*C*Vout; 0; 0];

V=A\b;

Vin=V(3)
```

The result is:

```
Vin = C^3*s^3*R^3*Vout/(C^3*s^3*R^3+6*C^2*s^2*R^2+5*C*s*R+1)
```

That is,

$$V_{in}(s) = \frac{C^3 s R^3}{C^3 s^3 R^3 + 6 C^2 s^2 R^2 + 5Cs + 1} V_{out}(s)$$

$$V_{in}(s) = \frac{s^3}{s^3 + \frac{6}{(RC)} s^2 + \frac{5}{(RC)^2} Cs + \frac{1}{(RC)^3}} V_{out}(s)$$

This expression, recall, gives the output of the feedback network, $V_{in}(s)$, in terms of the input to the feedback network, $V_{out}(s)$. Recall, also, that in phasor notation, the output of the amplifier, $\mathbf{V}_{out}$, in terms of the input to the amplifier, $\mathbf{V}_{in}$, is given by

$$\mathbf{V}_{out} = -A\mathbf{V}_{in}$$

In Laplace transform notation, this equation becomes

$$V_{out}(s) = -AV_{in}(s)$$

If we eliminate $V_{in}(s)$ between the input/output equations for the amplifier and for the feedback network, we find:

$$-\frac{1}{A} V_{out}(s) = \frac{s^3}{s^3 + \frac{6}{(RC)} s^2 + \frac{5}{(RC)^2} s + \frac{1}{(RC)^3}} V_{out}(s)$$

Because $V_{out}(s) \neq 0$ if the oscillator is to provide useful output, we must require

$$1 = \frac{-As^3}{s^3 + \frac{6}{(RC)} s^2 + \frac{5}{(RC)^2} s + \frac{1}{(RC)^3}}$$

This required consistency condition is tantamount to the Barkhausen condition for oscillation.

$$s^3 + \frac{6}{(RC)} s^2 + \frac{5}{(RC)^2} s + \frac{1}{(RC)^3} = -As^3$$

$$(A+1)s^3 + \frac{6}{(RC)} s^2 + \frac{5}{(RC)^2} s + \frac{1}{(RC)^3} = 0$$

Because we are interested in the sinusoidal steady state, we specialize to phasor analysis by substituting $s = j\omega$:

$$-(A+1)\,j\omega^3 + \frac{6}{(RC)}(-\omega)^2 + \frac{5}{(RC)^2}\,j\omega + \frac{1}{(RC)^3} = 0$$

$$\left\{-\frac{6}{(RC)}\omega^2 + \frac{1}{(RC)^3} + j\omega\left[-(A+1)\omega^2 + \frac{5}{(RC)^2}\right]\right\} = 0$$

This complex equation is in rectangular form. We obtain two separate equations by setting the real and imaginary parts to zero, separately. First, let's set the real part of the equation to zero:

$$-\frac{6}{(RC)}\omega^2 + \frac{1}{(RC)^3} = 0$$

$$-6\omega^2 + \frac{1}{(RC)^2} = 0$$

$$\omega^2 = \frac{1}{6(RC)^2}$$

$$\omega = \frac{1}{\sqrt{6}RC}$$

Thus, the frequency of the possible oscillations is determined by the values of the components in the feedback network. Whether or not oscillations will actually occur depends upon whether or not the second equation we obtain from the equation above is satisfied. To obtain this equation, we set the imaginary part of the equation to zero:

$$-(A+1)\omega^2 + \frac{5}{(RC)^2} = 0$$

$$(A+1)\omega^2 = \frac{5}{(RC)^2}$$

But, of course, we have already discovered the only possible value of ω:

$$\omega = \frac{1}{\sqrt{6}RC}$$

If we use this value in our equation, we find:

$$(A+1)\frac{1}{6(RC)^2} = \frac{5}{(RC)^2}$$

$$(A+1) = 30$$

Thus, we require

$$A = 29$$

to realize a loop gain through the amplifier and the feedback network of unity. In a practical oscillator, of course, A should be larger so that the oscillations will build up from noise. Perhaps it should be chosen to lie in the low $30's$ to ensure reliable operation without too much distortion of the essentially sinusoidal output voltage. Recall that the gain-bandwidth product for a 741 operational amplifier is roughly $1 MHz$. If we were to use it to realize an inverting amplifier with a gain of 30-something, then the bandwidth of the resulting amplifier would be no more than about $30 kHz$. Thus, a 741 operational amplifier can be used to realize a phase shift oscillator in the audio range, but not much higher. A 2N3904 BJT, in contrast, has a gain-bandwidth product of several hundred MHz and could be used to realize an amplifier with a gain of 30-something with a much larger bandwidth. Some details of the feedback circuit would change, but the arrangement would be similar. Even if we use devices with larger gain-bandwidth product, the output Thevenin resistance of the amplifier limits the maximum frequency at which the phase shift oscillator is useful in practice. The impedance of the phase shift feedback network at the oscillation frequency should be much larger than the Thevenin output impedance so that the amplifier output will not be unduly loaded and so that our simple theory will apply. As a consequence, the minimum resistance of the resistors with value, R, in the phase shift feedback network typically cannot be less than about 1000Ω. The minimum value of the capacitors, C, must be much larger than stray or parasitic capacitances in the circuit and hence typically should be no smaller than about $1000 pF$. From the result

$$\omega = \frac{1}{\sqrt{6}RC}$$

we see, therefore, that phase shift oscillators are seldom useful at frequencies above $500 kHz$, regardless of the GBW of the active device in the amplifier. Note that it is inconvenient to change the frequency of phase shift oscillators because the values of a minimum of three resistors or three capacitors must be changed simultaneously.

Band Pass Oscillators

If the output of a band pass amplifier is fed back to its input, it may oscillate at a frequency within its pass band. If the pass band is narrow, the frequency will occur near the center frequency of the amplifier pass band. To the extent that the band pass filter is effective in attenuating signals with frequencies outside its pass band, it suppresses the harmonic content (distortion) in the output waveform that results as the oscillations grow to the point that they are

limited by nonlinearities in the amplifier. As a consequence of this harmonic suppression, band pass oscillators can provide more nearly sinusoidal outputs than other types of practical oscillators.

To consider the requirements for oscillation in detail, recall that for a second order band pass filter that

$$V_{out}(s)=T(s)V_{in}(s)$$

where

$$T(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{n_1 s}{s^2+\left(\frac{\omega_o}{Q}\right)s+\omega_o{}^2}$$

Suppose that we connect the output directly to the input so that

$$v_{out}(t)\equiv v_{in}(t)$$

Our feedback network in this case is thus a simple piece of wire. In the Laplace transform domain,

$$V_{out}(s)\equiv V_{in}(s)$$

so that

$$T(s)\equiv 1$$

This condition, tantamount to the Barkhausen condition, requires

$$T(s)=\frac{n_1 s}{s^2+\left(\frac{\omega_o}{Q}\right)s+\omega_o{}^2}=1$$

For the steady state sinusoidal case that describes the operation of the circuit after transients have died out, we substitute $s=j\omega$ and obtain

$$T(j\omega)=\frac{n_1(j\omega)}{(j\omega)^2+\left(\frac{\omega_o}{Q}\right)(j\omega)+\omega_o{}^2}=\frac{j\omega n_1}{-\omega^2+j\omega\left(\frac{\omega_o}{Q}\right)+\omega_o{}^2}=1$$

or

$$j\omega n_1 = -\omega^2 + j\omega\left(\frac{\omega_o}{Q}\right) + \omega_o{}^2$$

$$\omega^2 + j\omega\left(n_1 - \frac{\omega_o}{Q}\right) - \omega_o{}^2 = 0$$

This complex equation, of course, gives two real equations. The real part gives

$$\omega^2 - \omega_o{}^2 = 0$$

so that the frequency of oscillations, if any, must be

$$\omega = \omega_o$$

The imaginary part of the equation gives

$$j\omega\left(n_1 - \frac{\omega_o}{Q}\right) = 0$$

or

$$n_1 = \frac{\omega_o}{Q}$$

This equation is a requirement on the gain of the band pass amplfier.

As an example, recall the state variable filter circuit

which provides a band passed output of

$$V_{BP}(s) = \frac{\omega_o s}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o{}^2} V_{in}(s)$$

where

$$\omega_o = \frac{1}{RC}$$

$$Q = \frac{1}{3}\left(1 + \frac{R_F}{R}\right)$$

If we wait until after the transients die out, we can substitute $s = j\omega$ and set $\mathbf{V}_{BP} \equiv \mathbf{V}_{in}$ to obtain

$$1 = \frac{\omega_o (j\omega)}{(j\omega)^2 + \left(\frac{\omega_o}{Q}\right)(j\omega) + \omega_o^2}$$

or

$$1 = \frac{j\omega\,\omega_o}{\omega^2 + j\omega\left(\frac{\omega_o}{Q}\right) + \omega_o^2}$$

$$-\omega^2 - j\omega\,\omega_o\left(1 - \frac{1}{Q}\right) + \omega_o^2 = 0$$

The real part of the equation requires

$$\omega = \omega_o = \frac{1}{RC}$$

and the imaginary part requires

$$1 = Q = \frac{1}{3}\left(1 + \frac{R_F}{R}\right)$$

or

$$3 = \left(1 + \frac{R_F}{R}\right)$$

or

$$\frac{R_F}{R} = 2$$

$$R_F = 2R$$

Note that this requirement means that $1/3$ of the band passed output is fed back to the input. To make the loop gain slightly greater than unity so that the oscillations will build up from noise, we need to feed back a larger fraction of the band passed output. To achieve this result, note that we should choose, in practice, $R_F < 2R$.

We noted earlier that band pass oscillators offer the advantage of built-in harmonic suppression from its band pass filter to purify their output waveform. We note that the state variable circuit offers additional harmonic suppression if we take the output from the low pass output rather than from the band bass output. The state variable circuit has the disadvantage of greater power requirements than circuits with only one operational amplifier. With the operational amplifier state variable implementation, band pass filters are limited basically to the audio frequency range. Changing the frequency of oscillations in the state variable band pass oscillator requires changing the value of 2 capacitors simultaneously, only slightly more convenient that for the phase shift oscillator's 3 capacitors (or resistors).

Wien Bridge Oscillator

The Wien Bridge oscillator is a band pass oscillator that requires only one operational amplifier:

where

$$Z_1(s) = R + \frac{1}{sC}$$

$$Z_2(s) = R \left\| \frac{1}{sC} = \frac{R\frac{1}{sC}}{R + \frac{1}{sC}} \right.$$

With a minor abuse of conventional notation, we represent impedances in this figure by resistances. We assume that the amplifier is non-inverting and has infinite input impedance and a real gain of A at the frequency of oscillation. For specificity, we show an operational amplifier configuration for which we saw, earlier, the gain is

$$A = 1 + \frac{R_F}{R}$$

but so our results will be more generally applicable, we express our results in terms of the open circuit gain, A, which might be provided by a BJT or FET amplifier. As before, we assume that we are interested in the sinusoidal steady state response so that we can neglect transients.

We begin our analysis by writing the following node equation:

$$\frac{V_{in}(s) - V_{out}(s)}{Z_1(s)} + \frac{V_{in}(s)}{Z_2(s)} = 0$$

But

$$V_{out}(s) = AV_{in}(s)$$

Thus, we can write the node equation as

$$\frac{AV_{in}(s) - AV_{out}(s)}{Z_1(s)} + \frac{AV_{in}(s)}{Z_2(s)} = 0$$

$$\frac{V_{out}(s) - AV_{out}(s)}{Z_1(s)} + \frac{AV_{out}(s)}{Z_2(s)} = 0$$

$$\left\{\frac{1 - A}{Z_1(s)} + \frac{1}{Z_2(s)}\right\} V_{out}(s) = 0$$

Recall that

$$Z_1(s) = R + \frac{1}{sC}$$

$$Z_2(s) = R \left\| \frac{1}{sC} = \frac{R\frac{1}{sC}}{R + \frac{1}{sC}} \right.$$

Thus,

$$\left\{\frac{1 - A}{R + \frac{1}{sC}} + sC + \frac{1}{R}\right\} V_{out}(s) = 0$$

To investigate the sinusoidal steady state, we convert this equation to phasor notation by substituting $s = j\omega$:

$$\left\{\frac{1 - A}{R + \frac{1}{j\omega C}} + j\omega C + \frac{1}{R}\right\} \mathbf{V}_{out} = 0$$

Multiply through by $R + \frac{1}{j\omega C}$:

$$\left\{1 - A + \left(j\omega C + \frac{1}{R} \right)\left(R + \frac{1}{j\omega C} \right)\right\}\mathbf{V}_{out} = 0$$

$$\left\{1 - A + j\omega RC + 1 + 1 + \frac{1}{j\omega RC}\right\}\mathbf{V}_{out} = 0$$

$$\left\{3 - A + j\left(\omega RC - \frac{1}{\omega RC} \right)\right\}\mathbf{V}_{out} = 0$$

If the oscillator is to produce useful output, then $\mathbf{V}_{out} \neq 0$ and the curly brackets must be zero. The real and imaginary parts of the curly brackets must be zero independently. If we set the imaginary part to zero, we find:

$$j\left(\omega RC - \frac{1}{\omega RC} \right) = 0$$

or

$$\omega^2 = \frac{1}{(RC)^2}$$

Thus, the frequency of possible oscillation is given

$$\omega = \frac{1}{RC}$$

Note that if the amplification, A, is provided by a BJT or an FET, the frequency of oscillation can be extended beyond the audio range, just as with the phase shift oscillator. Because of the absence of the factor $\sqrt{6}$ in the denominator, however, the Wien Bridge oscillator can achieve more than twice the frequency of a phase shift oscillator, in practice.

By setting the real part of the equation to zero, we obtain:

$$A = 3$$

In practice, of course, we would choose A to be slightly larger so that the oscillations can build up from noise. One of the advantages of the Wien Bridge oscillator is that it requires only a modest gain from the amplifier.

Colpitts and Hartley Oscillators

The Colpitts and Hartley oscillators are band pass filter oscillators in which the band pass filters are LC resonant circuits. In the Colpitts oscillator, a capacitive voltage divider, which also serves as the capacitance part of the LC resonant circuit, feeds back a portion of the output back into the input. In the Hartley oscillator, an inductive voltage divider, which also serves as the inductance part of the LC resonant circuit, feeds back a portion of the output back into the input. With appropriate amplifiers, these configurations can oscillate at frequencies up to a few hundred megahertz, much higher than the configurations we have considered so far.

Because these two oscillator configurations are identical topologically, we can perform much of the analysis of them simultaneously by considering the following circuit:

With a minor abuse of conventional notation, we represent impedances in this figure by resistances. We assume that the amplifier is non-inverting and has infinite input impedance, a real gain of A at the frequency of oscillation and a Thevenin output resistance of R_o. For specificity, we show an operational amplifier configuration for which we saw, earlier, the gain is

$$A=1+\frac{R_F}{R}$$

but so our results will be more generally applicable, we express our results in terms of the open circuit gain, A, which might be provided by a BJT or FET amplifier that permits operation at high frequencies. As before, we assume that we are interested in the sinusoidal steady state response so that we can neglect transients.

Using Laplace transform notation, we have for a Colpitts oscillator that

$$Z_1(s)=\frac{1}{sC_1}$$

$$Z_2(s)=\frac{1}{sC_2}$$

$$Z_3(s)=sL$$

while for a Hartley oscillator,

$$Z_1(s)=sL_1$$

$$Z_2(s)=sL_1$$

$$Z_3(s) = \frac{1}{sC}$$

We can easily write node equations that hold for both oscillators:

$$(1) \qquad \frac{V_{in}(s) - V_{out}(s)}{Z_1(s)} + \frac{V_{in}(s)}{Z_2(s)} = 0$$

$$(2) \qquad \frac{V_{out}(s) - V_{in}(s)}{Z_1(s)} + \frac{V_{out}(s)}{Z_3(s)} + \frac{V_{out}(s) - AV_{in}(s)}{R_o} = 0$$

Collecting terms, we find:

$$(1)' \qquad V_{in}(s)\left[\frac{1}{Z_1(s)} + \frac{1}{Z_2(s)}\right] + V_{out}(s)\left[-\frac{1}{Z_1(s)}\right] = 0$$

$$(2)' \qquad V_{in}(s)\left[-\frac{1}{Z_1(s)} - \frac{A}{R_o}\right] + V_{out}(s)\left[\frac{1}{Z_1(s)} + \frac{1}{Z_3(s)} + \frac{1}{R_o}\right] = 0$$

From equation (1)', we find:

$$(1)'' \qquad V_{in}(s) = \frac{\frac{1}{Z_1(s)}}{\frac{1}{Z_1(s)} + \frac{1}{Z_2(s)}} V_{out}(s)$$

We substitute equation (1)'' into (2)':

$$\left\{\frac{\frac{1}{Z_1(s)}}{\frac{1}{Z_1(s)} + \frac{1}{Z_2(s)}}\left[-\frac{1}{Z_1(s)} - \frac{A}{R_o}\right] + \left[\frac{1}{Z_1(s)} + \frac{1}{Z_3(s)} + \frac{1}{R_o}\right]\right\} V_{out}(s) = 0$$

$$\left\{\frac{1}{Z_1(s)}\left(-\frac{\frac{1}{Z_1(s)}}{\frac{1}{Z_1(s)} + \frac{1}{Z_2(s)}} + 1\right) + \frac{\frac{1}{Z_1(s)}}{\frac{1}{Z_1(s)} + \frac{1}{Z_2(s)}}\left(-\frac{A}{R_o}\right) + \frac{1}{Z_3(s)} + \frac{1}{R_o}\right\} V_{out}(s) = 0$$

$$\left\{\frac{1}{Z_1(s)}\left(\frac{-\frac{1}{Z_1(s)}+\frac{1}{Z_1(s)}+\frac{1}{Z_2(s)}}{\frac{1}{Z_1(s)}+\frac{1}{Z_2(s)}}\right)+\frac{\frac{1}{Z_1(s)}}{\frac{1}{Z_1(s)}+\frac{1}{Z_2(s)}}\left(-\frac{A}{R_o}\right)+\frac{1}{Z_3(s)}+\frac{1}{R_o}\right\}V_{out}(s)=0$$

We divide through by $\dfrac{\frac{1}{Z_1(s)}}{\frac{1}{Z_1(s)}+\frac{1}{Z_2(s)}}$:

$$\left\{\frac{1}{Z_2(s)}-\frac{A}{R_o}+\frac{\frac{1}{Z_3(s)}+\frac{1}{R_o}}{\frac{1}{Z_1(s)}}\left(\frac{1}{Z_1(s)}+\frac{1}{Z_2(s)}\right)\right\}V_{out}(s)=0$$

$$\left\{\frac{1}{Z_2(s)}-\frac{A}{R_o}+\left(\frac{1}{Z_3(s)}+\frac{1}{R_o}\right)\left(1+\frac{Z_1(s)}{Z_2(s)}\right)\right\}V_{out}(s)=0$$

$$\left\{\frac{1}{Z_2(s)}+\left(1+\frac{Z_1(s)}{Z_2(s)}\right)\frac{1}{Z_3(s)}+\frac{1}{R_o}\left(-A+1+\frac{Z_1(s)}{Z_2(s)}\right)\right\}V_{out}(s)=0$$

We now specialize this equation for the Colpitts oscillator, for which, recall,

$$Z_1(s)=\frac{1}{sC_1}$$

$$Z_2(s)=\frac{1}{sC_2}$$

$$Z_3(s)=sL$$

From these results, we obtain the following equation for the Colpitts oscillator:

$$\left\{sC_2+\left(1+\frac{C_2}{C_1}\right)\frac{1}{sL}+\frac{1}{R_o}\left(-A+1+\frac{C_2}{C_1}\right)\right\}V_{out}(s)=0$$

To investigate the sinusoidal steady state, we convert this equation to phasor notation by substituting $s=j\omega$:

$$\left\{ j\omega C_2 \; + \left(1 + \frac{C_2}{C_1}\right)\frac{1}{j\omega L} + \frac{1}{R_o}\left(-A + 1 + \frac{C_2}{C_1}\right)\right\}\mathbf{V}_{out} \; = \; 0$$

If the oscillator is to produce useful output, then $\mathbf{V}_{out} \neq 0$ and the curly brackets must be zero. The real and imaginary parts of the curly brackets must be zero independently. If we set the imaginary part to zero, we find:

$$j\omega C_2 \; + \left(1 + \frac{C_2}{C_1}\right)\frac{1}{j\omega L} \; = \; 0$$

$$\omega C_2 \; - \left(1 + \frac{C_2}{C_1}\right)\frac{1}{\omega L} \; = \; 0$$

$$\omega^{\,2} \; = \left(\frac{1}{C_1} \; + \; \frac{1}{C_2}\right)\frac{1}{L}$$

Thus, the frequency of possible oscillation is given

$$\omega = \sqrt{\left(\frac{1}{C_1} \; + \; \frac{1}{C_2}\right)\frac{1}{L}}$$

Because C_1 and C_2 are connected in series, this frequency is simply the resonant frequency of the LC circuit, that is, the center of the pass band.

By setting the real part of the equation to zero, we obtain:

$$-A + 1 \; + \; \frac{C_2}{C_1} \; = \; 0$$

or

$$A = 1 \; + \; \frac{C_2}{C_1}$$

In practice, of course, we would choose A to be slightly larger so that the oscillations can build up from noise. Because the designer can set the ratio of C_1 and C_2 to a convenient value, the gain of the amplifier, A, need not be especially large, a potential advantage over the other circuits we have investigated so far. In practice, it is difficult to vary the frequency by changing the values of the capacitors because their ratio should remain constant. In practical variable frequency Colpitts oscillators, therefore, the frequency is sometimes varied by partially inserting and withdrawing a low-loss ferrite core located within an inductive winding. Notice that neither

the frequency nor the gain requirement for the Colpitts oscillator depend upon R_o, the output Thevenin resistance of the amplifier.

We can see more clearly the physical meaning of the equation that specifies the minimum amplitude if we write it as follows:

$$A = 1 + \frac{C_2}{C_1} = \frac{C_1 + C_2}{C_1}$$

or

$$1 = A\frac{C_1}{C_1 + C_2} = A\frac{\frac{1}{C_2}}{\frac{1}{C_1} + \frac{1}{C_2}} = A\frac{\frac{1}{j\omega C_2}}{\frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}}$$

The quantity $\frac{\frac{1}{j\omega C_2}}{\frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}}$ is the fraction of the output that is fed back into the input of the amplifier in a Colpitts oscillator. Thus, the real part of the equation simply requires that the loop gain through the amplifier and feedback network be unity. The imaginary part of the equation requires the phase shift around the loop to be a multiply of 2π.

For a Hartley oscillator, recall that

$$Z_1(s) = s L_1$$

$$Z_2(s) = s L_1$$

$$Z_3(s) = \frac{1}{sC}$$

Thus, the equation

$$\left\{\frac{1}{Z_2(s)} + \left(1 + \frac{Z_1(s)}{Z_2(s)}\right)\frac{1}{Z_3(s)} + \frac{1}{R_o}\left(-A + 1 + \frac{Z_1(s)}{Z_2(s)}\right)\right\}V_{out}(s) = 0$$

becomes

$$\left\{\frac{1}{sL_2} + \left(1 + \frac{L_1}{L_2}\right)Cs + \frac{1}{R_o}\left(-A + 1 + \frac{L_1}{L_2}\right)\right\}V_{out}(s) = 0$$

To investigate the sinusoidal steady state, we convert this equation to phasor notation by substituting $s = j\omega$:

$$\left\{ \frac{1}{j\omega L_2} + \left(1 + \frac{L_1}{L_2}\right) j\omega C + \frac{1}{R_o}\left(-A + 1 + \frac{L_1}{L_2}\right) \right\} \mathbf{V}_{out} = 0$$

If the oscillator is to produce useful output, then $\mathbf{V}_{out} \neq 0$ and the curly brackets must be zero. The real and imaginary parts of the curly brackets must be zero independently. If we set the imaginary part to zero, we find:

$$\frac{1}{j\omega L_2} + \left(1 + \frac{L_1}{L_2}\right) j\omega C = 0$$

$$-\frac{1}{\omega L_2} + \left(1 + \frac{L_1}{L_2}\right) \omega C = 0$$

$$-1 + \omega^2 C L_2 \left(1 + \frac{L_1}{L_2}\right) = 0$$

$$\omega^2 C\left(L_2 + L_1\right) = 1$$

Thus, the frequency of possible oscillation is given

$$\omega = \frac{1}{\sqrt{(L_1 + L_2)C}}$$

Because L_1 and L_2 are connected in series, this frequency is simply the resonant frequency of the LC circuit, that is, the center of the pass band.

By setting the real part of the equation to zero, we obtain:

$$-A + 1 + \frac{L_1}{L_2} = 0$$

or

$$A = 1 + \frac{L_1}{L_2}$$

In practice, of course, we would choose A to be slightly larger so that the oscillations can build up from noise. Because the designer can set the ratio of L_1 and L_2 to a convenient value, the

gain of the amplifier, A, need not be especially large, a potential advantage shared with the Colpitts oscillator. In practice, it is difficult to vary the frequency by changing the values of the inductors because their ratio should remain constant. In practical variable frequency Hartley oscillators, therefore, the frequency usually is varied by adjusting the capacitance, C.

We can see more clearly the physical meaning of the equation that specifies the minimum amplitude if we write it as follows:

$$A = 1 + \frac{L_1}{L_2} = \frac{L_1 + L_2}{L_2}$$

or

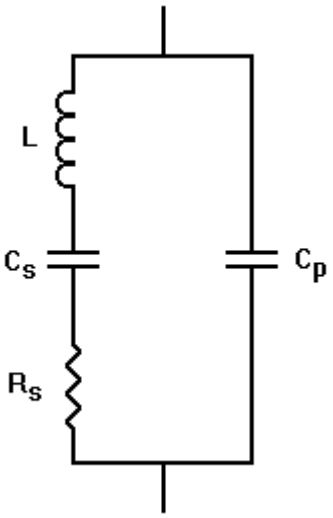
$$1 = A\frac{L_2}{L_1 + L_2} = A\frac{j\omega L_2}{j\omega L_1 + j\omega L_2}$$

The quantity $\frac{j\omega L_2}{j\omega L_1 + j\omega L_2}$ is the fraction of the output that is fed back into the input of the amplifier in a Hartley oscillator. Thus, the real part of the equation simply requires that the loop gain through the amplifier and feedback network be unity. The imaginary part of the equation requires the phase shift around the loop to be a multiply of 2π.

Piezoelectric Crystal Oscillators

When some materials are placed between conducting plates and subjected to mechanical compression, they produce an internal electric field that causes a voltage to appear between the conducting plates. A voltage also appears between the plates if the materials are subjected to mechanical tension, although the polarity of the voltage produced is opposite to that produced by compression. If the sample is subjected to neither compression nor tension, no voltage appears between the plates. Conversely, application of a voltage between the plates produces compression or tension in the material, depending on the polarity of the voltage applied. This electromechancial behavior is called the *piezoelectric effect*.

Excitation of high frequency mechanical vibrations in a small slab of a piezoelectric material, such as crystalline quartz, produces a damped oscillatory voltage across conducting electrodes placed on opposite faces of the material similar to that produced by an excited LC resonant circuit. Indeed, the electrical behavior of a small piece of piezoelectric material placed between conducting electrodes can be modeled by the following circuit:



where the upper and lower terminals connect to the conducting electrodes attached to opposite faces of the piezoelectric material. Given this equivalent circuit, it is not hard to show that a piezoelectric crystal can form the heart of a band pass filter, and hence, the basis of a band pass oscillator.

Although piezoelectric crystal oscillators can oscillate at frequencies as low as $10\,kHz$, they typically oscillate at frequencies between 1 and $10\,MHz$. Their frequency range can be extended to frequencies up to a few hundred megahertz by means of special tricks. Like Colpitts and Hartley oscillators, therefore, piezoelectric crystal oscillators can operate at much higher frequencies than the various RC oscillators that we considered earlier.

In addition to high frequency operation, piezoelectric crystal oscillators offer two main features, one recently important and one long important. The unrelenting trend toward miniaturization in contemporary electronics has made the capacitors and inductors required for high frequency band pass oscillators begin to seem huge and cumbersome. For typical frequencies of oscillation, a piezoelectric crystal in a practical oscillator will occupy less than $100\,mm^3$, hundreds of times less than the volume necessary for the coil and capacitor in Colpitts or Hartley oscillators. Since the early days of electronics, piezoelectric crystal oscillators have been known for offering incomparable frequency stability, a feature perhaps more important today than ever before.

A rather peculiar feature of piezoelectric crystal oscillators is that the crystal can vibrate mechanically not only at its fundamental frequency, but at harmonics of that frequency, as well. This phenomenon is analogous to the fact that a taut string can vibrate at multiples of the lowest possible frequency of oscillation. Oscillation at these *overtones* of the fundamental frequency permits oscillators with piezoelectric crystals of reasonable size to operate at frequencies up to a few hundred Mhz. In this respect, overtones provide a desirable feature. Overtone vibrations at harmonic frequencies, however, also mean that a piezoelectric crystal used as a band pass filter has pass bands at harmonics of the fundamental frequency as well as at the fundamental frequency itself. Consequently, harmonic suppression in a piezoelectric crystal band pass filter oscillator is not as effective as in Colpitts or Hartley oscillators. Therefore, it is usually necessary to pass the output of a piezoelectric crystal oscillator through an LC band pass filter to achieve

harmonic suppression comparable to the in Colpitts or Hartley oscillators. In practice, the pattern of resonant frequencies in piezoelectric crystals is actually even a little more complicated than we just described. The three-dimensional nature of the piezoelectric crystal permits it to vibrate at more than one "fundamental" frequency, as well as the harmonics of each one of these. Thus, piezoelectric crystals can exhibit resonant frequencies that are not obviously harmonically related.

Historically, the major disadvantage of piezoelectric oscillators was inflexibility: they operate at a single fixed frequency. Today, however, phase-locked loops and digital technology have liberated piezoelectric crystal oscillators from the severe limitation of single frequency operation and made them widely useful.

A typical quality factor, Q, (2π divided by the fraction of the oscillatory energy dissipated during each cycle of oscillation) for a piezoelectric crystal is a few hundred thousand, about 10,000 times larger than we can usually achieve with practical LC circuits. This high Q gives a piezoelectric band pass filter narrow bandwidth. Because

$$\Delta f = \frac{f_o}{Q}$$

the bandwidth, Δf, of a piezoelectric crystal filter with a center frequency, f_o, of $1 MHz$, for example, could be less than $10 Hz$, an impossible achievement for LC band pass filters, for which Q values of 10 or so are typical. In the equivalent circuit above, the inductor, L, may have values of a few $100 H$, the series capacitor, C_s, may have values of a few tenths of a femtofarad ($10^{-15} F$), and the series resistor, R_s, may have values of a few tens of $k\Omega$. The parallel capacitance, C_p, results mainly from the dielectric properties of the piezoelectric material between the conducting electrodes, often plated directly on the piezoelectric material. Its value is typically a few picofarads.

With these values in mind, let's look at the impedance, $Z(s)$, of the piezoelectric crystal.

$$Z(s) = \frac{1}{sC_p + \dfrac{1}{sL + \dfrac{1}{sC_s} + R_s}} = \frac{sL + \dfrac{1}{sC_s} + R_s}{1 + sC_p\left[sL + \dfrac{1}{sC_s} + R_s\right]}$$

$$Z(s) = \frac{s^2 LC_s + 1 + sC_s R_s}{sC_s + s^3 C_p C_s L + sC_p + s^2 C_p C_s R_s}$$

$$Z(s) = \frac{LC_s}{sC_p} \frac{s^2 + \frac{R_s}{L}s + \frac{1}{LC_s}}{\frac{C_s}{C_p} + s^2 C_s L + 1 + sC_s R_s}$$

$$Z(s) = \frac{1}{sC_p} \frac{s^2 + \frac{R_s}{L}s + \frac{1}{LC_s}}{\frac{1}{LC_p} + s^2 + \frac{1}{LC_s} + s\frac{R_s}{L}}$$

$$Z(s) = \frac{1}{sC_p} \frac{s^2 + \frac{R_s}{L}s + \frac{1}{LC_s}}{s^2 + \left(\frac{R_s}{L}\right)s + \frac{1}{L}\left(\frac{1}{C_p} + \frac{1}{C_s}\right)}$$

We are interested in the sinusoidal steady state response, so we substitute $s = j\omega$ and obtain

$$Z(j\omega) = \frac{1}{j\omega C_p} \frac{-\omega^2 + \frac{R_s}{L} j\omega + \omega_s^2}{-\omega^2 + \left(\frac{R_s}{L}\right) j\omega + \omega_p^2}$$

where

$$\omega_s = \frac{1}{\sqrt{LC_s}}$$

and

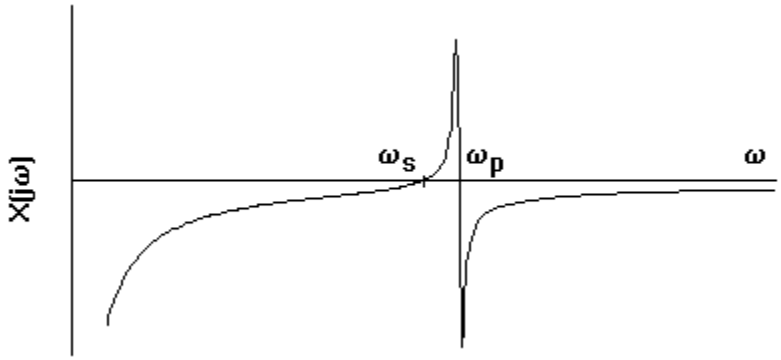
$$\omega_p = \sqrt{\frac{1}{L}\left(\frac{1}{C_p} + \frac{1}{C_s}\right)} \geq \omega_s$$

Because $C_p >> C_s$, note that ω_p is only the slightest bit larger than ω_s. Thus, we find

$$Z(j\omega) = -j\frac{1}{\omega C_p} \frac{\omega^2 - \omega_s^2 - j\omega\frac{R_s}{L}}{\omega^2 - \omega_p^2 - j\omega\left(\frac{R_s}{L}\right)} \equiv R(j\omega) + jX(j\omega)$$

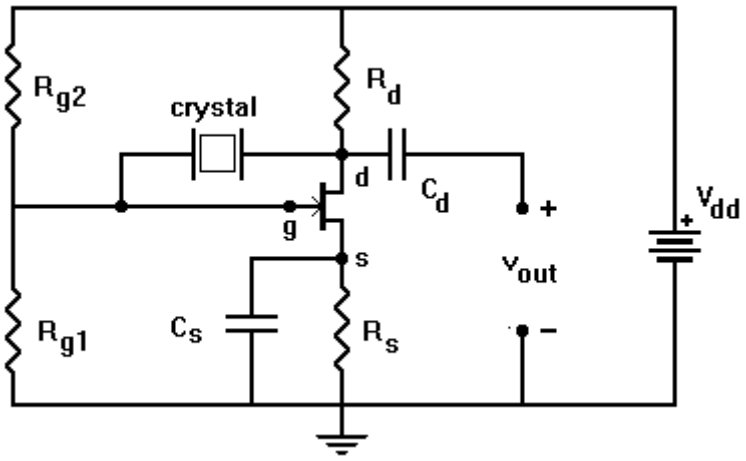
where $R(j\omega)$ is the resistance and $X(j\omega)$ is the reactance of the piezoelectric crystal at angular frequency ω and, recall, $\omega_p{}^2 > \omega_s{}^2$.

The dissipative resistance, $R(j\omega)$ is positive and shows a peak at a frequency between ω_s and ω_p, but is otherwise uninteresting for our present purposes. Here is a sketch of the reactance, $X(j\omega)$, of the piezoelectric crystal vs. frequency:



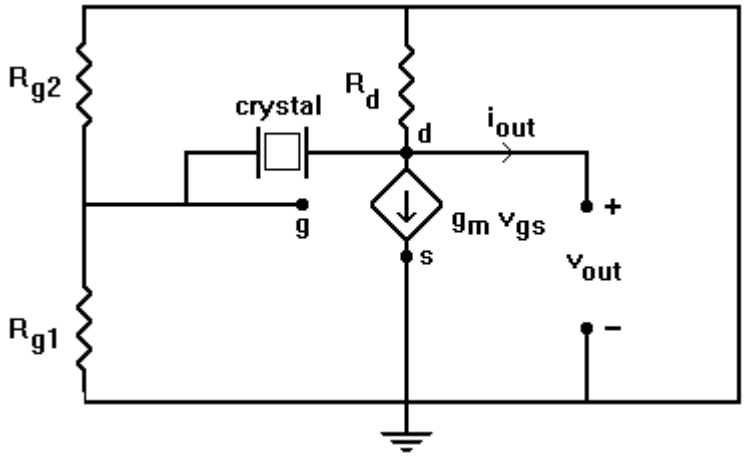
Note that the reactance, $X(j\omega)$, is positive only for frequencies, ω, in the range $\omega_s < \omega < \omega_p$. That is, for frequencies between ω_s and ω_p, the piezoelectric crystal behaves as an inductor. (Outside this range, it behaves as a capacitor.) Because ω_s and ω_p are nearly coincident, the crystal behaves as an inductor over only an extremely narrow range of frequencies. Because piezoelectric crystal oscillators are designed to rely on the effective inductance for their operation, the possible frequency of oscillation is limited to the extremely narrow frequency range over which the piezoelectric crystal behaves, indeed, as an inductor. Thus, the frequency of oscillation is necessarily extremely stable.

A simple example of a piezoelectric crystal oscillator is the Pierce oscillator. Consider the following FET realization:

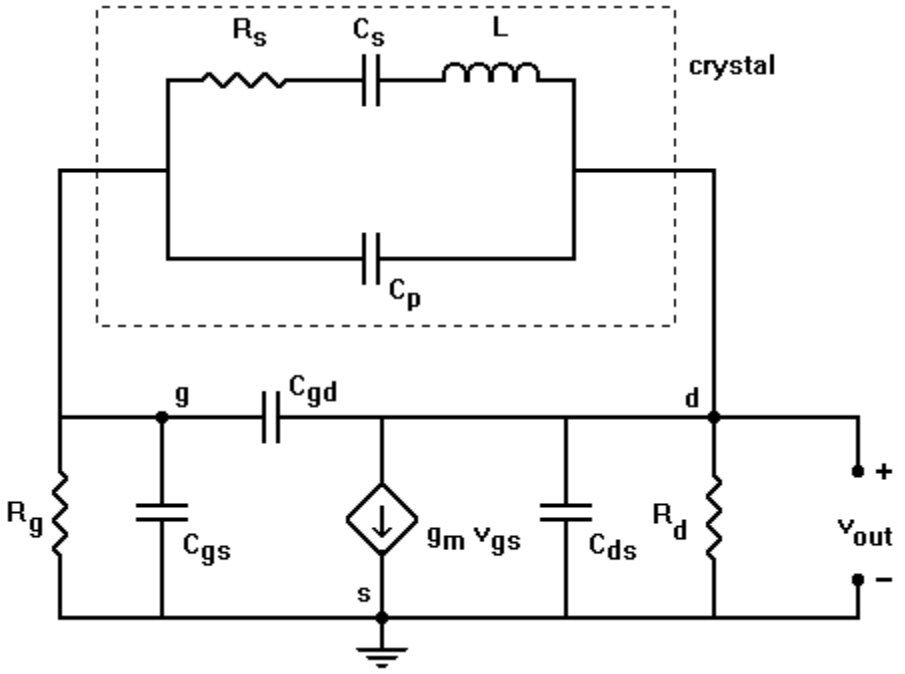


The popularity of this circuit is doubtless due to its apparent simplicity – it is only necessary to add a piezoelectric crystal to a fairly standard FET amplifier to form the Pierce oscillator. If the Pierce oscillator works, it is, indeed, an extremely simple oscillator. During the course of our analysis, however, we will discover that best operation is achieved if some additional components are added.

In the circuit above, the capacitor C_s is assumed to be chosen so that $\frac{1}{\omega C_s} << R_s$ at the frequency of oscillation. In this case, C_s can be considered to be a short circuit for signals. As a consequence, the negative feedback for signals that R_s otherwise would provide is eliminated and the voltage gain for the FET is higher than it would be without the presence of C_s. Note, however, that R_s still provides negative feedback necessary to achieve good bias stability. Similarly, we assume that C_d is chosen so that its reactance at the frequency of oscillation is small in comparison to the Thevenin output resistance of the amplifier, R_d: $\frac{1}{\omega C_d} << R_d$. Thus, C_d also behaves as a short circuit for signals. With these assumptions in mind, we can draw the following signal equivalent circuit for the Pierce oscillator circuit:



where g_m is the mutual transconductance of the FET and, for the moment, we have neglected to include the small parasitic capacitances associated with the FET so that the diagram is simpler. If we replace the piezoelectric crystal by the equivalent circuit that we considered before and add the parasitic capacitances associated with the FET, we obtain:



where $R_g \equiv R_{g1} \| R_{g2}$. Note that C_{gd}, the gate to drain parasitic capacitance of the FET, parallels C_p, the capacitance between the electrodes of the piezoelectric crystal. For $\omega_s < \omega < \omega_p$, the inductance of the piezoelectric crystal, together with the gate-to-source capacitance, C_{gs}, and the drain-to-source capacitance, C_{ds}, form a variation of the Colpitts oscillator configuration. The variation is that the junction of the capacitive voltage divider formed by C_{gs} and C_{ds} is connected to ground whereas the output of the feedback network is taken from the end of the inductor that is opposite to the end connected to the drain of the FET. At the LC resonant frequency, the effect of this variation is to reverse the sign of the voltage fed back to the input of the FET amplifier in comparison with the Colpitts configuration that we considered earlier. This sign reversal is equivalent to a phase shift of π that, in addition to the phase shift of π produced by the signal inversion in the FET, gives a loop phase shift of 2π, necessary to satisfy the phase part of the Barkhausen condition at resonance. Because C_{gs} and C_{ds} in practical devices are extremely small (picofards or smaller), the operation of the capacitive voltage divider can be unduly affected by stray capacitances external to the transistor package. As a consequence, it is usually prudent, as we will become clear during the course of the analysis, to place larger external capacitors in parallel with them to improve reliability of the oscillator performance.

To derive the Barkhausen conditions for the Pierce oscillator, we write node equations at the gate and drain terminals of the FET:

$$(1) \qquad V_{gs}(s)\left[\frac{1}{R_g} + sC_{gs}\right] + \frac{\left[V_{gs}(s) - V_{out}(s)\right]}{Z(s)} = 0$$

$$(2) \qquad V_{out}(s)\left[\frac{1}{R_d} + sC_{ds}\right] + \frac{\left[V_{out}(s) - V_{gs}(s)\right]}{Z(s)} + g_m V_{gs}(s) = 0$$

where, recall,

$$Z(s) = \frac{1}{sC_p}\frac{s^2 + \frac{R_s}{L}s + \omega_s^2}{s^2 + \frac{R_s}{L}s + \omega_p^2}$$

is the impedance of the piezoelectric crystal equivalent circuit. We rewrite equations (1) and equation (2) as a pair of pair of simultaneous linear algebraic equations with $V_{gs}(s)$ and $V_{out}(s)$ as unknowns:

$$(1)' \qquad V_{gs}(s)\left[\frac{1}{R_g} + sC_{gs} + \frac{1}{Z(s)}\right] - V_{out}(s)\left[\frac{1}{Z(s)}\right] = 0$$

$$(2)' \qquad V_{gs}(s)\left[g_m - \frac{1}{Z(s)}\right] + V_{out}(s)\left[\frac{1}{R_d} + sC_{ds} + \frac{1}{Z(s)}\right] = 0$$

From equation $(1)'$, we solve for $V_{gs}(s)$ in terms of $V_{out}(s)$:

$$V_{gs}(s) = \frac{\frac{1}{Z(s)}}{\frac{1}{R_g} + sC_{gs} + \frac{1}{Z(s)}}V_{out}(s)$$

We can use this result to eliminate $V_{gs}(s)$ from equation $(2)'$:

$$\left\{\frac{\frac{1}{Z(s)}\left(g_m - \frac{1}{Z(s)}\right)}{\frac{1}{R_g} + sC_{gs} + \frac{1}{Z(s)}} + \frac{1}{R_d} + sC_{ds} + \frac{1}{Z(s)}\right\}V_{out}(s) = 0$$

$$\left\{\frac{1}{Z(s)}\left(g_m - \frac{1}{Z(s)}\right) + \left(\frac{1}{R_d} + sC_{ds} + \frac{1}{Z(s)}\right)\left(\frac{1}{R_g} + sC_{gs} + \frac{1}{Z(s)}\right)\right\}V_{out}(s) = 0$$

$$\left\{ g_m Z(s) - 1 + \left(\frac{Z(s)}{R_d} + sC_{ds} Z(s) + 1 \right) \left(\frac{Z(s)}{R_g} + sC_{gs} Z(s) + 1 \right) \right\} V_{out}(s) = 0$$

$$\left\{ \begin{array}{l} g_m Z(s) - 1 + \left(\frac{Z(s)}{R_d} + sC_{ds} Z(s) \right) \left(\frac{Z(s)}{R_g} + sC_{gs} Z(s) \right) \\ + \frac{Z(s)}{R_d} + sC_{ds} Z(s) + \frac{Z(s)}{R_g} + sC_{gs} Z(s) + 1 \end{array} \right\} V_{out}(s) = 0$$

$$\left\{ \begin{array}{l} g_m + Z(s) \left(\frac{1}{R_d} + sC_{ds} \right) \left(\frac{1}{R_g} + sC_{gs} \right) \\ + \frac{1}{R_d} + sC_{ds} + \frac{1}{R_g} + sC_{gs} \end{array} \right\} V_{out}(s) = 0$$

$$\left\{ \begin{array}{l} g_m + Z(s) \left[\frac{1}{R_d} \frac{1}{R_g} + s^2 C_{ds} C_{gs} + s \left(\frac{1}{R_d} C_{gs} + \frac{1}{R_g} C_{ds} \right) \right] \\ + \frac{1}{R_d} + \frac{1}{R_g} + s \left(C_{ds} + C_{gs} \right) \end{array} \right\} V_{out}(s) = 0$$

$$\left\{ \begin{array}{l} g_m + Z(s) \left[\frac{1}{R_d} \frac{1}{R_g} + s^2 C_{ds} C_{gs} + s \left(\frac{1}{R_d} C_{gs} + \frac{1}{R_g} C_{ds} \right) \right] \\ + \frac{1}{R_d} + \frac{1}{R_g} + s \left(C_{ds} + C_{gs} \right) \end{array} \right\} V_{out}(s) = 0$$

Since we are interested in the sinusoidal steady state response, we switch to phasor notation by substituting $s = j\omega$:

$$\left\{ \begin{array}{l} g_m + Z(j\omega) \left[\frac{1}{R_d} \frac{1}{R_g} + (j\omega)^2 C_{ds} C_{gs} + (j\omega) \left(\frac{1}{R_d} C_{gs} + \frac{1}{R_g} C_{ds} \right) \right] \\ + \frac{1}{R_d} + \frac{1}{R_g} + (j\omega) \left(C_{ds} + C_{gs} \right) \end{array} \right\} \mathbf{V}_{out} = 0$$

At this point, we take time out to discover a simple approximate form for.

$$Z(j\omega) \equiv R(j\omega) + jX(j\omega) = -j\frac{1}{\omega(C_p + C_{gd})}\frac{\omega^2 - \omega_s^2 - j\omega\frac{R_s}{L}}{\omega^2 - \omega_p^2 - j\omega\frac{R_s}{L}}$$

where we have added C_{gd} to C_p, as mentioned above. A typical value of $\frac{R_s}{L} \sim \frac{10^4}{100} \sim 100$ so that for frequencies greater than $10^5 rad/\sec$, the $j\omega\frac{R_s}{L}$ terms in $Z(j\omega)$ are, except for frequencies quite near ω_p, negligible in comparison to ω^2 and to ω_p^2 and ω_s^2. The main effect of the $j\omega\frac{R_s}{L}$ term in the denominator is to limit the magnitude of the impedance to finite values at frequencies quite near ω_p,. Thus, we use the approximate form

$$Z(j\omega) \equiv R(j\omega) + jX(j\omega) = -j\frac{1}{\omega(C_p + C_{gd})}\frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

In this approximation, therefore, $R(j\omega) = 0$ and

$$Z(j\omega) \equiv jX(j\omega)$$

where

$$X(j\omega) = -\frac{1}{\omega(C_p + C_{gd})}\frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

Thus, we can write our consistency condition as:

$$\left\{\begin{array}{l} g_m + jX(j\omega)\left[\frac{1}{R_d}\frac{1}{R_g} - \omega^2 C_{ds}C_{gs} + j\omega\left(\frac{1}{R_d}C_{gs} + \frac{1}{R_g}C_{ds}\right)\right] \\ + \frac{1}{R_d} + \frac{1}{R_g} + j\omega(C_{ds} + C_{gs}) \end{array}\right\} \mathbf{V}_{out} = 0$$

$$\left\{\begin{array}{l} g_m + jX(j\omega)\left[\frac{1}{R_d}\frac{1}{R_g} - \omega^2 C_{ds}C_{gs}\right] - \omega X(j\omega)\left(\frac{1}{R_d}C_{gs} + \frac{1}{R_g}C_{ds}\right) \\ + \frac{1}{R_d} + \frac{1}{R_g} + j\omega(C_{ds} + C_{gs}) \end{array}\right\} \mathbf{V}_{out} = 0$$

$$\left\{ \begin{array}{l} g_m \; - \; \omega X(j\omega)\left(\dfrac{1}{R_d} C_{gs} + \dfrac{1}{R_g} C_{ds} \right) + \dfrac{1}{R_d} + \dfrac{1}{R_g} \\ \quad + \; jX(j\omega)\left[\dfrac{1}{R_d} \dfrac{1}{R_g} - \omega^2 C_{ds} C_{gs} \right] + j\omega\left(C_{ds} + C_{gs} \right) \end{array} \right\} \mathbf{V}_{out} = 0$$

For useful outputs, $\mathbf{V}_{out} \neq 0$ so that the curly brackets must be zero. Because the content of the curly brackets is a complex number, its real and imaginary parts must be zero separately. Let's first consider the consequences of setting the imaginary part to zero:

$$X(j\omega)\left[\frac{1}{R_d} \frac{1}{R_g} - \omega^2 C_{ds} C_{gs} \right] + \omega\left(C_{ds} + C_{gs} \right) = 0$$

Recalling the approximate form

$$X(j\omega) \approx -\frac{1}{\omega\left(C_p + C_{gd} \right)} \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

we find

$$-\frac{1}{\omega\left(C_p + C_{gd} \right)} \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2} \left[\frac{1}{R_d} \frac{1}{R_g} - \omega^2 C_{ds} C_{gs} \right] + \omega\left(C_{ds} + C_{gs} \right) = 0$$

$$\frac{\omega^2 - \omega_s^2}{\omega_p^2 - \omega^2} \left[\frac{1}{R_d} \frac{1}{R_g} - \omega^2 C_{ds} C_{gs} \right] + \omega^2 \left(C_{ds} + C_{gs} \right)\left(C_p + C_{gd} \right) = 0$$

$$\frac{\omega^2 - \omega_s^2}{\omega_p^2 - \omega^2} \left[\frac{1}{R_d C_{ds}} \frac{1}{R_g C_{gs}} - \omega^2 \right] + \omega^2 \left(\frac{1}{C_{ds}} + \frac{1}{C_{gs}} \right)\left(C_p + C_{gd} \right) = 0$$

For proper operation of the circuit, we need to choose values so that

$$\frac{1}{R_d C_{ds}} \frac{1}{R_g C_{gs}} << \omega^2$$

to minimize dependence of the oscillator frequency, as determined by the equation above, on the resistors R_d and R_g. (We prefer the frequency to depend only on the piezoelectric crystal parameters.) During design, we can satisfy the inequality by choosing large values for R_d and R_g and/or by adding external supplemental capacitances in parallel with C_{ds} and C_{gs}. Supplementing the values of C_{ds} and C_{gs} with sufficiently large fixed external capacitors also

has the advantage of making the equation above for the frequency of the oscillator independent of all transistor parameters. Of course, we must be careful not to make design choices that will require unrealistic values of the transconductance, g_m, to realize unity loop gain. We'll return to this issue later.

If the inequality above is satisfied, then the equation for the oscillator frequency becomes

$$\frac{\omega^2 - \omega_s^2}{\omega_p^2 - \omega^2}\left[-\omega^2\right] + \omega^2\left(\frac{1}{C_{ds}} + \frac{1}{C_{gs}}\right)\left(C_p + C_{gd}\right) = 0$$

or

$$\frac{\omega^2 - \omega_s^2}{\omega_p^2 - \omega^2} = \left(\frac{1}{C_{ds}} + \frac{1}{C_{gs}}\right)\left(C_p + C_{gd}\right) \equiv \alpha$$

where

$$\alpha \equiv \left(\frac{1}{C_{ds}} + \frac{1}{C_{gs}}\right)\left(C_p + C_{gd}\right) > 0$$

is a positive dimensionless constant. Proceeding, we find

$$\omega^2 - \omega_s^2 = \alpha\left(\omega_p^2 - \omega^2\right)$$

$$\left(1 + \alpha\right)\omega^2 = \omega_s^2 + \alpha\,\omega_p^2$$

$$\omega^2 = \frac{\omega_s^2 + \alpha\,\omega_p^2}{1 + \alpha}$$

Note that, regardless of the value of α, the frequency of oscillation is constrained to lie between ω_s and ω_p:

$$\omega_s^2 < \omega^2 < \omega_p^2$$

Thus, the frequency of oscillation is forced, by the piezoelectric crystal, to lie within a very narrow range. Remember that it is only in this frequency range that the piezoelectric crystal behaves as an inductor, a component essential for the basic Colpitts to function as an oscillator.

We now return to the equation

$$\left\{\begin{array}{l} g_m \; - \; \omega X\left(j\omega\right)\left(\frac{1}{R_d}C_{gs} + \frac{1}{R_g}C_{ds}\right) + \frac{1}{R_d} + \frac{1}{R_g} \\ \; + \; jX\left(j\omega\right)\left[\frac{1}{R_d}\frac{1}{R_g} - \omega^2 C_{ds}C_{gs}\right] + j\omega\left(C_{ds} + C_{gs}\right) \end{array}\right\} \mathbf{V}_{out} = 0$$

and consider the consequences of the real part of its curly brackets being zero:

$$g_m \; - \; \omega X\left(j\omega\right)\left(\frac{1}{R_d}C_{gs} + \frac{1}{R_g}C_{ds}\right) + \frac{1}{R_d} + \frac{1}{R_g} = 0$$

If we use our earlier result that

$$X\left(j\omega\right) \approx -\frac{1}{\omega\left(C_p + C_{gd}\right)}\frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

then we see

$$g_m + \frac{1}{\left(C_p + C_{gd}\right)}\frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}\left(\frac{1}{R_d}C_{gs} + \frac{1}{R_g}C_{ds}\right) + \frac{1}{R_d} + \frac{1}{R_g} = 0$$

$$g_m = \frac{C_{gs}C_{ds}}{\left(C_p + C_{gd}\right)}\frac{\omega_s^2 - \omega^2}{\omega^2 - \omega_p^2}\left(\frac{1}{R_dC_{ds}} + \frac{1}{R_gC_{gs}}\right) - \frac{1}{R_d} - \frac{1}{R_g}$$

Recall that

$$\frac{\omega^2 - \omega_s^2}{\omega_p^2 - \omega^2} = \left(\frac{1}{C_{ds}} + \frac{1}{C_{gs}}\right)\left(C_p + C_{gd}\right) \equiv \alpha$$

Thus,

$$g_m = \frac{C_{gs}C_{ds}}{\left(C_p + C_{gd}\right)}\left(\frac{1}{C_{ds}} + \frac{1}{C_{gs}}\right)\left(C_p + C_{gd}\right)\left(\frac{1}{R_dC_{ds}} + \frac{1}{R_gC_{gs}}\right) - \frac{1}{R_d} - \frac{1}{R_g}$$

$$g_m = \left(C_{ds} + C_{gs}\right)\left(\frac{1}{R_dC_{ds}} + \frac{1}{R_gC_{gs}}\right) - \frac{1}{R_d} - \frac{1}{R_g}$$

$$g_m = \frac{C_{ds} + C_{gs}}{R_d C_{ds}}\left(1 + \frac{R_d C_{ds}}{R_g C_{gs}}\right) - \frac{1}{R_d} - \frac{1}{R_g}$$

$$g_m = \frac{1}{R_d}\left(1 + \frac{C_{gs}}{C_{ds}}\right)\left(1 + \frac{R_d C_{ds}}{R_g C_{gs}}\right) - \frac{1}{R_d} - \frac{1}{R_g}$$

Because the drain in an FET is much further away from the source than is the gate, we find, in practice, $C_{ds} << C_{gs}$. In practice, it is also true that the parallel combination of the gate resistors, $R_g >> R_d$, the drain resistor. With little error, then, we can write

$$g_m = \frac{1}{R_d}\left(1 + \frac{C_{gs}}{C_{ds}}\right) - \frac{1}{R_d}$$

or

$$g_m = \frac{1}{R_d}\left(\frac{C_{gs}}{C_{ds}}\right)$$

This equation gives the critical minimum value of g_m necessary to achieve unity loop gain. To make the loop gain slightly larger to improve reliability in the operation of the oscillator, we should choose g_m to be larger than the minimum value given by the equation:

$$g_m > \frac{1}{R_d}\frac{C_{gs}}{C_{ds}}$$

Notice that the minimum transconductance, g_m, depends only on the ratio of the capacitances. Note also that the required g_m can be reduced by increasing R_d and/or C_{ds}. Increasing R_d increases the voltage gain of the FET amplifier, as we have seen. For a given operating point for the FET, however, increasing R_d means increasing the power supply voltage, which may not be easy to do. Increasing C_{ds} increases the fraction of the output fed back into the input. Increasing C_{ds} also helps us to satisfy the inequality

$$\frac{1}{R_d C_{ds}}\frac{1}{R_g C_{gs}} << \omega^2$$

Thus, it makes sense to add an external capacitor in parallel with C_{ds} to decrease the g_m required for oscillation and to reduce the sensitivity of the frequency of oscillation to values of the resistors R_d and R_g. If it does not make satisfying the above inequality too difficult, we can add a supplemental external capacitor in parallel with C_{gs} to make the frequency of oscillation essentially independent to the values of any parameters except those of the piezoelectric crystal,

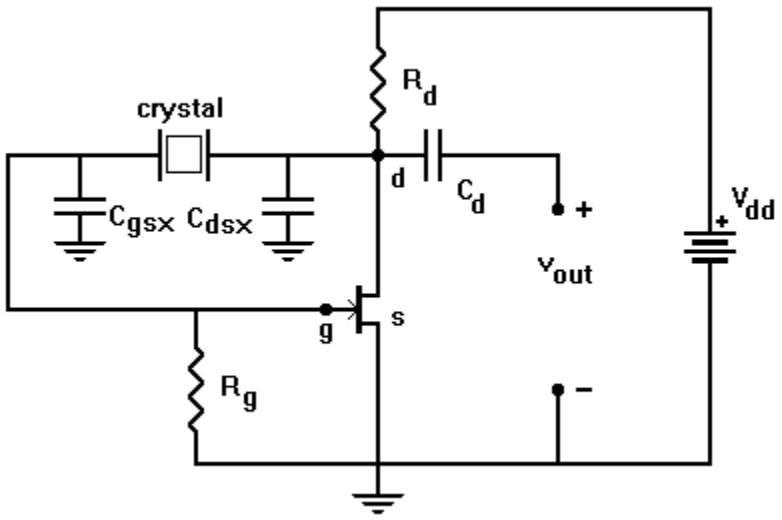
which are remarkable stable. If extreme frequency stability is required, the piezoelectric crystal can be placed in a controlled temperature oven to reduce even further the already slight variation of the piezoelectric crystal parameters caused by changes in temperature. A further advantage of increasing C_{ds} is that it, together with R_d, provides low pass filtering of the output to reduce harmonic content and prevent oscillations at overtones.

Recall that the transconductance, g_m, for an FET is given by

$$g_m = \frac{2|I_{dss}|}{|V_p|}\left(1 - \frac{V_{gsq}}{V_p}\right)$$

where V_p and I_{dss} are parameters for a particular FET and V_{gsq} is the bias value of the gate-source voltage. The value of g_m for a particular FET is greatest when $V_{gsq} = 0$. To achieve this condition, the Pierce oscillator circuit that we showed initially is often modified by setting $R_s = 0$ and letting $R_{b2} \to \infty$. With $R_s = 0$ note that C_s is unnecessary.

If we redraw our initial circuit to reflect the addition of supplemental external capacitors for C_{ds} and C_{gs}, as well as the removal of R_s, R_{b2} and C_s, we have:



where C_{dsx} and C_{gsx} are the supplemental external capacitors for C_{ds} and C_{gs}, respectively. This configuration, with external capacitors, is sometimes called a Colpitts crystal oscillator, rather than a Pierce crystal oscillator. In practice, a CMOS inverter is often substituted for the FET. Note that despite the changes, the signal equivalent circuit that we analyzed still applies, and hence all of our analysis still holds, provided only that we replace C_{dsx} and C_{gsx} with $C_{dsx} + C_{dsxx}$ and $C_{gsx} + C_{gsxx}$, respectively.

15.Additional Topics/Known Gaps

1. Effect of cascading on Bandwidth in multistage amplifiers.
2. Characteristics of MOS transistor to obtain small signal equivalent model.
3. Concept of positive feedback its characteristics.
4. Tuned circuits its working principle used in tuned amplifiers

16. UNIVERSITY QUESTION PAPERS WITH PREVIOUS YEAR

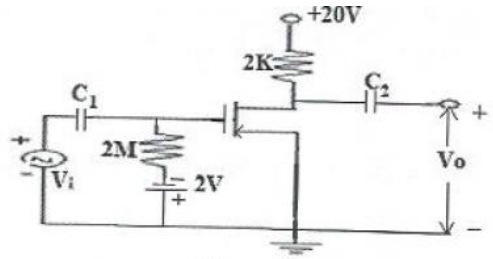


Figure.2

5.a) The block diagram shown in figure.3 is the topology of a feedback amplifier. Mention the

i) Name of the feedback amplifier
ii) Name of the basic amplifier
iii) Name of the input signal, X_i
iv) Name of the feedback signal, X_f
v) Sampling and mixing techniques implemented
vi) Expressions for R_{if} and R_{of}.

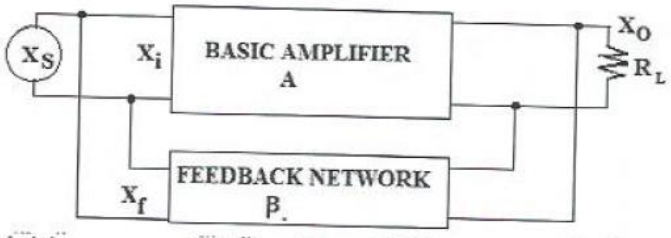


Figure.3

b) It is desired to reduce the total harmonic distortion of an amplifier from 8% to 2% by implementing 5% negative feedback. Estimate the gain of the amplifier with original distortion and with reduced distortion? [8+7]

6.a) Draw an RC oscillator to generate stable oscillations with variable frequency facility. Derive expression for its frequency of oscillation. Also show that the minimum gain required for maintaining oscillation is 3?

b) A Colpitts oscillator has a coil with an inductance of 50mH and is tuned by a capacitor of 300pF across the amplifier input and 100pF across the output. Find the frequency of oscillation and minimum for maintaining oscillation? [10+5]

7.a) Derive the expression, with necessary diagrams, to calculate the total harmonic distortion 'D' in power amplifiers using the three-point method of analysis.

b) A transformer- coupled class-A amplifier supplies 2W of power to speaker. If the supply voltage is 36V and I_{CQ} is 150mA, find the efficiency of the circuit. [10+5]

8.a) Explain the operation of a double-tuned amplifier with a neat sketch and obtain an equation for its gain-bandwidth product?

b) What is meant by parasitic oscillation in tuned amplifiers? How it can be suppressed? [12+3]

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(b) The amplifier shown in figure 2 uses an n - channel FET having I_{DSS} = 2mA, V_P = -2V. If the quiscent drain to ground voltage is 10V, find R_1 and the effective input impedance. [7+8]

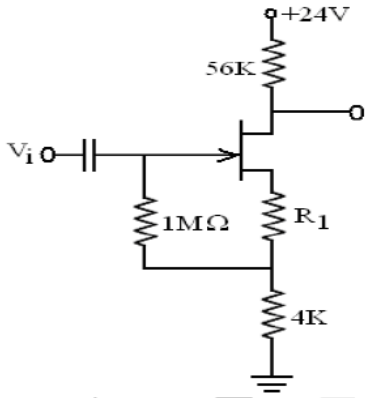

Figure 2:

5. (a) Draw the equivalent circuit of a double tuned amplifier and derive the expression for gain at resonance.
   (b) Derive the expression for effective bandwidth of cascaded tuned amplifier. [8+7]

6. (a) Derive an expression for the transfer gain of a feedback amplifier.
   (b) The feedback amplifier shown in figure 3 has transistor parameters h_{ie} = 1k h_{re} and h_{oe} negligible. Find $R_{mf} = V_o/I_s$, $A_{vf} = V_o/V_s$, R_{if} and R_{of}. [5+10]

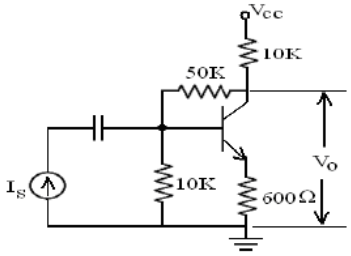

Figure 3:

7. (a) Prove that $h_{fe} = g_m r_{b'e}$
   (b) How does g_m vary with $|I_C|$, $|V_{CE}|$ &T?
   (c) Draw the small-signal high frequency CE model of a transistor. [5+5+5]

8. (a) How the bandwidth is effected in multistage amplifier?
   (b) What are the advantages of direct coupled amplifiers?

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(c) What is the use of transformer coupling in the output stage of multi-stage amplifier?

[5+5+5]

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011

ELECTRONIC CIRCUIT ANALYSIS

(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

Time: 3hours Max. Marks: 75

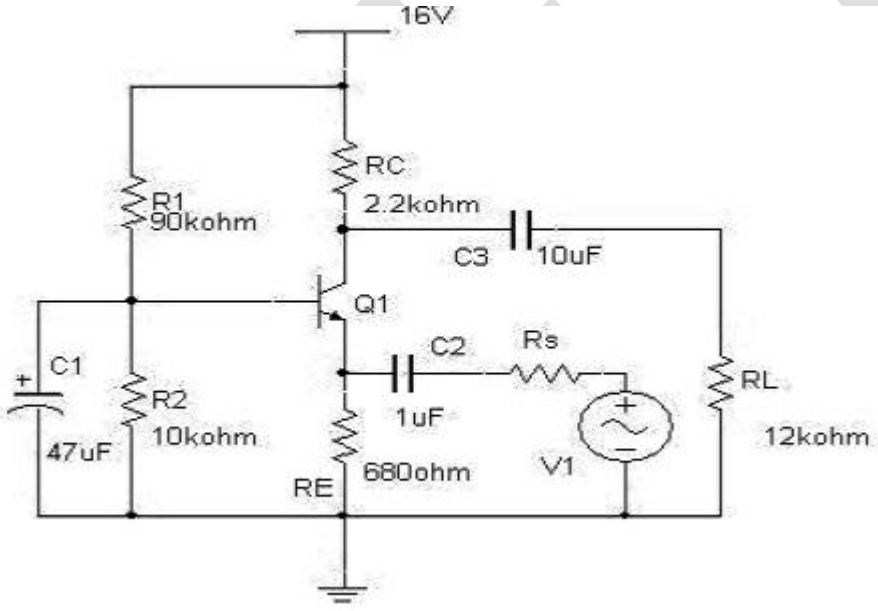
Answer any FIVE questions

All Questions Carry Equal Marks

1.a) For the CB amplifier circuit shown, compute RIN and ROUT if C1 is i) Connected ii) Not connected

The h-parameters of the transistor in CE configuration are listed as:

hie = 2.1KΩ, hfe = 81, hoe = 1.66 µMhos and hre is negligibly small.



b) Reason out the causes and results of Phase & Frequency distortions in transistor amplifiers. [9+6]

2.a) Differentiate between direct and capacitive coupling of multiple stages of amplifiers.

b) With the help of a neat circuit diagram, describe the working of a cascode amplifier.

c) What are the merits and demerits of a cascade amplifier over a simple Common Emitter amplifier? [4+7+4]

3.a) Derive the expressions for hybrid Π conductance, gce, and gbb' of a transistor.

b) Explain how hybrid Π parameters, gm and gce vary with Ic, Vce and temperature.

c) Compute the overall lower cut-off frequency of an identical two stage cascade of

amplifiers with individual lower cut-off frequency given as 432 Hz. [7+4+4]

4.a) Discuss the effect of different type of loads to a common source MOS amplifier.
b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a) If negative feedback with a feedback factor, β of 0.01 is introduced into an amplifier with a gain of 200 and bandwidth of 6 MHz, obtain the resulting bandwidth of the feedback amplifier.
b) With the help of a suitable BJT based voltage series feedback amplifier diagram, explain the features and benefits of negative feedback in amplifiers. [6+9]
6.a) Substantiate the requirement of positive feedback in amplifier for oscillations. Relate the requirement to Barkhausen Criterion.
b) With the help of neat circuit diagram, explain how sustained oscillations are obtained in RC phase shift BJT based oscillator. Derive the expression for frequency of oscillation. [6+9]
7.a) A single stage class A amplifier Vcc=20V, VCEQ =10V, ICQ =600mA, RL=16 Ω. The ac output current varies by 300mA, with the ac input signal. Find
i) The power supplied by the dc source to the amplifier circuit.
ii) AC power consumed by the load resistor.
iii) AC power developed across the load resistor.
iv) DC power wasted in transistor collector.
v) Overall efficiency
vi) Collector efficiency.
b). List the advantages of complementary-symmetry configuration over push pull configuration. [9+6]
8. Describe the following briefly:
a) Stagger Tuned Amplifiers – Operation and comparison with synchronous tuning
b) Heat Sinks for tuned power amplifiers. [8+7]

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011

ELECTRONIC CIRCUIT ANALYSIS

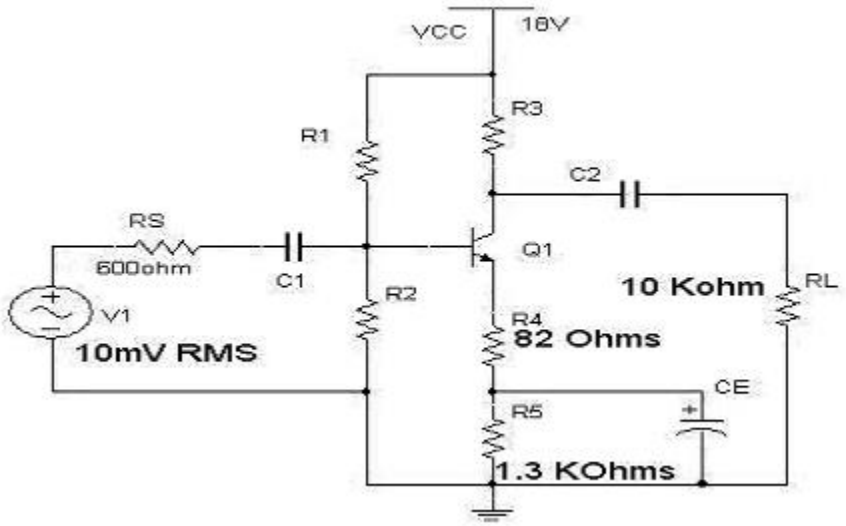
(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

Time: 3hours Max. Marks: 75

Answer any FIVE questions

All Questions Carry Equal Marks

1. For the amplifier circuit shown with partially unbypassed emitter resistance, calculate the voltage gain with R4 in place and with R4 shorted. Consider hie = 1.1KΩ, hfe = 100, hre & hoe are negligibly small. Assume R1 and R2 to be 100KΩ and 22 KΩ respectively.



b) Analyse what the output voltage should be if the DC power supply given to a CE amplifier is shorted to ground. [10+5]

2.a) With the help of circuit diagram and equivalent circuit of a Darlington amplifier generate the expression for the overall input impedance of the pair.

b) Develop a generalized expression for overall current gain(AIS) when two transistor stages with ROUT2 < RL, ROUT1 > RIN2, RIN1> RS and individual voltage gains are AV1, AV2. [7+8]

3.a) A transistor amplifier in CE configuration is operated at high frequency with the following specifications. fT=6MHz, gm=0.04,hfe =50, rbb' =100 Ω, Rs =500 Ω , Cb'c =10pF, RL=100 Ω. Compute the voltage gain, upper 3dB cut-off frequency, and gain

bandwidth product (GBW).
b) Derive an expression for the overall higher cut-off frequency of a two stage amplifier with identical stages of individual higher cut-off frequency, fH. [7+8]

4.a) Discuss the effect of different type of loads to a common source MOS amplifier.
b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a). If the non-linear distortion in a negative feedback amplifier with an open loop gain of 100 is reduced from 40% to 10%with feedback, compute the feedback factor, β of the amplifier.
b) Draw the circuit diagram of a current series feedback amplifier, Derive expressions to show the effect of negative feedback on input & output impedances, bandwidth, distortion of the amplifier. [6+9]

6.a) Differentiate between RC and LC type oscillators.
b) Derive the expression for frequency of oscillation in a Hartley Oscillator.
c) State Barkhausen Critterion for Oscillations [5+7+3]

7.a) Derive the expression for maximum conversion efficiency for a simple series fed Class A power amplifier.
b) What are the drawbacks of transformer coupled power amplifiers?
c) A push pull amplifier utilizes a transformer whose primary has a total of 160 turns and whose secondary has 40 turns. It must be capable of delivering 40W to an 8 Ω load under maximum power conditions. What is the minimum possible value of Vcc? [5+4+6]

8.a) List possible configurations of tuned amplifiers.
b) Derive an expression for bandwidth of a capacitive coupled tuned amplifier in CE configuration. Make necessary assumptions and mention them. [6+9]

R09 SET No -3 CODE NO: R09220402

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011

ELECTRONIC CIRCUIT ANALYSIS

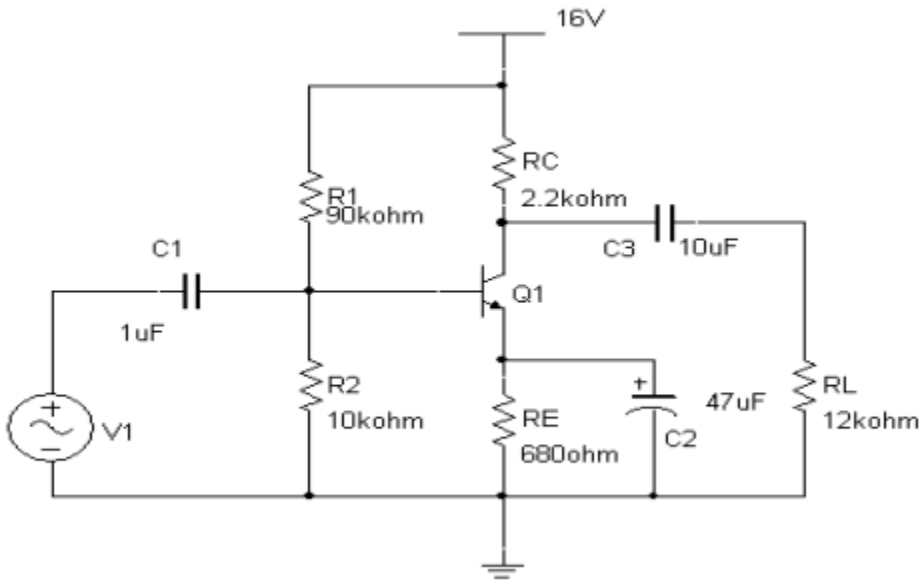
(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

Time: 3hours Max. Marks: 75

Answer any FIVE questions

All Questions Carry Equal Marks

1.a) For the common emitter amplifier shown, draw the AC and DC load lines. Determine the peak-to-peak output voltage for a sinusoidal input voltage of 30mV peak-to-peak. Assume C1, C2 and C3 are large enough to act as short circuit at the input frequency. Consider hie = 1.1KΩ, hfe = 100, hre & hoe are negligibly small.



b) State Miller's theorem. Specify its relevance in the analysis of a BJT amplifier.

c) Write expressions for AV and RIN of a Common Emitter amplifier. [7+4+4]

2.a) Derive expressions for overall voltage gain and overall current gain of a two-stage RC coupled amplifier.

b) List out the special features of Darlington pair and cascode amplifiers. [9+6]

3.a) Discuss the effect of emitter bypass capacitor and input & output coupling capacitors on the lower cut-off frequency if number of amplifiers are cascaded.

b) Describe how an emitter follower behaves at high frequencies. [8+7]

4.a) Discuss the effect of different types of loads to a common source MOS amplifier.

b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a) The β and the open loop gain of an amplifier are -10% and -80 respectively. By how much % the closed loop gain changes if the open loop gain increases by 25%?

b) Compare the characteristics of feedback amplifiers in all the four configurations.

c) Reason out why 2 stages are required to implement current shunt feedback. [5+6+4]

6. Starting from the description of a generalized oscillator, derive the expression for frequency of oscillation in a colpitts oscillator. [15]

7.a) With the help of a suitable circuit diagram, show that the maximum conversion efficiency of a class B power amplifier is 78.5%.

b) Explain how Total harmonic distortion can be reduced in a Class B push-pull configured amplifier. [7+8]

8.a) Derive an expression for the bandwidth of a synchronous tuned circuit.

b) Discuss the necessity of stabilization circuits in tuned amplifiers. [8+7]

******** R09 SET No -4 CODE NO: R09220402

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011

ELECTRONIC CIRCUIT ANALYSIS

(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

Time: 3hours Max. Marks: 75

Answer any FIVE questions

All Questions Carry Equal Marks

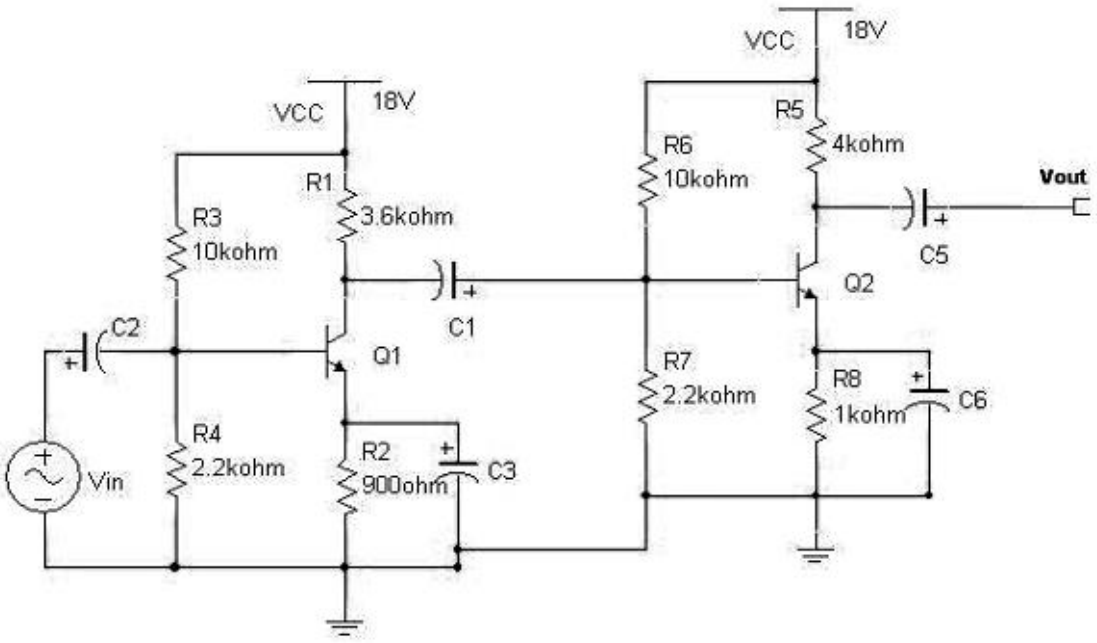
1.a) Draw the circuit diagram of a common collector amplifier along with its equivalent circuit. Derive expressions for AV and RI.

b) What is meant by small signal for analyzing a BJT based amplifier?

c) What is non-linear distortion? List the causes for this type of distortion in amplifiers. [7+4+4]

2.a) Discuss various possibilities of inter-stage coupling of amplifiers.

b) For the two-stage RC coupled amplifier circuit shown, calculate the Individual stage voltage gains and the overall voltage gain. Input impedance of individual stages is given as 2.4 KΩ and β of individual transistors as 80. [6+9]



3.a) A transistor has fα = 8MHz, and β=80.when connected as an amplifier, it has stray capacitance of 100pF at the output terminal. Calculate its upper 3dB frequency when Rload is

i) 10KΩ ii) 100KΩ.

b) Discuss the effect of coupling capacitors of a CE amplifier on the overall frequency response of the amplifier. [8+7]

4.a) Discuss the effect of different type of loads to a common source MOS amplifier.

b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a) An amplifier has a gain of 50 with negative feedback. For a specified output voltage, if the input required is 0.1V without feedback and 0.8V with feedback, Compute β and open loop gain.

b) Through the block schematics, show four types of negative feedback in amplifiers.

c) List the advantages of negative feedback in amplifiers. [5+5+5]

6.a) List out the merits × demerits of oscillators.

b) With the help of suitable schematic and description, show that both positive and negative feedback are used in a Wien Bridge oscillator. Establish the condition for oscillations. [7+8]

7.a) State the merits of using push pull configuration? Describe the operation of class B

push pull amplifier and show how even harmonics are eliminated.
b) A single ended class A amplifier has a transformer coupled load of 8 Ω. If the transformer turns ration is 10, find the maximum power output delivered to the load. Take the zero signal collector current of 500mA. [7+8]

8.a) Derive the expressions for Bandwidth and Q-factor of single tuned, capacitively coupled amplifiers. List the assumptions made for the derivation.
b) What is stagger tuning? Suggest possible applications. [9+6]

****

Time: 3 hours Max. Marks.80
Answer any Five questions
All questions carry equal marks

1. Write the analysis of a CE amplifier circuit using h parameters. Derive the expressions for AI, AV, Ri, R0, AIs, AVs. (16)

2. (a) Sketch two RC-coupled CE transistor stages. Show the middle and low frequency model for one stage. Write the expressions for current gains. (12)
(b) Draw the circuit diagram of cascode amplifier with and without biasing circuit. What is the advantages of this. (4)

3. Draw the hybrid-pi model, explain and derive the conductance and capacitances. (16)

4. (a) How even harmonics is eliminated using push-pull circuit, derive the expression. (8)
(b) Write about the operation of a class D amplifier. (8)

5. (a) Derive the expression for bandwidth in terms of resonant frequency and quality factor in case of double tuned amplifiers. (10)
(b) Differentiate between synchronous tuned amplifiers and tapped tuned amplifiers. (6)

6. Design consideration for video amplifiers. (8)
(b) Explain about cascode video amplifier with neat diagram. (8)

7. Explain the operation of low and high voltage regulators using 723 IC. (16)

8. Explain the basic switching regulator and types of it with neat diagrams. Time: 3 hours Max. Marks.80

ELECTRONIC CIRCUIT ANALYSIS

(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

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The h-parameters of the transistor in CE configuration are listed as:

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b) Reason out the causes and results of Phase & Frequency distortions in transistor amplifiers. [9+6]

2. a) Differentiate between direct and capacitive coupling of multiple stages of amplifiers.

b) With the help of a neat circuit diagram, describe the working of a cascode amplifier.

c) What are the merits and demerits of a cascade amplifier over a simple Common Emitter amplifier? [4+7+4]

3. a) Derive the expressions for hybrid Π conductance, $g_{ce,}$ and $g_{bb'}$ of a tran sistor.

b) Explain how hybrid Π parameters, g_m and g_{ce} vary with I_c, V_{ce} and temperature.

c) Compute the overall lower cut-off frequency of an identical two stage cascade of amplifiers with individual lower cut-off frequency given as 432 Hz. [7+4+4]

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5.a) If negative feedback with a feedback factor, β of 0.01 is introduced into an amplifier with a gain of 200 and bandwidth of 6 MHz, obtain the resulting bandwidth of the feedback amplifier.

b) With the help of a suitable BJT based voltage series feedback amplifier diagram, explain the features and benefits of negative feedback in amplifiers. [6+9]

6.a) Substantiate the requirement of positive feedback in amplifier for oscillations. Relate the requirement to Barkhausen Criterion.

b) With the help of neat circuit diagram, explain how sustained oscillations are obtained in RC phase shift BJT based oscillator. Derive the expression for frequency of oscillation. [6+9]

7.a) A single stage class A amplifier V_{cc}=20V, V_{CEQ} =10V, I_{CQ} =600mA, R_L=16 Ω. The ac output current varies by 300mA, with the ac input signal. Find ±

i) The power supplied by the dc source to the amplifier circuit.

ii) AC power consumed by the load resistor.

iii) AC power developed across the load resistor.

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vi) Collector efficiency.

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II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011

ELECTRONIC CIRCUIT ANALYSIS

(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

- - -

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b) Analyse what the output voltage should be if the DC power supply given to a CE amplifier is shorted to ground. [10+5]

2.a) With the help of circuit diagram and equivalent circuit of a Darlington amplifier generate the expression for the overall input impedance of the pair.

b) Develop a generalized expression for overall current gain(A_{IS}) when two transistor stages with $R_{OUT2} < R_L$, $R_{OUT1} > R_{IN2}$, $R_{IN1} > R_S$ and individual voltage gains are A_{V1}, A_{V2}. [7+8]

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[5+4+6]

8.a) List possible configurations of tuned amplifiers.

b) Derive an expression for bandwidth of a capacitive coupled tuned amplifier in CE configuration. Make necessary assumptions and mention them. [6+9]

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011

ELECTRONIC CIRCUIT ANALYSIS

(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics, Instrumentation & Control Engineering)

Time: 3hours Max. Marks: 75

Answer any FIVE questions

All Questions Carry Equal Marks

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1.a) For the common emitter amplifier shown, draw the AC and DC load lines. Determine the peak-to-peak output voltage for a sinusoidal input voltage of 30mV peak-to-peak. Assume C_1, C_2 and C_3 are large enough to act as short circuit at the input frequency. Consider $h_{ie} = 1.1K\Omega$, $h_{fe} = 100$, h_{re} & h_{oe} are negligibly small.

b) State Miller's theorem. Specify its relevance in the analysis of a BJT amplifier.

c) Write expressions for A_V and R_{IN} of a Common Emitter amplifier. [7+4+4]

2.a) Derive expressions for overall voltage gain and overall current gain of a two-stage RC coupled amplifier.

b) List out the special features of Darlington pair and cascode amplifiers. [9+6]

3.a) Discuss the effect of emitter bypass capacitor and input & output coupling capacitors on the lower cut-off frequency if number of amplifiers are cascaded.

b) Describe how an emitter follower behaves at high frequencies. [8+7]

4.a) Discuss the effect of different types of loads to a common source MOS amplifier.

b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a) The β and the open loop gain of an amplifier are -10% and -80 respectively. By how much % the closed loop gain changes if the open loop gain increases by 25%?

b) Compare the characteristics of feedback amplifiers in all the four configurations.

c) Reason out why 2 stages are required to implement current shunt feedback. [5+6+4]

6. Starting from the description of a generalized oscillator, derive the expression for frequency of oscillation in a colpitts oscillator. [15]

7.a) With the help of a suitable circuit diagram, show that the maximum conversion efficiency of a class B power amplifier is 78.5%.

b) Explain how Total harmonic distortion can be reduced in a Class B push-pull configured amplifier. [7+8]

8.a) Derive an expression for the bandwidth of a synchronous tuned circuit.

b) Discuss the necessity of stabilization circuits in tuned amplifiers. [8+7]

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II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
ELECTRONIC CIRCUIT ANALYSIS
(Common to Electronics & Communication Systems, Electronics & Computer Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics,)

1.a) Draw the circuit diagram of a common collector amplifier along with its equivalent circuit. Derive expressions for A_V and R_I.

b) What is meant by small signal for analyzing a BJT based amplifier?

c) What is non-linear distortion? List the causes for this type of distortion in amplifiers.

2.a) Discuss various possibilities of inter-stage coupling of amplifiers.

b) For the two-stage RC coupled amplifier circuit shown, calculate the Individual stage voltage gains and the overall voltage gain. Input impedance of individual stages is given as 2.4 KΩ and β of individual transistors as 80. [6+9]

3.a) A transistor has f_α = 8MHz, and β=80.when connected as an amplifier, it has stray capacitance of 100pF at the output terminal. Calculate its upper 3dB frequency when R_{load} is

i) 10KΩ ii) 100KΩ.

b) Discuss the effect of coupling capacitors of a CE amplifier on the overall frequency response of the amplifier. [8+7]

4.a) Discuss the effect of different type of loads to a common source MOS amplifier.

b) Differentiate between cascode and folded cascode configurations. [8+7]

5.a) An amplifier has a gain of 50 with negative feedback. For a specified output voltage, if the input required is 0.1V without feedback and 0.8V with feedback, Compute β and open loop gain.

b) Through the block schematics, show four types of negative feedback in amplifiers.

c) List the advantages of negative feedback in amplifiers. [5+5+5]

6.a) List out the merits × demerits of oscillators.

b) With the help of suitable schematic and description, show that both positive and negative feedback are used in a Wien Bridge oscillator. Establish the condition for oscillations. [7+8]

7.a) State the merits of using push pull configuration? Describe the operation of class B push pull amplifier and show how even harmonics are eliminated.

b) A single ended class A amplifier has a transformer coupled load of 8 Ω. If the transformer turns ration is 10, find the maximum power output delivered to the load. Take the zero signal collector current of 500mA. [7+8]

8.a) Derive the expressions for Bandwidth and Q-factor of single tuned, capacitively coupled amplifiers. List the assumptions made for the derivation.

b) What is stagger tuning? Suggest possible applications. [9+6]

17. UNIT-WISE QUESTION BANK

UNIT 1:

1. Explain the classification of amplifiers?

2. Draw the circuit of CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?

3. Draw the circuit of CE amplifier with un bypassed emitter resistor and derive expressions for Ri, Ro ,Av &Ai using approximate h-parameter model?

4. Draw the circuit of CC amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?

5. Compare different types of amplifier circuits?

6. Explain the term multistage amplifiers & its advantages?

7. Draw the circuit of two stage RC coupled CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?

8. Draw the circuit of cascade CB-CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?

9. Draw the circuit of CC- CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?

10. Draw the circuit of Darlington CC amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model and its merits &demerits ?

UNIT 2:

1. What is frequency response and explain how it is obtained?

2. Explain the relation between low frequency gain &mid frequency gain with suitable expres

sions?

3. Explain the terms B.W, cutoff frequencies of an amplifier circuit?

4. Draw the equivalent circuit of a transistor at high frequencies(i.e) hybrid π model?

5. Explain Gain-bandwidth product for voltage &current?

6. Explain small signal model of a MOS transistor its equivalent circuit?

7. Explain the circuit of CS amplifier with resistive load using small signal model?

8. Explain the circuit of CS amplifier with diode connected load using small signal model?

9. Explain common gate amplifier circuit and derive expressions for Ri, Ro &Av?

10. Draw the circuit for folded cascade amplifier and explain its analysis using small signal model?

UNIT 3:

1. Show that for voltage shunt feedback amplifier transresistance gain R_i and R_o are decreased by a factor $(1+A\beta)$ with feedback?

2. Explain the concept of feedback with block diagram applied to an amplifier circuit. What are the advantages and disadvantages of positive & negative feedback?

3. Draw the circuit diagram of current shunt feedback amplifier and expressions for R_{if} and R_{of}?

4. Draw the frequency response of an amplifier with &without feedback and show the bandwidth for each case and how these two curves are related?

5. Draw the circuit diagram of voltage series feedback amplifier and expressions for R_{if} and R_{of}?

6. Explain the concept of positive feedback used in oscillators. State and explain Barkhausen criterion?

7. Show that the gain of Wien bridge oscillator using BJT amplifier must be at least **3** for the oscillations to occur?

8. Explain the basic circuit of an LC oscillator and derive the conditions for the oscillations?

9. What are the factors that affect frequency stability of an oscillator? How frequency stability improved in oscillators?

10. Draw the circuit diagram of RC phase shift oscillator using BJT.derive the expression for frequency of oscillatoions?

UNIT 4:

1. Explain about class A, class B, class C and class AB operation of power amplifiers?

2. Draw the circuit diagram of complementary symmetry push pull amplifier and its working?

3. Distinguish between crossover distortion and harmonic distortion. How they can be eliminated?

4. Show that the efficiency of class A amplifier is 50%?

5. Explain the concept of heat sinks?

UNIT 5:

1. What is meant by the term tuned amplifier and briefly explain the various methods of classification of tuned amplifiers?

2. Draw the ideal and actual frequency response curves of single tuned amplifier?

3. Draw the circuit diagram and small signal A.C equivalent circuit of a single tuned amplifier with the tank circuit connected at the input side?

4. Derive the expressions for B.W in terms of resonant frequency and quality factor in case of double tuned amplifiers?

5. Explain in detail the effect of cascading tuned amplifier and hence derive the expression for B.W of n-stage amplifier. Also draw the frequency response and explain what happens as the no .of stages increases?

18. Assignment Questions

UNIT 1

Part A:

1. Explain the basic amplifier circuit and its components?

2. Using hybrid model explain the circuit of CB amplifier and derive expressions for Ri, Ro ,Av &Ai ?

3. Draw the circuit of CE amplifier with un bypassed emitter resistor and derive expressions for Ri, Ro ,Av &Ai using approximate h-parameter model?

4. Draw the circuit of CC amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?

5. Compare different types of amplifier circuits?

Part B:

1. Explain the concept of multistage amplifiers and its merits&demerits?

2. Draw the circuit of Bootstrapped Darlington CC amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model and its merits &demerits ?

3. Draw the circuit of two stage RC coupled CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?

4. Draw the circuit of cascade CB-CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?

5. Draw the circuit of CC- CE amplifier and derive expressions for Ri, Ro ,Av &Ai using h-parameter model?

UNIT 2

Part A:

1. Explain the frequency response of single stage amplifier?

2. Derive the expressions for lower& upper cutoff frequencies?

3. Explain the terms B.W, cutoff frequencies of an amplifier circuit?

4. Draw the equivalent circuit of a transistor at high frequencies (i.e) hybrid π model?

5. Explain Gain-bandwidth product for voltage &current?

Part B**:**

1. Explain small signal model of a MOS transistor its equivalent circuit?

2. Explain the circuit of CS amplifier with resistive load using small signal model?

3. Explain the circuit of CS amplifier with diode connected load using small signal model?

4. Explain common gate amplifier circuit and derive expressions for Ri, Ro &Av?

5. Draw the circuit for folded cascade amplifier and explain its analysis using small signal model?

UNIT 3

Part A:

1. Show that for voltage shunt feedback amplifier transresistance gain R_i and R_o are decreased by a factor (1+Aβ) with feedback?

2. Explain the concept of feedback with block diagram applied to an amplifier circuit. What are the advantages and disadvantages of positive & negative feedback?

3. Draw the circuit diagram of current shunt feedback amplifier and expressions for R_{if} and R_{of}?

4. Draw the frequency response of an amplifier with &without feedback and show the bandwidth for each case and how these two curves are related?

5. Draw the circuit diagram of voltage series feedback amplifier and expressions for R_{if} and R_{of}?

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1. Explain the concept of positive feedback used in oscillators. State and explain Barkhausen criterion?

2. Show that the gain of Wien bridge oscillator using BJT amplifier must be at least **3** for the oscillations to occur?

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1. Explain about class A, class B, class C and class AB operation of power amplifiers?

2. Draw the circuit diagram of complementary symmetry push pull amplifier and its working?

3. Distinguish between crossover distortion and harmonic distortion. How they can be eliminated?

4. Show that the efficiency of class A amplifier is 50%?

5. Explain the concept of heat sinks?

UNIT 5

1. What is meant by the term tuned amplifier and briefly explain the various methods of classification of tuned amplifiers?

2. Draw the ideal and actual frequency response curves of single tuned amplifier?

3. Draw the circuit diagram and small signal A.C equivalent circuit of a single tuned amplifier with the tank circuit connected at the input side?

4. Derive the expressions for B.W in terms of resonant frequency and quality factor in case of double tuned amplifiers?

5. Explain in detail the effect of cascading tuned amplifier and hence derive the expression for B.W of n-stage amplifier. Also draw the frequency response and explain what happens as the no .of stages increases?

19. Unit wise Quiz Questions and long answer questions

Unit 1:

1) Critical capacitance with smallest equivalent resistance that determines the lower cut off of CB amplifier is
a) I/P coupling capacitor
b) Emitter bypass capacitor if c1 = c2
c) c2 output coupling capacitor
d) None.

2).resultant phase shift of odd no of CE amplifier stages at mid band frequency is
a)3600
b) 1800
c) 450
d) 900

3) The miller input capacitance in CB AMP IS
a) Large compared to miller capacitance in CE
b) very large because of +ve voltage gain in CB
c) Small because of +ve voltage gain in CB
d) Is not negligible compare to other capacitance

4) Identify the correct statement regarding the voltage gain of a CE transistor amplifier
a) it increases with increase in ac load R
b) it is independent of ac load R & is large
c) it decreases with increase in ac load R
d) it is always approximately unity

5) Identify the incorrect statement
[d]
a) frequency distortion in an amplifier is mainly due to the reactive component circuit
b) amplitude distortion is also referred to as non-linear distortion
c) distortion in amplifier due to unequal phase shifts at different frequencies is called delay distortion
d) phase shift distortion is same as frequency distortion
ans: [D]

6) i/p &o/p capacitors in a transistors amplifier are not referred to as
[a]
a) inter electrode capacitors
b) coupling capacitors
c) blocking capacitors
d) dc de-coupling capacitors
ans : [A]

7) CB amplifier of BJT is similar in behaviour with following FET configuration
[a]
a)common gate amplifier
b) common drain amplifier
C) common source amplifier
d)swamped source resistor amplifier
ans:[A]

8) The miller i/p capacitance in CB amplifier
[c]
a) Is large compared to miller capacitance in CE
b) is very large because of +ve voltage gain in CB
c) is small because of +ve voltage gain in CB
d) not negligible compared to other capacitance
ans: [C]

9) CE is the capacitance of forward biased junction & is therefore
[c]
a) independent of collector current
b) much lager than Cc
c) mainly diffusion capacitance
d) mainly transition capacitance
ans: [C]

10) dissipation capability of a transistor is defined as
[a]
a) capability to launch heat generated into the surroundings
b) deviation in power delivered to load resistor

c) capability to withstand the variation in dc power at operating power
d) deviation in o/p & i/p signal wave shapes
ans: [A]

11) phase difference between o/p voltage &i/p voltage of a CC amplifier at mid band frequencies
[b]
a) 1800
b) 00
c) 450
d) 900
ans : [B]

12) major draw back of Darlington transistor pair
[d]
a) low current gain compared to single emitter follower
b) dependence of Av on transistor selected
c) low i/p impedance compared to single emitter follower
d) dependence of H -parameters on quiescent conditions
ans: [D]

13) cascade amplifier is 2- transistor combination has
a) collector of first transistor is connected to the base of second transistor
b) collector current of first transistor is same as emitter current of second transistor
c) emitter current of first transistor is same as the collector current of the second transistor
d) none

14) resultant phase shift of odd no of CE amplifier stages at mid band frequency is a)
3600
b) 1800
c) 450
d) 900

15) major drawbacks of Darlington transistor pair is
a) low current gain compared to single emitter follower
b) dependence of AV on transistor selected condition
c) low i /p impedance compared to single emitter follower
d) dependence of h-parameters on quiescent point.

16) Resultant current gain of a Darlington pair individual current gain of hfe is
[d]
a) hfe/2
b) hfe
c) 2hfe
d) hfe2
ans: [D]

17) 2-stage rc coupled amplifier is configured as
[a]
a) 2 capacitively coupled CE stages cascaded
b) a CE stage capacitively coupled to a CC stage
c) 2 capacitively coupled CB stages cascaded.
d) 2 capacitively coupled CC stages cascaded
ans: [A]

18) 2-transistor cascade with both collectors tied together & emitter of the transistor connected to the base of the transistor is referred to as [a]
a) Darlington pair
b) CE &CC cascade
c) cascade amplifier
d) differential pair
ans: [A]

19) the i/p impedance of cascade amplifier is [b]
a) hic
b) hie
c) infinity
d) hib
ans: [B]

20) type of inter stage coupling resulting in highest overall gain
[c]
a) direct coupling
b)inductive coupling
c) RC coupling
d) transistor coupling
ans : [C]

21) main disadvantage of Darlington pair amplifier is
[d]
a) low i/p impedance
b) low current gain
c) high o/p impedance
d)high leakage current
ans: [D]

22) Major advantage of boot strap Darlington pair over single Darlington pair is
(a) High overall Av with proper DC biasing
(b) increased Ai irrespective of bias condition
(c) high i/p impedance irrespective of bias condition

(d) increased Ai depending upon the bias condition
Ans: (c)

Unit 2:

1) identify the correct relationship
a) f alpha ~ f beta
b) f beta >> f alpha
c) f alpha ~ ft
d) f alpha >> f beta

2) lower cutoff &higher cutoff frequency of rc coupled amplifier are
a) both zero
b) both infinity
c) zero & infinity respectively
d) similar to those of CE stage

3) voltage gain of an amplifier reduces to 1/(root 2)its max
a) break frequency
b) miller frequency
c) half power frequency
d) cutoff frequency

4) rce >> rbe condition is applicable in hybrid -pie equivalent of CE amplifier because
a) collector base junction is reverse biased & emitter base junction is forward biased
b) o/p R is always much larger than i/p R
c) b is the internal base terminal
d) base region is extremely tin compared to emitter & collector terminals

5) expression for short circuit current gain bandwidth
[d]
a) gm/2pie hfe (ce+cc)
b) gm/(ce+cc)
c) gm/ hfe (ce+cc)
d)gm/2pie (ce+cc)

6) identify the expression for voltage gain CE & fet amplifier at low frequency [c]
a) -gm rd Rl /(rd + Rl)
b) gm rd Rl / (rd +Rl+ gm rd Rl)
c) gm rd Rl /(rd + Rl)
d) Rl || rd / (1+ gm rd)

7) Resultant phase shift of even no of CB amplifier stage at frequency below lower cutoff frequency [d]
a) always a multiple of 2 pie

b) product of phase shift introduced by individual stages
c) always 1800
d) sum of the phase shifts introduced by individual stages

8) Identify the incorrect statement for a high frequency hybrid pie model of a BJT is [a]
a) high frequency hybrid pie capacitances can be expressed in terms of low frequency hparameters
b) capacitance between collector & base terminal of a BJT is called overlap -diode capacitance
c) ' B' represent internal base terminal
d) high frequency hybrid pie conductances can be expressed in terms of low frequency hparameters.
9) identify false statement [c]
a) fbeta & Ic exhibits a peak value of a particular ic.
b) unity gain band width Ft is the function of Ic
c)ft & Ic both are functions of f beta
d) Ft variation with Ic is similar to hfe variation with T
ans: [C]

10) during the mid band frequency the gain of amplifier is [d]
a) 1/(root 2) times Max value
b) min
c)unity
d) constant
ans: [D]

11) bandwidth of an amplifier with lower & higher cutoff frequency Fl & Fh .& quantity factor Qis [a]
a) Fh - F l
b) Fh/ q
c) (Fh-Fl)/1.414
d) q-Fl
ans: [A]

12) identify the expression for voltage gain CD & fet amplifier at low frequency
[b]
a) -gm rd Rl /(rd + Rl)
b) gm rd Rl / (rd +Rl+ gm rd Rl)
c) gm rd Rl /(rd + Rl)
d) Rl || rd / (1+ gm rd)
ans: [B]

13) the transconductance gm of a transistor depend on
[b]
a) temperature
b) operation frequency
c) CE voltage

d) C c
ans : [B]

14) ft for a ce amplifier is defined as
[b]
a) the frequency at which the CE current gain falls to half its Max value
b) frequency at which CE current gain becomes unity
c) frequency at which CE voltage gain falls to half its Max value
d) frequency at which CE voltage gain becomes unity
15) the capacitance determining the corner frequency lag network at the i/p of CE amplifier is
[b]
a) miller i/p capacitor
b) c wiring
c) external capacitor at the base
d)cbe
ans: [B]

16) if Av is the voltage gain of an amplifier in db & Ai is its current gain in db then power gain of
amplifier in db is [d]
a) Av- Ai
b) Av/ Ai
c)10log 10 Av/ Ai
d) Av+Ai
ans : [D]

17) at frequency below lower cut off frequency in CE amplifier coupling capacitor at the base of the amplifier form an LPF [b]
a) with emitter resistance
b) with i/p resistance
c) with o/p resistance
d) with base resistance
ans: [B]

18) advantage of impedance type inter stage coupling is
[c]
a) very wide band & frequency independent gain curve
b) flat response of frequency in mid band region
c) no dc voltage drop across collector load
d) no requirement of bulky components all frequency
ans: [C]

19) resultant phase shift of odd number of CE amplifier stages at mid band frequency is [b]
a) 3600
b)1800
c) 450

d) 900

20) lower cutoff & higher cut off frequency of an rc coupled amplifier are
[c]
a) both zero
b) both infinity
c) similar to of CE stage
d) zero& infinity
ans: [C]
21) higher cutoff frequency of transistor amplifier is mainly because of
[a]
a) inter electrode capacitance
b) bypass capacitance
c) blocking capacitance
d) coupling capacitance

22) ratio of slopes of the gain curve of an amplifier below lower cutoff frequency & above cutoff frequency is [b]
a) 3
b) unity
c)2
d) 6
ans: [B]

23) the capacitors that are short circuited at low frequencies in CE amplifier are
[d]
a) o/p coupling capacitors
b) i/p coupling capacitors
c) emitter bypass capacitors
d) inter electrode capacitor
ans:[B]

24) the critical capacitance that determines the overall cut off frequency of an amplifier is the one which sees an equivalent resistance [a]
a) of minimum value
b) of Max value
c) of infinity value
d) equals to its reactance value at that frequency
ans: [A]

25) distortion in amplifiers due to unequal amplitude gains at different frequencies is referred to as [c]
a) phase shift distortion
b) amplitude distortion
c) frequency distortion
d) delay distortion

ans : [C]

26) slope of the gain curve of an amplifier below cut off frequency is
[a]
a) -20 db decade
b) 6 db decade
c)-6 db decade
d) 20 db decade
ans : [A]
28) the CE short circuit current gain in db at frequency f = Ft is
[d]
a) hfe/1.414
b) unity
c) hfe
d)zero
ans: [D]

29). Phase difference between o/p and i/p voltages of a transistor amplifier at lower cut off frequencies is
a)180 b) 45 c) 0 d) 90
Ans: (b)

30) All frequencies below lower cut off frequency in a CE amplifier, the coupling capacitor at the base of the amplifier forms a LPF
a)with RE b)Rip c)RB d)Rop
Ans: (b)

31) Phase reversal between i/p & o/p signal voltages occurs in
a) common base amplifier
b) common drain amplifier
c) common gate amplifier
d) common source amplifier

32) FET amplifier configuration , which is similar to CC BJT is
[b]
a) common gate amplifier
b) common drain amplifier
c) common source amplifier
d) swamped source resistor amplifier
ans:[B]

33) phase difference between o/p voltage &i/p voltage of a CG amplifier at mid band frequencies
[b]
a) 1800
b) 00
c) 450

d) 900
ans : [B]

34) Voltage gain of a given CS FET depends on its
a)Dynamic drain resistance b)i/p impedance
c) Amplification factor d)Drain load resistance
Ans: (d)

35). Resultant phase shift of even no of CG amplifier stages at higher cut off frequencies is
Ans: Sum of phase shift introduced by individual stages.

36) Phase relationship between o/p and i/p voltage of a CS amplifier for frequency below lower cut-off frequency is
(a) both are in phase
(b) o/p lags i/p
(c) output leads i/p
(d) both are 180◦ out of phase
Ans: (c)

37). The phase relationship between output and input voltages of a CS amplifier for frequency above higher cut off frequency is
a) both are 180 degrees out of phase
b) output leads input
c) both are in phase
d) output lags input
Ans: (d)

Unit 3& 4:

1) Non-linear distortion is maximum in
a) class
B mode
b) class A mode
c) class AB mode
d) class C mode

2) final stage of multistage amplifier is generally a) a
pre-amplifier
b) a voltage post amplifier
c) a power amplifier
d) a microphone amplifier
3) Max conversion efficiency of a series fed class A power amplifier is
a) 75
b) 100
c) 50

d) 25
4) even harmonics are not present in the o/p of
a) class A transformer coupled amplifier
b) class c amplifier
c)class A amplifier
d) class B push pull amplifier

5) Even harmonics in the o/p are connected in push - pull configurations only if
[a]
a) both transistors are perfectly matched
b) both NPN & PNP transistors are used
c) A phase inversion is not used at inputs of 2 transistors
d) two power supplies are used
ans:[A]

6) i/p signals swing in class A power amplifier is restricted to
[d]
a) a small portion around Q point in active region
b) entire portion around Q point in saturation
c) entire portion around Q point in cutoff
d) entire portion around Q point in active
ans: [D]
7) transistor in class C amplifier is based beyond cutoff region to
[b]
a) ensure reduced distortion of o/p signal
b) ensure conduction angle of less than 1800
c) ensure conduction angle of transistor for entire i/p cycle
d) ensure o/p wave shape to the replica of i/p wave shape
ans: [B]

8) increased conversion efficiency in class B over class A operation is mainly due to
[b]
a) elimination of all higher harmonics
b) elimination of dc current in the load
c) usage of single power supply
d) elimination of cross over distortion
ans: [B]

9). The frequency at which CE is short circuit current gain becomes unity is represented by__fT_____
71. Non linear distortion is maximum in
a) Class B mode a) Class A mode
a) Class AB mode d) a) Class C mode
Ans: (b)

10). Even harmonics are not present in the o/p of Class B push pull amplifier.

11) Cross over distortion in class B amplifier is due to
(a) finite cut-off voltage of the two transistors
(b) non-identical behaviour of the two transistors
(c) elimination of two power supplies in the circuit
(d) elimination of even harmonics in the o/p
impedance

Unit 5

1. A parallel tuned circuit is also known as
a. matched circuit b. notch circuit
c. resonant circuit
d. anti resonant circuit

2. In tuned amplifiers equivalent circuits, the model used for transistor is a. hybrid - π
b. Thevinen's
c. y parameter d. z parameter

3. What factors govern the selectivity of a single tuned amplifier ?
a. resonant frequency and gain
b. quality factor and bandwidth
c. quality factor and gain d. gain and bandwidth

4. The harmonic distortion of an ideal tuned amplifier is
a. unity
b. zero
c. infinity
d. depends on tuned circuit

5. Higher quality factor of a single tuned amplifier provides a
a. higher selectivity and bandwidth b. smaller selectivity and bandwidth
c. higher selectivity and smaller bandwidth
d. smaller selectivity and higher bandwidth

6. The function of tuned circuit in Tuned Amplifier is
a. allows only dc signal
b. reject dc and allow all frequencies
c. selecting a particular frequency and rejecting all other frequencies
d. passing all frequencies

7. In tuned amplifiers, harmonic distortion is very small because, at these frequencies
a. the impedance is high and gain is low b. the impedance is low and gain is high
c. the impedance and gain of the amplifier becomes high
d. the impedance and gain of the amplifier becomes negligible

8. If the quality factor of a resonant circuit of tuned amplifier is doubled then the bandwidth is
a. doubled b. same
c. halved
d. zero

9. The Band width of an ideal tuned amplifier is
a. unity
b. zero
c. infinity
d. depends on tuned circuit

10. The drawbacks of a single tuned amplifier are
a. wider bandwidth and the sides of gain versus frequency curve are steeper
b. wider bandwidth and the sides of gain versus frequency curve are not steeper
c. narrow bandwidth and the sides of gain versus frequency curve are not steeper
d. narrow bandwidth and the sides of gain versus frequency curve are steeper

11. The tapping of inductance of tuned circuit of a tapped single tuned capacitance coupled amplifier
a. increases the impedance of resonant circuit b. increases the operating frequency
c. increases the resonant frequency
d. reduces the impedance of resonant circuit

12. In the tapped single tuned capacitance coupled amplifier the output voltage when the coil is tapped a. (1-n) times of the voltage developed across the complete coil
b. n times of the voltage developed across the complete coil c. same as the voltage developed across the complete coil
d. half of the voltage developed across the complete coil

13. Tapping in the LC tuned circuit is used to
a. reduce the impedance of the LC circuit to match the low impedance of the CE amplifier
b. increase the impedance of the LC circuit to match the low impedance of the CE amplifier c. reduce the impedance of the LC circuit to match the high impedance of the CE amplifier d. increase the impedance of the LC circuit to match the high impedance of the CE amplifier

15. The tapping point in a tapped single tuned capacitance coupled Amplifier divide the inductance L into two part such that
a. L1= 2L and L2 = L/2
b. L1= (n-1)L and L2 = (1-n)L
c. L 1=nL and L 2 = (1-n)L
d. L1=n/L and L2 = (1-n)/L

16. The gain bandwidth product of a single tuned capacitive couple amplifier is
a. depends on transconductance and independent on total input circuit capacitance
b. depends on both transconductance and total input circuit capacitance
c. independent on both transconductance and total input circuit capacitance

d. independent on transconductance and dependent on total input circuit capacitance

17. The LC tuned circuit of single tuned capacitive coupled amplifier is not connected between collector and ground because
b. inductor
c. transistor collector
d. capacitor

18. In a single tuned transformer coupled amplifier, the output is taken by
a. capacitive coupling b. inductive coupling c. resistive coupling
d. frequency coupling

19. The sharpness of the frequency response curve if the transformer coupled amplifier is depends on the
a. impedance of the tuned circuit
b. resonance frequency of tuned circuit c. the gain of the transistor
d. quality factor of the tuned circuit

20. In a single tuned transformer coupled amplifier the output of the tuned circuit is coupled to the next stage or
output device through a
a. resistor
b. inductor
c. transistor collector
b. single tuned resistive coupled amplifier
c. Inductively coupled amplifier
d. single tuned capacitive coupled amplifier

21. In a single tuned transformer coupled amplifier the matching between two stages is done by
a. coil tapping
b. using pad circuits
c. capacitively coupled circuit
d. the transformer turns ratio

22. In a single tuned transformer coupled amplifier, under conditions of maximum transform of power, total resistance appearing is shunt with the coil equals
a. R02
b. R0/2
c. R0
d. 2R0

20. Tutorial Problems (Classes)

UNIT 1:

- Classification of amplifiers& distortion in amplifiers.
- Analysis of CE, CB configurations with Hybrid model.
- Design of single stage amplifier using BJT.
- Miller's theorem its dual.
- Analysis of Cascaded RC coupled BJT amplifiers.
- Cascode amplifier& Darlington pair
- Different coupling schemes used in amplifiers.
- RC coupled, Transformer coupled& direct coupled amplifiers.

UNIT 2:

- Frequency response of single stage BJT amplifier.
- Effect of coupling &bypass capacitors on frequency response.
- The hybrid model at high frequencies.
- Gain bandwidth product.
- Small signal model of a MOS transistor.
- CS amplifier with resistive load using small signal model.
- CS amplifier with diode connected load using small signal model.
- CG cascode and folded cascode amplifier and its analysis using small signal model?

UNIT 3:

- The concept of feedback & advantages and disadvantages
- Classification of feedback amplifiers.
- Characteristics of negative feedback & its effect on amplifiers.
- Voltage series &shunt, current series& shunt feedback configurations.
- Classification of oscillators &conditions for oscillations.
- RC phase shift& Wien bridge oscillators.
- Generalized analysis of LC oscillators .
- Crystal oscillators.

UNIT 4:

- Classification of power amplifiers.
- Class A,B&AB power amplifiers.
- Efficiency of power amplifiers.
- Thermal runaway &heat sinks.

UNIT 5:

- Small signal Tuned amplifiers.
- Effect of cascading on B.W of tuned amplifiers.
- Stagger tuned amplifiers.
- Stability of tuned amplifiers.

21. Known gaps, if any and inclusion of the same in lecture schedule

1. Characteristics of MOS transistor to obtain small signal equivalent model
2. Concept of positive feedback its characteristics
3. Tuned circuits its working principle used in tuned amplifiers

22. Discussion topics if any

23. References, Journals, Websites and E-Links

Reference book names :

1. Electronic devices and circuit theory – Robert L.boylestad, Louis Nashelsky,2008 PE

2. Introductory Electronic devices and circuits – RobertT.paynter, 7 ed.,2009,PEL

3. Electronic circuit analysis-K.Lalkishore,2004,BSP

4. Electronic devices and circuits,DavidA.Bell -5 ed.,Oxford UniversityPress

5. Microelectronic circuits-Sedra and smith-5 ed.,2009, Oxford UniversityPress

6 .Integrated Electronics – Jacob Milliman and Christos C Halkias,1991 edu,2008.TMH

WEBSITES

1. en.wikipedia.org/wiki/Digital_electronics
2. www.modernelectronics.org
3. www.electronicsforyou.com
4. www.npteliitm.ac.in

Ebooks:

http://books.google.co.in/books?id=sxswmJgMbEsC&pg=PA118&lpg=PR16&ots=DXZAEipuZB&focus=viewport&dq=Pulse,+Digital+and+Switching+Waveforms+-+J.+Millman+and+H.+Taub#v=onepage&q=Pulse%2C%20Digital%20and%20Switching%20Waveforms%20-%20J.%20Millman%20and%20H.%20Taub&f=false

http://www.youtube.com/watch?v=aO6tA1z933k

24.Quality Control Sheets. a) Course end survey b) Teaching Evaluation

Hard copy will attach at the end of the course of course end survey and Teaching Evalution

25. STUDENT LIST:

ECE – 2-1A		
S.No	**Roll Number**	**Name of the Candidate**
1	14R11A0401	ADITYA B
2	14R11A0402	ADULLA JANARDHAN REDDY
3	14R11A0403	ANDE HEMANTH REDDY
4	14R11A0404	ANKATI NAVYA
5	14R11A0405	ASHFAQ AZIZ AHMED
6	14R11A0406	BANDI SANDHYA
7	14R11A0407	BASWARAJ SHASHANK YADAV
8	14R11A0408	BITLA SRIKANTH REDDY
9	14R11A0409	BUDDANA DHARANI KUMAR
10	14R11A0410	CHEBARTHI RAMYA GAYATHRI
11	14R11A0411	CHETLAPALLI NAGA SAI SUSHMITHA
12	14R11A0412	DASARI DHAMODHAR REDDY
13	14R11A0413	G AYESHA SULTANA
14	14R11A0414	G MADHURI
15	14R11A0415	G RISHI RAJ
16	14R11A0416	G VAMSHI KRISHNA
17	14R11A0417	G VENKATESH YADAV

18	14R11A0418	GONDA RISHIKA
19	14R11A0419	GUDE GOPI
20	14R11A0420	JAGGANNAGARI MANOJKUMAR REDDY
21	14R11A0421	JAGGARI SRINIJA REDDY
22	14R11A0422	JALAGAM NANDITHA
23	14R11A0423	JAMMIKUNTLA SHIVA CHARAN
24	14R11A0424	JATAPROLU LAKSHMI SOWMIKA
25	14R11A0425	JEKSANI SHREYA
26	14R11A0426	K VIJAY KUMAR
27	14R11A0427	KAALISETTY KRISHNA CHAITANYA
28	14R11A0428	KAKARLA MOUNICA
29	14R11A0429	KARRE PRIYANKA
30	14R11A0430	KL N SATYANARAYANA MURTHY
31	14R11A0431	KONDA KRITISH KUMAR
32	14R11A0432	KOPPULA RAHUL
33	14R11A0433	KURUGANTI RUNI TANISHKA SHARMA
34	14R11A0434	L THRILOK
35	14R11A0435	MANDULA SANTOSHINI
36	14R11A0436	MATLA PRINCE TITUS
37	14R11A0437	NARSETTI SAIPRAVALIKA
38	14R11A0438	NIKITHA RAGI
39	14R11A0439	P VIJAYA ADITYA VARMA
40	14R11A0440	PASHAM VIKRAM REDDY
41	14R11A0441	PELLURI KARAN KUMAR
42	14R11A0442	PERURI CHANDANA
43	14R11A0443	PODUGU SRUJANA DEVI
44	14R11A0444	RAJNISH KUMAR
45	14R11A0445	RAJU PAVANA KUMARI
46	14R11A0446	RAMIDI NITHYA
47	14R11A0447	RAMOJI RAJESH
48	14R11A0448	S ALEKHYA
49	14R11A0449	SARANGA SAI KIRAN
50	14R11A0450	SHAIK SAMEER ALI
51	14R11A0451	SOUMYA MISHRA
52	14R11A0452	SRIRAMOJU MANASA
53	14R11A0453	T ARUN KUMAR
54	14R11A0454	T S SANTHOSH KUMAR
55	14R11A0455	V BAL RAJ
56	14R11A0456	V POOJA
57	14R11A0457	V SRIVATS VISHWAMBER
58	14R11A0458	VEMI REDDY VISHNU VARDHAN REDDY

59	14R11A0459	VENNAMANENI VAMSI KRISHNA
60	14R11A0460	YERASI TEJASRI

ECE -2-1B

S.No	Roll Number	Name of the Candidate
1	14R11A0461	ADDAKULA SURESH
2	14R11A0462	AGARTI MADHU VIVEKA
3	14R11A0463	AKULA SAI KIRAN
4	14R11A0464	ANUMULA SNIGDHA
5	14R11A0465	B DIVYA
6	14R11A0466	B MANOHAR
7	14R11A0467	BANDARI MAMATHA
8	14R11A0468	BINGI DIVYA SUDHA RANI
9	14R11A0469	BIRE BHAVYA
10	14R11A0470	CH SAI BHARGAVI
11	14R11A0471	CHAVALI SUMA SIREESHA
12	14R11A0472	CHELLABOINA SHIVA KUMAR
13	14R11A0473	CHETTY AKHIL CHAND
14	14R11A0474	CHINTAPALLI MADHAV REDDY
15	14R11A0475	CHIVUKULA VENKATA SUBRAMANYA PRASANTH
16	14R11A0476	D NAGA SUMANVITHA
17	14R11A0477	D VAMSI
18	14R11A0478	DHARMENDER KEERTHI
19	14R11A0479	EADARA NAGA SIRISHA
20	14R11A0480	ERANKI SAI UDAYASRI ALAKANANDA
21	14R11A0481	GANGA STEPHEN RAVI KUMAR
22	14R11A0482	GUNDAM SHRUTHI
23	14R11A0483	GUNDREVULA SAMEERA
24	14R11A0484	K NAGA REKHA
25	14R11A0485	KANDADI VARSHA
26	14R11A0486	KURELLI SAI VINEETH KUMAR GOUD
27	14R11A0487	MADDIKUNTA SOMA SHEKAR REDDY
28	14R11A0488	MAMILLA SAI NISHMA
29	14R11A0489	MARELLA NAGA LASYA PRIYA
30	14R11A0490	MARKU VENKATESH
31	14R11A0491	MOHAMED KHALEEL
32	14R11A0492	MOHAMMED WASEEM AKRAM
33	14R11A0493	MOTURI DIVYA
34	14R11A0494	MUDIUM KOUSHIKA
35	14R11A0495	MYLAPALLI RAMBABU
36	14R11A0496	NAGU MOUNIKA
37	14R11A0497	NEELAM SNEHANJALI
38	14R11A0498	NIDAMANURI VENKATA VAMSI KRISHNA

39	14R11A0499	NIKHIL KUMAR N
40	14R11A04A0	ORUGANTI HARSHINI
41	14R11A04A1	PARAMKUSAM NIHARIKA
42	14R11A04A2	PASAM ABHIGNA
43	14R11A04A3	PATI VANDANA
44	14R11A04A4	PODISHETTY MANOGNA
45	14R11A04A5	PONAKA SREEVARDHAN REDDY
46	14R11A04A6	R NAVSHETHA
47	14R11A04A7	R PRANAY KUMAR
48	14R11A04A8	RAMIDI ROJA
49	14R11A04A9	RUDRA VAMSHI
50	14R11A04B0	S SHARAD KUMAR
51	14R11A04B1	SAGGU SOWMYA
52	14R11A04B2	TADELA SARWANI
53	14R11A04B3	THOTA SAI BHUVAN
54	14R11A04B4	VALLAPU HARIKRISHNA
55	14R11A04B5	VECHA PAVAN KUMAR
56	14R11A04B6	Y SAI VISHWANATH
57	14R11A04B7	ADHINARAYANAN SARITHA
58	14R11A04B8	PASUPULETI AVINASH
ECE – 2-1C		
S.No	**Roll Number**	**Name of the Candidate**
1	14R11A04B9	ANAMALI REETHIKA
2	14R11A04C0	ARUMILLI LEKYA
3	14R11A04C1	ARUMUGAM ASHWINI
4	14R11A04C2	BASAVARAJU MEGHANA
5	14R11A04C3	BEERAM TEJASRI REDDY
6	14R11A04C4	BHARAT SAKETH
7	14R11A04C5	BOMMANA HARIKADEVI
8	14R11A04C6	BYRAGONI ROJA
9	14R11A04C7	CANDHI SHASHI REKHA
10	14R11A04C8	CH RENUKA
11	14R11A04C9	CHAGANTI MOUNICA
12	14R11A04D0	CHITTARLA LOKESH GOUD
13	14R11A04D1	D LAVANYA
14	14R11A04D2	D MANIKANTA
15	14R11A04D3	DASARI VENKATA NAGA SAISH
16	14R11A04D4	DODDA MANOJ
17	14R11A04D5	E RAHUL CHOWDHARY
18	14R11A04D6	GOWRISHETTY VINEETHA
19	14R11A04D7	GUNTUPALLI RAVI TEJA

20	14R11A04D8	K L ANUSHA
21	14R11A04D9	K SASIDHAR
22	14R11A04E0	KANAKA RAMYA PRATHIMA
23	14R11A04E1	KASTURI SHIVA SHANKER REDDY
24	14R11A04E2	KODHIRIPAKA DHENUSRI
25	14R11A04E3	KOLA AISHWARYA
26	14R11A04E4	KONDOJU AKSHITHA
27	14R11A04E5	KOUDAGANI ALEKHYA REDDY
28	14R11A04E6	KUMMARIKUNTA PRASHANTH
29	14R11A04E7	KURVA SAI KUMAR
30	14R11A04E8	M AJAY KRISHNA
31	14R11A04E9	M MRIDULA GAYATRI
32	14R11A04F0	MANGALAPALLI SRAVANTHI
33	14R11A04F1	MERUGU PALLAVI
34	14R11A04F2	MITHIN VARGHESE
35	14R11A04F3	MOHD EESA SOHAIL
36	14R11A04F4	MUCHUMARI HARSHA VARDHAN REDDY
37	14R11A04F5	MUNUGANTI PRADHYUMNA
38	14R11A04F6	N DURGA RAJU
39	14R11A04F7	N SAKETH
40	14R11A04F8	N SANDHYA
41	14R11A04F9	NALLAGONI SRAVANTHI
42	14R11A04G0	P MANMOHAN SHASHANK VARMA
43	14R11A04G1	PRABHALA SRUTHI
44	14R11A04G2	PRAYAGA VENKATA SATHYA KAMESWARA PAV
45	14R11A04G3	R SAILESH
46	14R11A04G4	SAMBANGI POOJA
47	14R11A04G5	SAMEENA
48	14R11A04G6	SANGOJI SAI CHANDU
49	14R11A04G7	SURANENI NAMRATHA
50	14R11A04G8	TADAKAPALLY VIVEK REDDY
51	14R11A04G9	THUMUKUMTA VAMSHI TEJA
52	14R11A04H0	TIRUNAGARI SRAVAN KUMAR
53	14R11A04H1	TRIPURARI SOWGANDHIKA
54	14R11A04H2	TUNIKI MADHULIKA REDDY
55	14R11A04H3	U SAI MANASWINI
56	14R11A04H4	VAIDYA KEERTHI MALINI
57	14R11A04H5	VANGETI PRAVALLIKA
58	14R11A04H6	VASIREDDY VENKATA SAI
59	14R11A04H7	VELDURTHY SAI KEERTHI
60	14R11A04H8	WILSON DAVIES

ECE – 2-1D		
S.No	**Roll Number**	**Name of the Candidate**
1	14R11A04H9	A SHIRISHA
2	14R11A04J0	ABHIJEET KUMAR
3	14R11A04J1	ADULLA PRANAV REDDY
4	14R11A04J2	AINAPARTHI SAIVIJAYALAKSHMI SANDHYA
5	14R11A04J3	AMBATI SHIVA SAI
6	14R11A04J4	ANU PRASAD
7	14R11A04J5	B SAI APOORVA
8	14R11A04J6	B SRI KRISHNA SAI KIREETI
9	14R11A04J7	CHITTOJU LAKSHMI NARAYANAMMA
10	14R11A04J8	CHOWDARAPALLY SANTOSH KUMAR
11	14R11A04J9	D SAHITHI
12	14R11A04K0	DEVULAPALLI SAI CHAITANYA SANDEEP
13	14R11A04K1	DUSARI ANUSHA
14	14R11A04K2	GOLLAPUDI SRIKETH
15	14R11A04K3	GOLLIPALLY TEJASREE
16	14R11A04K4	GOUTE SHRAVAN KUMAR
17	14R11A04K5	GUDA PRATHYUSHA REDDY
18	14R11A04K6	JUNNU RAVALI
19	14R11A04K7	K DEVI PRIYANKA
20	14R11A04K8	KANDULA MANI
21	14R11A04K9	KARRA AVINASH
22	14R11A04L0	KASULA PRADEEP GOUD
23	14R11A04L1	KOMARAKUNTA SHASHANK
24	14R11A04L2	KOTHAKOTA PHANI RISHITHA
25	14R11A04L3	MADHADI NIKHIL KUMAR REDDY
26	14R11A04L4	MANDUMULA RAGHAVENDRA
27	14R11A04L5	MOHD HAMEED
28	14R11A04L6	MOHD SHAMS TABREZ
29	14R11A04L7	MORSU GANESH REDDY
30	14R11A04L8	MUKKERA VARUN
31	14R11A04L9	NAGULAPALLY MANOHAR REDDY
32	14R11A04M0	NAMBURI LAKSHMI MANJUSHA
33	14R11A04M1	NIROGI SURYA PRIYANKA
34	14R11A04M2	NUNE SAI CHAND
35	14R11A04M3	PALLETI SUSHMITHA
36	14R11A04M4	PANCHAYAT SHAMILI
37	14R11A04M5	POOSA JAI SAI NISHANTH
38	14R11A04M6	PRANAV RAJU A
39	14R11A04M7	RAYCHETTI CHANDRASENA

40	14R11A04M8	REBBA BHAVANI
41	14R11A04M9	S BHARATH SAGAR
42	14R11A04N0	S V M SURYA TEJASWINI
43	14R11A04N1	SAMA MANVITHA REDDY
44	14R11A04N2	SHAMALA MEGHANA
45	14R11A04N3	SMITHA KUMARI PATRO
46	14R11A04N4	T L SARADA RAMYA KAPARDHINI
47	14R11A04N5	T VINAY KUMAR
48	14R11A04N6	TABELA OMKAR
49	14R11A04N7	TADACHINA SAINATH REDDY
50	14R11A04N8	VANGA MOUNIKA
51	14R11A04N9	VARRI PRASHANTHI
52	14R11A04P0	VASARLA SAI TEJA
53	14R11A04P1	VISHWANATHAM ANUSHA
54	14R11A04P2	Y SRI SAI ADITYA
55	14R11A04P3	YAKKALA ASHIKA
56	14R11A04P4	YALAVARTHY MAHIMA
57	14R11A04P5	YALLAPRAGADA SAI TEJASRI
58	14R11A04P6	YARASI SAI RAMYA REDDY
59	14R11A04P7	S TARUN

DISCUSSION GROUPS:

ECE - A		
(Group – 1)		
S.No	**Roll Number**	**Name of the Candidate**
1	14R11A0401	ADITYA B
2	14R11A0402	ADULLA JANARDHAN REDDY
3	14R11A0403	ANDE HEMANTH REDDY
4	14R11A0404	ANKATI NAVYA
5	14R11A0405	ASHFAQ AZIZ AHMED
6	14R11A0406	BANDI SANDHYA

7	14R11A0407	BASWARAJ SHASHANK YADAV
8	14R11A0408	BITLA SRIKANTH REDDY
9	14R11A0409	BUDDANA DHARANI KUMAR
10	14R11A0410	CHEBARTHI RAMYA GAYATHRI
(Group – 2)		
11	14R11A0411	CHETLAPALLI NAGA SAI SUSHMITHA
12	14R11A0412	DASARI DHAMODHAR REDDY
13	14R11A0413	G AYESHA SULTANA
14	14R11A0414	G MADHURI
15	14R11A0415	G RISHI RAJ
16	14R11A0416	G VAMSHI KRISHNA
17	14R11A0417	G VENKATESH YADAV
18	14R11A0418	GONDA RISHIKA
(Group – 3)		
19	14R11A0419	GUDE GOPI
20	14R11A0420	JAGGANNAGARI MANOJKUMAR REDDY
21	14R11A0421	JAGGARI SRINIJA REDDY
22	14R11A0422	JALAGAM NANDITHA
23	14R11A0423	JAMMIKUNTLA SHIVA CHARAN
24	14R11A0424	JATAPROLU LAKSHMI SOWMIKA
25	14R11A0425	JEKSANI SHREYA
26	14R11A0426	K VIJAY KUMAR
27	14R11A0427	KAALISETTY KRISHNA CHAITANYA
(Group – 4)		
28	14R11A0428	KAKARLA MOUNICA
29	14R11A0429	KARRE PRIYANKA
30	14R11A0430	KL N SATYANARAYANA MURTHY
31	14R11A0431	KONDA KRITISH KUMAR
32	14R11A0432	KOPPULA RAHUL
33	14R11A0433	KURUGANTI RUNI TANISHKA SHARMA
34	14R11A0434	L THRILOK
35	14R11A0435	MANDULA SANTOSHINI
36	14R11A0436	MATLA PRINCE TITUS
37	14R11A0437	NARSETTI SAIPRAVALIKA
38	14R11A0438	NIKITHA RAGI
(Group – 5)		
39	14R11A0439	P VIJAYA ADITYA VARMA
40	14R11A0440	PASHAM VIKRAM REDDY
41	14R11A0441	PELLURI KARAN KUMAR
42	14R11A0442	PERURI CHANDANA
43	14R11A0443	PODUGU SRUJANA DEVI

44	14R11A0444	RAJNISH KUMAR
45	14R11A0445	RAJU PAVANA KUMARI
46	14R11A0446	RAMIDI NITHYA
47	14R11A0447	RAMOJI RAJESH
48	14R11A0448	S ALEKHYA
49	14R11A0449	SARANGA SAI KIRAN
(Group – 6)		
50	14R11A0450	SHAIK SAMEER ALI
51	14R11A0451	SOUMYA MISHRA
52	14R11A0452	SRIRAMOJU MANASA
53	14R11A0453	T ARUN KUMAR
54	14R11A0454	T S SANTHOSH KUMAR
55	14R11A0455	V BAL RAJ
56	14R11A0456	V POOJA
57	14R11A0457	V SRIVATS VISHWAMBER
58	14R11A0458	VEMI REDDY VISHNU VARDHAN REDDY
59	14R11A0459	VENNAMANENI VAMSI KRISHNA
60	14R11A0460	YERASI TEJASRI

ECE - B

(Group – 1)		
S.No	**Roll Number**	**Name of the Candidate**
1	14R11A0461	ADDAKULA SURESH
2	14R11A0462	AGARTI MADHU VIVEKA
3	14R11A0463	AKULA SAI KIRAN
4	14R11A0464	ANUMULA SNIGDHA
5	14R11A0465	B DIVYA
6	14R11A0466	B MANOHAR
7	14R11A0467	BANDARI MAMATHA
8	14R11A0468	BINGI DIVYA SUDHA RANI
9	14R11A0469	BIRE BHAVYA
(Group – 2)		
10	14R11A0470	CH SAI BHARGAVI
11	14R11A0471	CHAVALI SUMA SIREESHA
12	14R11A0472	CHELLABOINA SHIVA KUMAR
13	14R11A0473	CHETTY AKHIL CHAND
14	14R11A0474	CHINTAPALLI MADHAV REDDY

15	14R11A0475	CHIVUKULA VENKATA SUBRAMANYA PRASANTH
16	14R11A0476	D NAGA SUMANVITHA
17	14R11A0477	D VAMSI
18	14R11A0478	DHARMENDER KEERTHI
19	14R11A0479	EADARA NAGA SIRISHA
(Group – 3)		
20	14R11A0480	ERANKI SAI UDAYASRI ALAKANANDA
21	14R11A0481	GANGA STEPHEN RAVI KUMAR
22	14R11A0482	GUNDAM SHRUTHI
23	14R11A0483	GUNDREVULA SAMEERA
24	14R11A0484	K NAGA REKHA
25	14R11A0485	KANDADI VARSHA
26	14R11A0486	KURELLI SAI VINEETH KUMAR GOUD
27	14R11A0487	MADDIKUNTA SOMA SHEKAR REDDY
28	14R11A0488	MAMILLA SAI NISHMA
29	14R11A0489	MARELLA NAGA LASYA PRIYA
(Group – 4)		
30	14R11A0490	MARKU VENKATESH
31	14R11A0491	MOHAMED KHALEEL
32	14R11A0492	MOHAMMED WASEEM AKRAM
33	14R11A0493	MOTURI DIVYA
34	14R11A0494	MUDIUM KOUSHIKA
35	14R11A0495	MYLAPALLI RAMBABU
36	14R11A0496	NAGU MOUNIKA
37	14R11A0497	NEELAM SNEHANJALI
38	14R11A0498	NIDAMANURI VENKATA VAMSI KRISHNA
39	14R11A0499	NIKHIL KUMAR N
40	14R11A04A0	ORUGANTI HARSHINI
(Group – 5)		
41	14R11A04A1	PARAMKUSAM NIHARIKA
42	14R11A04A2	PASAM ABHIGNA
43	14R11A04A3	PATI VANDANA
44	14R11A04A4	PODISHETTY MANOGNA
45	14R11A04A5	PONAKA SREEVARDHAN REDDY
46	14R11A04A6	R NAVSHETHA
47	14R11A04A7	R PRANAY KUMAR
48	14R11A04A8	RAMIDI ROJA
(Group – 6)		
49	14R11A04A9	RUDRA VAMSHI
50	14R11A04B0	S SHARAD KUMAR
51	14R11A04B1	SAGGU SOWMYA
52	14R11A04B2	TADELA SARWANI

53	14R11A04B3	THOTA SAI BHUVAN
54	14R11A04B4	VALLAPU HARIKRISHNA
55	14R11A04B5	VECHA PAVAN KUMAR
56	14R11A04B6	Y SAI VISHWANATH
57	14R11A04B7	ADHINARAYANAN SARITHA
58	14R11A04B8	PASUPULETI AVINASH
ECE – 2-1C		
(Group – 1)		
S.No	**Roll Number**	**Name of the Candidate**
1	14R11A04B9	ANAMALI REETHIKA
2	14R11A04C0	ARUMILLI LEKYA
3	14R11A04C1	ARUMUGAM ASHWINI
4	14R11A04C2	BASAVARAJU MEGHANA
5	14R11A04C3	BEERAM TEJASRI REDDY
6	14R11A04C4	BHARAT SAKETH
7	14R11A04C5	BOMMANA HARIKADEVI
8	14R11A04C6	BYRAGONI ROJA
9	14R11A04C7	CANDHI SHASHI REKHA
(Group – 2)		
10	14R11A04C8	CH RENUKA
11	14R11A04C9	CHAGANTI MOUNICA
12	14R11A04D0	CHITTARLA LOKESH GOUD
13	14R11A04D1	D LAVANYA
14	14R11A04D2	D MANIKANTA
15	14R11A04D3	DASARI VENKATA NAGA SAISH
16	14R11A04D4	DODDA MANOJ
17	14R11A04D5	E RAHUL CHOWDHARY
18	14R11A04D6	GOWRISHETTY VINEETHA
19	14R11A04D7	GUNTUPALLI RAVI TEJA
20	14R11A04D8	K L ANUSHA
(Group – 3)		
21	14R11A04D9	K SASIDHAR
22	14R11A04E0	KANAKA RAMYA PRATHIMA
23	14R11A04E1	KASTURI SHIVA SHANKER REDDY
24	14R11A04E2	KODHIRIPAKA DHENUSRI
25	14R11A04E3	KOLA AISHWARYA
26	14R11A04E4	KONDOJU AKSHITHA
27	14R11A04E5	KOUDAGANI ALEKHYA REDDY
28	14R11A04E6	KUMMARIKUNTA PRASHANTH
29	14R11A04E7	KURVA SAI KUMAR
30	14R11A04E8	M AJAY KRISHNA

(Group – 4)		
31	14R11A04E9	M MRIDULA GAYATRI
32	14R11A04F0	MANGALAPALLI SRAVANTHI
33	14R11A04F1	MERUGU PALLAVI
34	14R11A04F2	MITHIN VARGHESE
35	14R11A04F3	MOHD EESA SOHAIL
36	14R11A04F4	MUCHUMARI HARSHA VARDHAN REDDY
37	14R11A04F5	MUNUGANTI PRADHYUMNA
38	14R11A04F6	N DURGA RAJU
39	14R11A04F7	N SAKETH
40	14R11A04F8	N SANDHYA
(Group – 5)		
41	14R11A04F9	NALLAGONI SRAVANTHI
42	14R11A04G0	P MANMOHAN SHASHANK VARMA
43	14R11A04G1	PRABHALA SRUTHI
44	14R11A04G2	PRAYAGA VENKATA SATHYA KAMESWARA PAV
45	14R11A04G3	R SAILESH
46	14R11A04G4	SAMBANGI POOJA
47	14R11A04G5	SAMEENA
48	14R11A04G6	SANGOJI SAI CHANDU
49	14R11A04G7	SURANENI NAMRATHA
50	14R11A04G8	TADAKAPALLY VIVEK REDDY
(Group – 6)		
51	14R11A04G9	THUMUKUMTA VAMSHI TEJA
52	14R11A04H0	TIRUNAGARI SRAVAN KUMAR
53	14R11A04H1	TRIPURARI SOWGANDHIKA
54	14R11A04H2	TUNIKI MADHULIKA REDDY
55	14R11A04H3	U SAI MANASWINI
56	14R11A04H4	VAIDYA KEERTHI MALINI
57	14R11A04H5	VANGETI PRAVALLIKA
58	14R11A04H6	VASIREDDY VENKATA SAI
59	14R11A04H7	VELDURTHY SAI KEERTHI
60	14R11A04H8	WILSON DAVIES
ECE – 2-1D		
(Group – 1)		
S.No	**Roll Number**	**Name of the Candidate**
1	14R11A04H9	A SHIRISHA
2	14R11A04J0	ABHIJEET KUMAR
3	14R11A04J1	ADULLA PRANAV REDDY
4	14R11A04J2	AINAPARTHI SAIVIJAYALAKSHMI SANDHYA
5	14R11A04J3	AMBATI SHIVA SAI

6	14R11A04J4	ANU PRASAD
7	14R11A04J5	B SAI APOORVA
8	14R11A04J6	B SRI KRISHNA SAI KIREETI
9	14R11A04J7	CHITTOJU LAKSHMI NARAYANAMMA
(Group – 2)		
10	14R11A04J8	CHOWDARAPALLY SANTOSH KUMAR
11	14R11A04J9	D SAHITHI
12	14R11A04K0	DEVULAPALLI SAI CHAITANYA SANDEEP
13	14R11A04K1	DUSARI ANUSHA
14	14R11A04K2	GOLLAPUDI SRIKETH
15	14R11A04K3	GOLLIPALLY TEJASREE
16	14R11A04K4	GOUTE SHRAVAN KUMAR
17	14R11A04K5	GUDA PRATHYUSHA REDDY
18	14R11A04K6	JUNNU RAVALI
19	14R11A04K7	K DEVI PRIYANKA
(Group – 3)		
20	14R11A04K8	KANDULA MANI
21	14R11A04K9	KARRA AVINASH
22	14R11A04L0	KASULA PRADEEP GOUD
23	14R11A04L1	KOMARAKUNTA SHASHANK
24	14R11A04L2	KOTHAKOTA PHANI RISHITHA
25	14R11A04L3	MADHADI NIKHIL KUMAR REDDY
26	14R11A04L4	MANDUMULA RAGHAVENDRA
27	14R11A04L5	MOHD HAMEED
28	14R11A04L6	MOHD SHAMS TABREZ
29	14R11A04L7	MORSU GANESH REDDY
(Group – 4)		
30	14R11A04L8	MUKKERA VARUN
31	14R11A04L9	NAGULAPALLY MANOHAR REDDY
32	14R11A04M0	NAMBURI LAKSHMI MANJUSHA
33	14R11A04M1	NIROGI SURYA PRIYANKA
34	14R11A04M2	NUNE SAI CHAND
35	14R11A04M3	PALLETI SUSHMITHA
36	14R11A04M4	PANCHAYAT SHAMILI
37	14R11A04M5	POOSA JAI SAI NISHANTH
38	14R11A04M6	PRANAV RAJU A
39	14R11A04M7	RAYCHETTI CHANDRASENA
(Group – 5)		
40	14R11A04M8	REBBA BHAVANI
41	14R11A04M9	S BHARATH SAGAR
42	14R11A04N0	S V M SURYA TEJASWINI

43	14R11A04N1	SAMA MANVITHA REDDY
44	14R11A04N2	SHAMALA MEGHANA
45	14R11A04N3	SMITHA KUMARI PATRO
46	14R11A04N4	T L SARADA RAMYA KAPARDHINI
47	14R11A04N5	T VINAY KUMAR
48	14R11A04N6	TABELA OMKAR
49	14R11A04N7	TADACHINA SAINATH REDDY
(Group – 6)		
50	14R11A04N8	VANGA MOUNIKA
51	14R11A04N9	VARRI PRASHANTHI
52	14R11A04P0	VASARLA SAI TEJA
53	14R11A04P1	VISHWANATHAM ANUSHA
54	14R11A04P2	Y SRI SAI ADITYA
55	14R11A04P3	YAKKALA ASHIKA
56	14R11A04P4	YALAVARTHY MAHIMA
57	14R11A04P5	YALLAPRAGADA SAI TEJASRI
58	14R11A04P6	YARASI SAI RAMYA REDDY
59	14R11A04P7	S TARUN