PDC

COURSE FILE

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Geethanjali College of Engineering and Technology

DEPARTMENT OF ELECTRONICS & COMMUNICATIONS

(Name of the Subject/Lab Course) : Pulse & Digital Circuits

(JNTU CODE: A40415   )   **Programme : UG**

Branch: ECE	**Version No : 4**
Year: II	**Document Number : GCET/ECE/**
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3) Design :	**3) Design :**
4) Date :	**4) Date :**

Approved by (HOD) :

 1) Name :

 2) Sign   :

 3) Date :

JAWAHARLAL NEHRU TECHNOLOGIVAL

UNIVERSITY HYDERABAD

Objective:

II Year B.Tech. ECE -II Sem   **T   P C**   **4+1* 0 4**

Pulse and Digital Circuits (PDC)

UNIT I

LINEAR WAVE SHAPING

High pass and low pass RC circuits and their response for sinusoidal, step, pulse, square and ramp inputs. High pass RC network as differentiator, Low pass RC network as an integrator, Attenuators and its application as a CRO probe, RL and RLC circuits and their response for step input, Ringing circuit.

UNIT II

NON-LINEAR WAVE SHAPING

Diode clippers, Transistor clippers, clipping at two independent levels, Comparators, Applications of Voltage Comparators, Clamping operation, Clamping circuit taking Source and Diode resistance into account, Clamping circuit theorem, Practical clamping circuits, Effect of diode characteristics on clamping Voltage, Synchronized Clamping.

UNITIII

SWITCHING CHARACTERISTICS OF DEVICES

Diode as a switch, Piecewise linear diode characteristics, Diode Switching times, Transistor as a Switch, Break down voltages, Transistor in saturation, Temperature variation of saturation parameters, Transistor-switching times, Silicon Controlled switch circuits.

SAMPLING GATES

Basic operating principles of sampling gates, Unidirectional and Bi-directional sampling gates, Four Diode Sampling Gate, Reduction of pedestal in Gate Circuits, Six Diode Gate, Applications of sampling gates.

UNIT IV

MULTIVIBRATORS

Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt trigger using transistors.

TIME BASE GENERATORS

General features of a time base signal, methods of generating time base waveform, Miller and Bootstrap time base generators – Basic Principles, Transistor Miller Time Base Generator, Transistor Bootstrap Time Base Generator, Current Time Base Generators, Methods of Linearity improvement.

UNIT V

SYNCHRONIZATION AND FREQUENCY DIVISION

Pulse Synchronization of Relaxation Devices, Frequency division in Sweep Circuit, Stability of Relaxation devices, Astable Relaxation circuits, Monost Transistors able relaxation circuits, Synchronization of a sweep circuit with symmetrical signals, Sine wave frequency division with a sweep circuit, A Sinusoidal Divider using Regeneration and Modulation

REALIZATION OF LOGIC GATES USING DIODES & TRANSISTORS

AND, OR and NOT gates using Diodes and Transistors, DCTL, RTL, DTL, TTL and CML Logic Families and its Comparison.

TEXT BOOKS

1. Millman's Pulse, Digital and Switching Waveforms - J. Millman, H. Taub and Mothiki S Prakash Rao, 2nd ed. 2008, TMH
2. Solid State Pulse circuits - David A. Bell, , 4th Edn.., 2002 . PHI

REFERENCES

a. Pulse and Digital Circuits –A. Anand Kumar, 205, PHI.
b. Fundamentals of Pulse and digital Circuits – Ronald J Tocci, 3 ed., 2008
c. Pulse and digital Circuits – Motheki S Prakash Rao, 2006, TMH.
d. Wave Generation and Shaping - L. Strauss.

3. VISION OF THE DEPARTMENT

Vision of the Department

To impart quality technical education in Electronics and Communication Engineering emphasizing analysis, design/synthesis and evaluation of hardware/ embedded software, using various Electronic Design Automation (EDA) tools with accent on creativity, innovation and research thereby producing competent engineers who can meet global challenges with societal commitment.

4. MISSION OF THE DEPATMENT

Mission of the Department

➢ To impart quality education in fundamentals of basic sciences, mathematics, electronics and communication engineering through innovative teaching-learning processes.

➢ To facilitate Graduates define, design, and solve engineering problems in the field of Electronics and Communication Engineering using various Electronic Design Automation (EDA) tools.

- To encourage research culture among faculty and students thereby facilitating them to be creative and innovative through constant interaction with R & D organizations and Industry.

- To inculcate teamwork, imbibe leadership qualities, professional ethics and social responsibilities in students and faculty.

5. PEO's and PO's

Program Educational Objectives of B. Tech (ECE) Program

- ❖ PEO-1:To prepare students with excellent comprehension of basic sciences, mathematics and engineering subjects facilitating them to gain employment or pursue higher studies with an appreciation for lifelong learning.

- ❖ PEO-2:To train students with problem solving capabilities such as analysis and design with adequate practical skills wherein they demonstrate creativity and innovation that would enable them to develop state of the art equipment and technologies of multidisciplinary nature for societal development.

- ❖ PEO-3:To inculcate positive attitude, professional ethics, effective communication and interpersonal skills which would facilitate them to succeed in the chosen profession exhibiting creativity and innovation through research and development both as team member and as well as leader.

PROGRAM OUTCOMES (ECE)

1.An ability to apply knowledge of Mathematics, Science, and Engineering   to solve complex engineering problems of Electronics and Communication Engineering systems.

2.An ability to model, simulate and design Electronics and Communication Engineering systems, conduct experiments, as well as analyze and   interpret data and prepare a report with conclusions.

3.An ability to design an Electronics and Communication Engineering system, component, or process to meet desired needs within the realistic constraints such as economic, environmental, social, political, ethical, health and safety, Manufacturability and sustainability.

4.An ability to function on multidisciplinary teams involving interpersonal skills.

5.An ability to identify, formulate and solve engineering problems of multidisciplinary nature.

6.Understanding of professional and ethical responsibilities involved in the practice of Electronics and Communication Engineering profession.

7.Ability to communicate effectively with a range of audience on complex engineering problems of multidisciplinary nature both in oral and written form.

8.The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental and societal context.

9.Recognition of the need for, and an ability to engage in life-long learning and acquire the capability for the same.

10.Knowledge of contemporary issues involved in the practice of Electronics and Communication Engineering profession

11.An ability to use the techniques, skills and modern engineering tools necessary for engineering practice.

12.An ability to use modern Electronic Design Automation (EDA) tools, software and electronic equipment to analyze, synthesize and evaluate Electronics and Communication Engineering systems for multidisciplinary tasks.

13.Apply engineering and project management principles to one's own work and also to manage projects of multidisciplinary nature.

6. Course objectives and Outcomes

COURSE OBJECTIVES:

The main objectives of this course are:
CO 1: Understand the applications of diode as Integrator, differentiator, clippers, clamper circuits.
CO 2: Learn various switching devices such as diode, transistor, SCR.
CO 3: Difference between logic gates and sampling gates.
CO 4: Design Multivibrators for various applications, synchronization techniques and sweep circuits.
CO 5: Realize logic gates using diodes and transistors.

COURSE OUTCOMES:

At the end of the course, the student will be able to:
CO1: Understand the applications of diode as Integrator, differentiator, clippers, clamper circuits.
CO2: Learn various switching devices such as diode, transistor, SCR.
CO3: Difference between logic gates and sampling gates
CO4: Design Multivibrators for various applications, synchronization techniques and sweep circuits
CO5: Realize logic gates using diodes and transistors.

7. Brief notes on the importance of the course and how it fits into the curriculum

This is the basic course for electronic engineers to understand the behavior of active and passive devices and circuit configurations used for the generation and processing of pulse, digital and switching waveforms. These non-sinusoidal signals find extensive application in fields such as computers, control systems, counting and timing systems, data-processing systems, digital instrumentation ,pulse communication, radar, telemetry, television and in many areas of experimental research. By studying this course students can understand better the courses in their future semesters such as control systems, IC Applications and Microprocessor and Microcontrollers.

8. Prerequisites if any

The following subject's knowledge is required for understanding the PDC course.

1.Electronic Devices and Circuits 2.Electric Circuits   3. STLD.

9. Instructional Learning Outcomes

Instructional objectives and learning outcomes

Instructional Unit-wise objectives

1. To study and analyze linear wave shaping circuits such as R-C and R-L-C transient circuits .
2. To study and analyze non-linear wave shaping circuits such as clippers, clampers and comparators.
3. To study the switching characteristics of diode, transistor and SCR.
4. To study the operating principles of various sampling gates.
5. To design and analyze various multivibrators using transistors.
6. To design and analyze time base generators
7. To design and analyze various sweep circuits.
8. To discuss and realize logic gates using diodes and transistors

Instructional objectives
Unit 1: Linear Wave Shaping

- To study about linear wave shaping circuits and Non-linear wave shaping circuits for different input signals.
- To describe the application of a low pass circuit as an integrator.
- To understand the principles of working of uncompensated and compensated attenuators and the operation of the attenuator circuit in CRO probe.

- To derive the response of high pass RC, RL and RLC circuits to different types of inputs like Sinusoidal, pulse, step, square, ramp and exponential inputs.
- To describe the application of high pass circuit as Differentiator.
- To understand the operation of the ringing circuit.

Unit 2: Non-linear Wave Shaping

- To study the principle of operation of various series and shunt clipping circuits
- To study about diode comparators and double differentiators as amplitude comparators and it's applications .
- To study the principle of operation of various clamping circuits and verify the clamping circuit theorem.
- To derive the necessary relations to plot steady state output.
- To describe the effect of diode characteristics on the clamping voltage.
- To describe synchronized clamping.

Unit 3: Switching characteristics of Devices:

- To study the principle of operation of diodes and transistors as switches.
- To study the effect of inter-electrode capacitances on switching times.
- To study the switching times of devices and derive the necessary relations.
- To study the temperature dependence of the transistor on various parameters.
- To understand the use of transistor switch as latch.
- To realize the use of transistor switches with inductive and capacitive loads.
- To study the principle of operation of switching circuits using SCS.
- To understand the working of unidirectional and bidirectional sampling gates and their variations
- To understand the working of sampling gates using Diodes (two, four and six) and transistors.
- To realize the applications of sampling gates in sampling scope
- To derive a choppers stabilized amplifier using sampling gates

Unit 4: Multivibratos

- To study the principle of operation of the multivibrators.
- To study the applications of multivibrators.
- To realize the need for a commutating condenser in a monostable multivibrator and bistable multivibrator.
- To study the principle of operation of Time base generators
- To study the features of the Time base signal.
- To study the principle of operation of Miller Time base
- To study the principle of operation of Bootstrap Time base generator
- To study the principle of operation of UJT saw tooth generator.
- To study the principle of operation of time base generators using Op-Amps.

Unit 5: Synchronization and frequency division

- To study the operation of synchronization and frequency division circuits..
- To describe the methods of achieving frequency synchronization and division in other relaxation circuits like astable and monostable multivibratos
- To realize the circuit that eliminates jitter in a relaxation divider
- To understand the principle of operation of the circuits that achieve frequency synchronization and division using symmetric circuits

Realization of logic gates using Diodes and Transistors

- To understand the principle of operation of basic logic gates like AND, OR and NOT gates

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- To implement these gates using Diodes and Transistors
- To understand the various logic families like DCTL, RTL, DTL, TTL and CML and their comparison
- To implement simple Boolean functions using different logic families.

Student Learning Outcomes

Unit 1: Linear Wave Shaping

After completing this unit, the students are able to
- Design linear wave shaping circuits using linear elements like R C and L.
- Derive the expressions and plot the response of low pass RC circuits to different types of inputs namely sinusoidal, step, pulse, square-wave, exponential and ramp.
- Describe the application of a low pass circuit as an integrator.
- Understand the principles of working of uncompensated and compensated attenuators and the operation of the attenuator circuit in CRO probe.
- Derive the response of high pass RC and RL circuits to different types of inputs like Sinusoidal, pulse, step, square, ramp and exponential inputs.
- Describe the application of high pass circuit as Differentiator.
- Understand the operation of the ringing circuit.
- Find the response of RL and RLC circuits to step input.

Unit 2: Non-linear Wave Shaping

After completing this unit, the students are able to
- Design various series and shunt clipping circuits and their combinations.
- Understand the principle of operation of two level emitter coupled transistor clippers and noise clippers
- Describe simple diode comparators and double differentiators as amplitude comparators.
- Explain the applications of comparators.
- Design various clamping circuits and verify the clamping circuit theorem.
- Derive the necessary relations to plot steady state output.
- Describe the effect of diode characteristics on the clamping voltage.
- Describe synchronized clamping.
- State and derive the clamping circuit theorem

Unit 3: Switching characteristics of Devices and sampling gates

After completing this unit, the students are able to
- Use diodes and transistors as switches.
- Describe the effect of inter-electrode capacitances on switching times.
- Describe the switching times of devices and derive the necessary relations.
- Describe the temperature dependence of the transistor on various parameters.
- Understand the use of transistor switch as latch.
- Realize the use of transistor switches with inductive and capacitive loads.
- Design switching circuits using SCS.
- Understand the working of unidirectional and bidirectional sampling gates and their variations
- Design sampling gates using Diodes (two, four and six) and transistors.
- Describe the output by adjusting the levels of the control signal
- Realize the applications of sampling gates in sampling scope
- Derive a choppers stabilized amplifier using sampling gates

Unit 4: Multivibratos & Time Base Generators

After completing this unit, the students are able to
- Explain the principle of operation of the multivibrators.
- Analyze and design Bistable, Monostable and Astable multivibrators and able to calculate and frequency / pulse width of the generated signal.
- Plot the waveforms at various points in the circuit.
- Describe the emitter coupled astable multivibrators
- Use an astable multivibrator for applications such as voltage to frequency converter and frequency modulator
- Understand the working of emitter coupled monostable multivibrator
- Realize the need for a commutating condenser in a monostable multivibrator and bistable multivibrator.
- Realize the application of a monostable multivibrator as a voltage to time converter
- Analyze fixed bias and self bias bistable multivibrators
- Analyze and design emitter coupled bistable multivibrator, also called Schmitt trigger
- Describe the applications of bistable multivibrator circuits.
- Able to design different types of Time base generators
- Explain the features of the Time base signal.
- Design Miller Time base Generator and explain the principle of operation.
- Design Bootstrap Time base generator and explain the principle of operation.
- Design UJT saw tooth generator.
- Design current Time base generator.
- Design time base generators using Op-Amps.

Unit 5: Synchronization and frequency division & Realization of logic gates using Diodes and Transistors

After completing this unit, the students are able to
- Understand the principle of frequency synchronization using exponential methods like UJT relaxation oscillator circuit.
- Describe the methods of achieving frequency synchronization and division in other relaxation circuits like astable and monostable multivibratos
- Realize the circuit that eliminates jitter in a relaxation divider
- Understand the principle of operation of the circuits that achieve frequency synchronization and division using symmetric circuits
- Understand the principle of operation of basic logic gates like AND, OR and NOT gates
- Implement these gates using Diodes and Transistors
- Understand the various logic families like DCTL, RTL, DTL, TTL and CML and their comparison
- Able to implement simple Boolean functions using different logic families.

10. Course mapping with PEOS and POs

POs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Pulse and Digital circuits														
CO 1: Understand the applications of diode as Integrator, differentiator, clippers, clamper	**2**	**2**	**2**		**2**			**1**	**1**		**2**			**1**

circuits.													
CO 2: Learn various switching devices such as diode, transistor, SCR.	2	2	2		2			1	1		2		2
CO 3: Difference between logic gates and sampling gates	2	2	2		2			1	2		2		2
CO 4: Design Multivibrators for various applications, synchronization techniques and sweep circuits	1	2	2		2			1	2		2		2
CO 5: Realize logic gates using diodes and transistors.	1	2	2		2			1	2		2		2

Mapping of Course with Programme Educational Objectives: (Sample)

S.No	Course component	code	course	Semester	PEO 1	PEO 2	PEO 3
1	Basic Electronics	A40415	Pulse and Digital circuits	2	√	√	

11. Time table of concerned class

Department of Electronics & Communication Engineering								
Year/Sem/Sec: II-B. Tech-I Sem-A Section				Room no.: LH-15			Acad Year 2014-15, WEF: 29-12-2014	
Class Incharge:								
Time	09.30-10.20	10.20-11.10	11.10-12.00	12.00-12.50	12.50-13.30	13.30-14.20	14.20-15.10	15.10-16.00
Period	1	2	3	4		5	6	7
Monday					LUNCH			
Tuesday								
Wednesday								
Thursday								
Friday								
Saturday								
No	**Subject(T/P)**			**Faculty Name**			**Subject Code**	**Periods/Week**
1								
2								

3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				

Year/Sem/Sec: II-B.Tech-I Sem-		D Section		Room no: LH-18			Acad Year 2014-15, WEF: 29-12-2014	
Class Incharge:								
Time	09.30-10.20	10.20-11.10	11.10-12.00	12.00-12.50	12.50-13.30	13.30-14.20	14.20-15.10	15.10-16.00
Period	1	2	3	4		5	6	7
Monday					LUNCH			
Tuesday								
Wednesday								
Thursday								
Friday								
Saturday								

No	Subject(T/P)	Faculty Name	Subject Code	Periods/Week
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

11									
12									
13									

* represents Tutorial classes

12. Individual time table

Work Load:			W.E.F:						
Day/Hour	**I**	**II**	**III**	**IV**		**V**	**VI**	**VII**	
MON									
TUE					LUNCH				
WED									
THU									
FRI									
SAT									

 PDC-II ECE- 2-2 A&D

13 .Lecture schedule with methodology being used/adopted

Department of   **Electronics & Communications Engineering**

Year & Semesters to who subject is offered   **II-II ECE (A, B,C & D)**

Name of the Subject: **Pulse and Digital and Circuits**

Name of the Faculty: **Prof. K.Somasekhara Rao** Designation: **Dean of Academics**   Department: **ECE-section B**

Name of the Faculty: **M.Muthamma** Designation: **Assistant Professor**   Department: **ECE section-C**

Name of the Faculty: **V.Venkata lakshmi**   Designation: **Assistant Professor**   Department: **ECE section-A**

Name of the Faculty: **Subrahmanyam** Designation: **Assistant Professor**   Department: **ECE section-D**

13.1   Introduction to the Subject

   This is the basic course for electronic engineers to understand the behavior of active and passive devices and circuit configurations used for the generation and processing of pulse, digital and switching waveforms.

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These non-sinusoidal signals find extensive application in fields such as computers, control systems, counting and timing systems, data-processing systems, digital instrumentation ,pulse communication, radar, telemetry, television and in many areas of experimental research.

13.2 JNTU Syllabus with additional topics

S.No.	Unit No.	Topic	Additional Topics
1	I	**Linear wave shaping:** High pass, low pass RC circuits	**CRO operation and CRO probes**
		High pass RC circuit response for sinusoidal and step inputs	
		High pass RC circuit response for ramp, pulse and square inputs	
		Low pass RC circuit response for sinusoidal and step inputs	
		Low pass RC circuit response for ramp, pulse and square inputs	
		High pass RC as an Differentiator and Low pass circuit as Integrator	
		RL and RLC circuits and their response for step input, Ringing circuit.	
		Attenuators and its application as a CRO Probe	
2	II	**Non-linear wave shaping:** Diode series clippers	
		Diode parallel clippers	
		Clipping at two independent levels	
		Comparators, applications of voltage comparators	
		Clamping operation	
		Clamping circuit taking Source and Diode resistance into account	
		Clamping circuit theorem, practical clamping circuits	
		Effect of diode characteristics on clamping voltage, Synchronized Clamping	
3	III	<u>**Switching characteristics of Devices:**</u> Diode as a switch, piecewise linear diode characteristics	
		Diode Switching times	
		Transistor as a switch	
		Break down voltage consideration of transistor	

		Saturation parameters of Transistor and their variation with temperature	
		Transistor switching times and Silicon controlled switch circuits	
**MID-I**		
	III	**Sampling gates:** Basic operating principles of sampling gates	
		Unidirectional and Bi-directional sampling gates	
		Four diode and Six diode sampling gate	
		Reduction of pedestal in gate circuits and Applications of sampling gate	
4	**IV**	**Multivibrators:** Analysis of Bistable Multivibrator	
		Design of Bistable Multivibrator	
		Analysis of Mono stable Multivibrator	
		Design of Mono stable Multivibrator	
		Analysis of Astable Multivibrator	
		Design of Astable Multivibrator	
		Applications of Multivibrators	
		Triggering methods	
		Schmitt trigger	
		Design Problems solving	
		Time base generators: General features of a time base signal, methods of generating time base waveform	
		Miller and Bootstrap time base generators – basic principle	
		Transistor miller time base generator	
		Transistor Bootstrap time base generator	
		UJT saw tooth wave generator	
		Current time base generators	
		Methods of linearity improvement	
5	**V**	**Synchronization and frequency division:** Pulse Synchronization of Relaxation Devices	**CMOS and Bi-CMOS logic family**
		Frequency division in sweep circuit, Stability of Relaxation Devices	

		Astable relaxation circuits, Monostable relaxation circuits	
		Synchronization of a sweep circuit with symmetrical signals	
		Sine wave frequency division with a sweep circuit	
		Realization of logic gates using Diodes and Transistors: AND, OR gates using Diodes	
		AND, OR gates using Transistors	
		DCTL,RTL	
		DTL, TTL	
		CML logic families and its comparison	

13.3.   Source of Information

13.3.1 TEXT BOOKS:

Suggested Text Books

1. Millman's Pulse, Digital and Switching Waveforms - J. Millman and H. Taub and Mothiki S .Prakash Rao, 2 ed.,2008, TMH.
2. Solid State Pulse circuits - David A. Bell, PHI, 4th Edn., 2002 PHI.

   Reference Books:

13.3.2 REFERENCE BOOKS:

   13.3.2.1   Pulse and Digital Circuits – A Anand Kumar, 2005, PHI

   13.3.2.2   Fundamentals of Pulse and Digital Circuits – Ronald Tocci, 3rd Ed, 2008

   13.3.2.3   Pulse and Digital circuits – Mothiki S Prakash Rao, 2006 TMH

   13.3.2.4   Wave generation and Shaping – L Strauss

13.3.3 WEBSITES

1. en.wikipedia.org/wiki/Digital_electronics
2. www.modernelectronics.org
3. www.electronicsforyou.com
4. www.npteliitm.ac.in

13.3.4 E-books

1. http://www.youtube.com/watch?v=aO6tA1z933k
2. http://books.google.co.in/books?id=sxswmJgMbEsC&pg=PA118&lpg=PR16&ots=DXZAEipuZB&focus=viewport&dq=Pulse,+Digital+and+Switching+Waveforms+-+J.+Millman+and+H.+Taub#v=onepage&q=Pulse%2C%20Digital%20and%20Switching%20Waveforms%20-%20J.%20Millman%20and%20H.%20Taub&f=false

13.3.5. JOURNALS

1.Nonsymmetric multivibrators with an auxiliary RC-circuit Filanovsky, I.M.; Piskarev, V.A.; Stromsmoe, K.A. Electronic Circuits and Systems, IEE Proceedings G

Volume: 131 , Issue: 4 Topic(s):   Digital Object Identifier: 10.1049/ip-g-1:19840029

Publication Year: 1984 , Page(s): 141 - 146

2.Combining 2-level logic families in grid-based nanoscale fabrics Teng Wang; Narayanan, P.; Moritz, C.A. Nanoscale Architectures, 2007. NANOSARCH 2007. IEEE International Symposium on

Topic(s): Components, Circuits, Devices & Systems

3.**Stability analysis of a digitally based HVDC firing-pulse synchronization control**

Larsen, E.V.; Clark, K.; Lorden, D.J.

Power Delivery, IEEE Transactions on

13.4 MICRO PLAN:

Sec –A

S.No.	Unit No.	Total no. of Periods	Date	Topic to be covered in one lecture	Reg/Additional	Teaching aids used	Remarks

						LCD/ OHP/ BB	
1	I	10		**Linear wave shaping:** High pass, low pass RC circuits	**Regular**	**BB**	
2				High pass RC circuit response for sinusoidal and step inputs	**Regular**	**BB**	
3				High pass RC circuit response for ramp, pulse and square inputs	**Regular**	**BB**	
4				Low pass RC circuit response for sinusoidal and step inputs	**Regular**	**BB**	
5				Low pass RC circuit response for ramp, pulse and square inputs	**Regular**	**BB**	
6				High pass RC as an Differentiator and Low pass circuit as Integrator	**Regular**	**BB**	
7				RL and RLC circuits and their response for step input, Ringing circuit. Attenuators and its application as a CRO Probe	**Regular**	**BB**	
8				CRO operation and CRO probes	**Additional**	**Video lecture**	
9				Tutorial	**Regular**	**BB**	
10				Assignment Test		**BB**	
11	II	10		**Non-linear wave shaping:** Diode series clippers	**Regular**	**BB/OHP**	
12				Diode parallel clippers	**Regular**	**BB/ OHP**	
13				Clipping at two independent levels	**Regular**	**BB/ OHP**	
14				Comparators, applications of voltage comparators	**Regular**	**BB**	
15				Clamping operation	**Regular**	**BB**	
16				Clamping circuit taking Source and Diode resistance into account	**Regular**	**BB**	
17				Clamping circuit theorem, practical clamping circuits	**Regular**	**BB**	

18				Effect of diode characteristics on clamping voltage, Synchronized Clamping	**Regular**	**BB/ OHP**	
19				Tutorial	**Regular**	**BB**	
20				Assignment Test		**BB**	
21	**III**	**11**		**<u>Switching characteristics of Devices:</u>** Diode as a switch, piecewise linear diode characteristics	**Regular**	**BB**	
22				Diode Switching times	**Regular**	**BB**	
23				Transistor as a switch, Break down voltage consideration of transistor	**Regular**	**BB**	
24				Saturation parameters of Transistor and their variation with temperature	**Regular**	**BB**	
25				Transistor switching times and Silicon controlled switch circuits	**Regular/ OHP**	**BB**	
26				**MID-I**			
27	**III**			**Sampling gates:** Basic operating principles of sampling gates	**Regular**	**BB/O HP**	
28				Unidirectional and Bi-directional sampling gates	**Regular**	**BB**	
29				Four diode and Six diode sampling gate	**Regular**	**BB**	
30				Reduction of pedestal in gate circuits and Applications of sampling gate	**Regular**	**BB**	
31				Tutorial	**Regular**	**BB**	
32				Assignment Test	**Regular**	**BB**	
33	**IV**			**Multivibrators:** Analysis of Bistable Multivibrator	**Regular**	**BB/O HP**	
34				Design of Bistable Multivibrator	**Regular**	**BB/O HP**	
35				Analysis of Mono stable Multivibrator Design of Mono stable Multivibrator	**Regular**	**BB/O HP**	
36				Analysis of Astable Multivibrator Design of Astable Multivibrator	**Regular**	**BB/O**	

						HP	
37					Applications of Multivibrators	**Regular**	**Video lecture**	
38					Triggering methods	**Regular**	**BB**	
39					Schmitt trigger	**Regular**	**BB**	
40					Design Problems solving	**Regular**	**BB**	
41					Tutorial	**Regular**	**BB**	
42					**Time base generators:** General features of a time base signal, methods of generating time base waveform	**Regular**	**BB**	
43					Miller and Bootstrap time base generators – basic principle	**Regular**	**BB**	
44					Transistor miller time base generator	**Regular**	**BB/OHP**	
45					Transistor Bootstrap time base generator	**Regular**	**BB/OHP**	
46					UJT saw tooth wave generator	**Regular**	**BB/OHP**	
47					Current time base generators Methods of linearity improvement	**Regular**	**BB/OHP**	
48					Tutorial	**Regular**	**BB/OHP**	
49					Assignment Test	**Regular**	**BB**	
50					**Synchronization and frequency division:** Pulse Synchronization of Relaxation Devices	**Regular**	**BB**	
51	**V**				Frequency division in sweep circuit, Stability of Relaxation Devices		**BB**	
52					Astable relaxation circuits, Monostable relaxation circuits		**BB**	

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53				Synchronization of a sweep circuit with symmetrical signals		**BB**	
54				Sine wave frequency division with a sweep circuit	**Regular**	**BB**	
55				**Realization of logic gates using Diodes and Transistors:** AND, OR gates using Diodes and Transistors	**Regular**	**BB/LCD**	
56				DCTL,RTL, DTL, TTL	**Regular**	**BB/LCD**	
57				**CMOS and Bi-CMOS logic family**	**Regular**	**BB/LCD**	
58				CML logic families and its comparison	**Regular**	**BB/LCD**	
59				Tutorial	**Regular**	**BB**	
60				Assignment Test	**Regular**	**BB**	
61				Revision	**Regular**	**BB**	
62				MID-II	**Regular**	**BB**	

13.5. Subject Contents

13.5. 1. Synopsis page for each period(62 pages)

13.5.2. Detailed Lecture notes containing:

   1. PPTs

   2. OHP slides

   3. Subjective type questions (approximately 5 to 8 in no)

   4. Objective type questions (approximately 20 to 30 in no)

   5. Any simulations

13.6. Course Review (By the concerned Faculty):

 (I)Aims

 (II) Sample check

(III) End of the course report by the concerned faculty

GUIDELINES:

Distribution of periods:

No. of classes required to cover JNTU syllabus : 44

No. of classes required to cover Additional topics : 2

No. of classes required to cover Assignment tests (for every 1 units 1 test) : 5

No. of classes required to cover tutorials : 6

No. of classes required to cover Mid tests : 2

No of classes required to solve University : 3

Question papers

_____

Total no of periods   :62

14 .Detailed notes

UNIT- I

1. INTRODUCTION

Linear network: Circuit designed with linear elements Resistors, Capacitor and Inductors is called linear network.

Linear elements :Resistor ,capacitors and inductors are called linear elements because the current passing to the elements is proportional to the applied voltage, there is a linear relation between current and voltage.

When a sinusoidal signal applied to linear network the output also sinusoidal in nature but a non-sinusoidal signal response is different.

When devices such as diodes, bipolar junction transistors (BJTs) and field-effect transistors (FETs) are used in amplifiers, oscillators, rectifiers and other such applications, these devices are used either as linear or nonlinear circuit elements, for which they have to be used in a limited range of the transfer characteristic (defines the relation between the input and the output). If the operation goes beyond the

linear region of the transfer characteristic, unwanted frequencies called harmonics—integer multiples of the fundamental frequency—appear in the output of the circuit. However, when the signal swing is large, as in power amplifiers, the output is invariably distorted. This distortion can be minimized using a push–pull configuration as this arrangement eliminates even harmonics. To analyze a given circuit comprising such devices, it is possible to replace the device by its equivalent circuit. To simplify the analysis, it is necessary, at times, to piece-wise linearize the transfer characteristic so that the behavior of the device can be predicted in that limited region of operation.

These devices—diodes, transistors, FETs and so on—can also be used as switches in switching applications by driving the device into the OFF state in one case and by driving the device into the ON state in the other case. However, the inter-electrode capacitances limit the switching speed. Operational amplifiers and negative resistance devices also find applications in pulse and switching circuits. This chapter presents a brief overview of the fundamentals to facilitate comprehension of the principles of pulse and switching circuits.

1.2 CURRENT AND VOLTAGE SOURCES

Normally either ac or dc sources are used as current and voltage sources. A source can be either a voltage source (Thévenin source) or a current source (Norton source). An ideal voltage source should have zero internal resistance so that when current is drawn from the source, there is no voltage drop across the internal resistance of the source and the entire source voltage is available at its output terminals. Similarly, in a current source, no appreciable amount of current should flow through the internal resistance of the generator and the entire source current should flow through the load. For this, the internal resistance of the current source should ideally be infinity.

Figure 1.1(a) shows a practical voltage or Thévenin source and Fig. 1.1(b) a current or Norton source. It is possible to convert a Thévenin source into a Norton source and vice versa. To convert the Thévenin source [represented in Fig. 1.1(a)] into a Norton source [see Fig. 1.1(b)], we calculate the current (I) in the circuit using the relation $I = V/R_s$, where R_S is the internal resistance in shunt with the current source I. Similarly, to convert the Norton source into a Thévenin source as shown in Fig. 1.1(a), we calculate the voltage (V) across R_S as $V = IR_S$, where R_S is its internal resistance in series with the source V. Consider the single-loop network using a voltage source, as shown in Fig. 1.2. From Fig. 1.2:
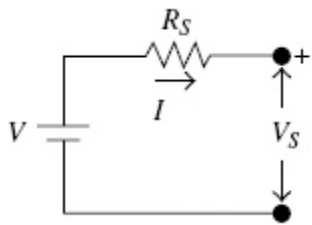
FIGURE 1.1(a) Thévenin or voltage source
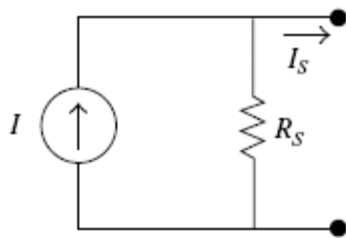
FIGURE 1.1(b) Norton or current source

$$I = \frac{V}{R_1 + R_2}$$

and

$$V_{R2} = IR_2 = \frac{VR_2}{R_1 + R_2}$$

The single-loop network shown in <u>Fig. 1.2</u> is analyzed using Ohm's law. In this circuit, R_1 and R_2 comprise a potential divider. So, <u>Eq. (1.1)</u> is used to calculate V_{R2} directly instead of first calculating the current and then the voltage.

However, to analyze a network that has more than one loop, i.e., calculate the current in a given loop or voltage across the given branch, two basic network theorems—Kirchoff's voltage law and Kirchoff's current law—are used.
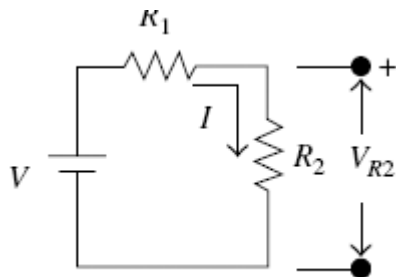
FIGURE 1.2 A single-loop network

Linear systems are those that satisfy both homogeneity and additivity.

(i) Homogeneity: Let x be the input to a linear system and y the corresponding output, as shown in <u>Fig. 2.1</u>. If the input is doubled ($2x$), then the output is also doubled ($2y$). In general, a system is said to exhibit homogeneity if, for the input nx to the system, the corresponding output is ny (where n is an integer). Thus, a linear system enables us to predict the output.
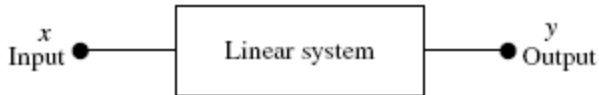
FIGURE 2.1 A linear system

(ii) Additivity: For two input signals x_1 and x_2 applied to a linear system, let y_1 and y_2 be the corresponding output signals. Further, if ($x_1 + x_2$) is the input to the linear system and ($y_1 + y_2$) the corresponding output, it means that the measured response will just be the sum of its responses to each of the inputs presented separately. This property is called additivity. Homogeneity and additivity, taken together, comprise the principle of superposition.

(iii) Shift invariance: Let an input x be applied to a linear system at time t_1. If the same input is applied at a different time instant t_2, the two outputs should be the same except for the corresponding shift in time. A linear system that exhibits this property is called a shift-invariant linear system. All linear systems are not necessarily shift invariant.

A circuit employing linear circuit components, namely, R, L and C can be termed a linear circuit. When a sinusoidal signal is applied to either RC or RL circuits, the shape of the signal is preserved at the output, with a change in only the amplitude and the phase. However, when a non-sinusoidal signal is transmitted through a linear network, the form of the output signal is altered. The process by which the shape of a non-sinusoidal signal passed through a linear network is altered is called linear waveshaping. We study the response of high-pass RC and RL circuits to different types of inputs in the following sections.

2.2 HIGH-PASS CIRCUITS

<u>Figures 2.2(a)</u> and <u>2.2(b)</u> represent high-pass RC and RL circuits, respectively.
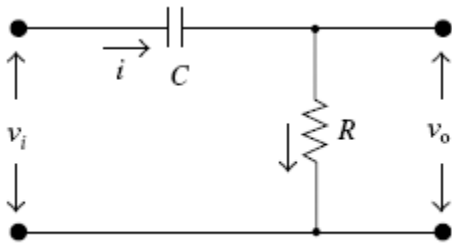
FIGURE 2.2(a) A high-pass RC circuit

Consider the high-pass *RC* circuit shown in Fig. 2.2(a). The capacitor offers a low reactance ($X_C = 1/j\omega C$) as the frequency increases; hence, the output is large. Consequently, high-frequency signals are passed to the output with negligible attenuation whereas, at low frequencies, due to the large reactance offered by the condenser, the output signal is small. Similarly, in the circuit shown in Fig. 2.2(b), the inductive reactance $X_L (= j\omega L)$ increases with frequency, leading to a large output. At low frequencies, the reactance of the inductor X_L becomes small; hence, the output is small. Therefore, the circuits in Figs. 2.2(a) and (b) are called high-pass circuits. In the case of *L*, X_L is directly proportional to frequency; and in the case of *C*, X_C is inversely proportional to frequency. *C* and *L* may therefore be called inverse circuit elements. Thus, in the high-pass circuit of Fig. 2.2(a), *C* appears as a series element; and in the high-pass circuit of Fig. 2.2(b), *L* appears as a shunt element. The time constant τ is given by: $\tau = RC = L/R$.
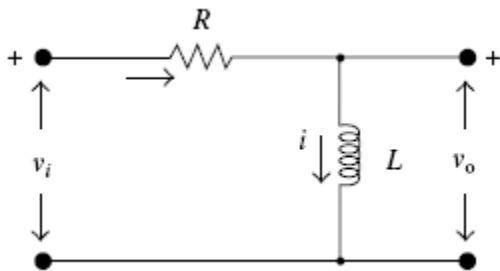
FIGURE 2.2(b) A high-pass *RL* circuit

What will be the response if different types of inputs such as sinusoidal, step, pulse, square wave, exponential and ramp are applied to a high-pass circuit?

$$v_o = v_i \frac{R}{R + \dfrac{1}{j\omega C}} \tag{2.1}$$

$$\left|\frac{v_o}{v_i}\right| = \frac{R}{\sqrt{R^2 + \left(\dfrac{1}{\omega C}\right)^2}} = \frac{R}{R\sqrt{1 + \left(\dfrac{1}{\omega CR}\right)^2}} = \frac{1}{\sqrt{1 + \left(\dfrac{1}{\omega CR}\right)^2}}$$

Let

$$\omega_1 = \frac{1}{CR} = \frac{1}{\tau} \tag{2.2}$$

where, $\tau = RC$, the time constant of the circuit.

$$\left|\frac{v_o}{v_i}\right| = \frac{1}{\sqrt{1 + \left(\dfrac{\omega_1}{\omega}\right)^2}} = \frac{1}{\sqrt{1 + \left(\dfrac{T}{\tau}\right)^2}} \tag{2.3}$$

LOW PASS RC CIRCUITS

A low-pass circuit is one which gives an appreciable output for low frequencies and zero or negligible output for high frequencies. In this chapter, we essentially consider low-pass *RC* and *RL* circuits and their responses to different types of inputs. Also, we study attenuators that reduce the magnitude of the signal to the desired level. Attenuators which give an output that is independent of frequency are studied. One application of such a circuit is as a CRO probe. Further, the response of the *RLC* circuit to step input is considered and its output under various conditions such as under-damped, critically damped and over-damped conditions is presented. The application of an *RLC* circuit as a ringing circuit is also considered.

3.2 LOW-PASS CIRCUITS

Low-pass circuits derive their name from the fact that the output of these circuits is larger for lower frequencies and vice-versa. Figures 3.1(a) and (b) represent a low-pass *RC* circuit and a low-pass *RL* circuit, respectively.

In the *RC* circuit, shown in Fig. 3.1(a), at low frequencies, the reactance of *C* is large and decreases with increasing frequency. Hence, the output is smaller for higher frequencies and vice-versa. Similarly, in

the *RL* circuit shown in Fig. 3.1(b), the inductive reactance is small for low frequencies and hence, the output is large at low frequencies. As the frequency increases, the inductive reactance increases; hence, the output decreases. Therefore, these circuits are called low-pass circuits. Let us consider the response of these low-pass circuits to different types of inputs.
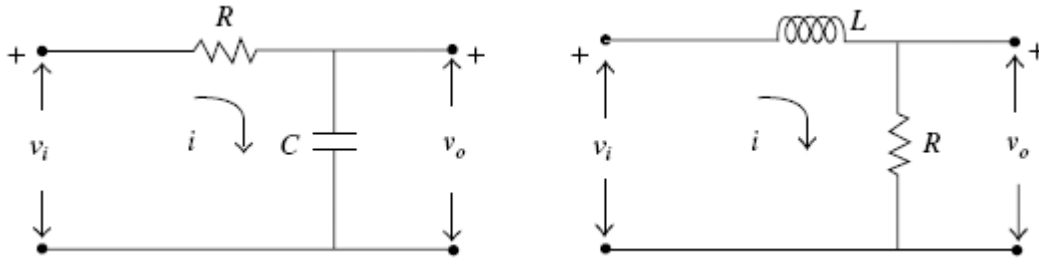
FIGURE 3.1(a) A low-pass *RC* circuit; and (b) a low-pass *RL* circuit

3.2.1 The Response of a Low-pass *RC* Circuit to Sinusoidal Input

For the circuit given in Fig. 3.1(a), if a sinusoidal signal is applied as the input, the output v_o is given by the relation:

$$v_0 = v_i \frac{\dfrac{1}{j\omega C}}{R + \dfrac{1}{j\omega C}} \qquad \frac{v_o}{v_i} = \frac{1}{1 + j\omega CR}$$

$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{1 + (\omega CR)^2}} = \frac{1}{\sqrt{1 + \left(\dfrac{\omega}{\omega_2}\right)^2}} = \frac{1}{\sqrt{1 + \left(\dfrac{\tau}{T}\right)^2}} \qquad\qquad (3.1)$$

where, $\omega_2 = 1/CR = 1/\tau$. From Eq. (3.1), the phase shift θ the signal undergoes is given as:

$\theta = \tan^{-1}(\omega/\omega_2) = \tan^{-1}(\tau/T)$

Figure 3.2(a) shows a typical frequency vs. gain characteristic. Hence, f_2 is the upper half-power frequency. At $\omega = \omega_2$,

$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{2}} = 0.707$$

Figure 3.2(b) shows the variation of gain with frequency for different values of τ. As is evident from the figure, the half-power frequency, f_2, increases with the decreasing values of τ, the time constant. The sinusoidal signal undergoes a change only in the amplitude but its shape remains preserved.

Figure 3.2(c) shows the variation of θ as a function of frequency. As (τ/T) becomes large, θ approaches 90°. This characteristic can be appreciated when we talk about an integrator later.

Non-sinusoidal Waveforms

Any waveform whose shape is different from that of sinusoidal wave is called a non-sinusoidal waveform. For example pulse square, symmetrical square triangular and saw-tooth are non- sinusoidal waves. When one quantity is dependent upon some other variable quantity varies with respect to others. In case of electronic circuits function usually means that current or voltage varies with respect to time. All these waveform are the function voltage or current with respect to time such as step, ramp and exponential are explained as under:

Step Function:

A step function shown in Fig. 1(a), makes an instantaneous jump from one steady value to

another steady value. A step means an instantaneous change in level.
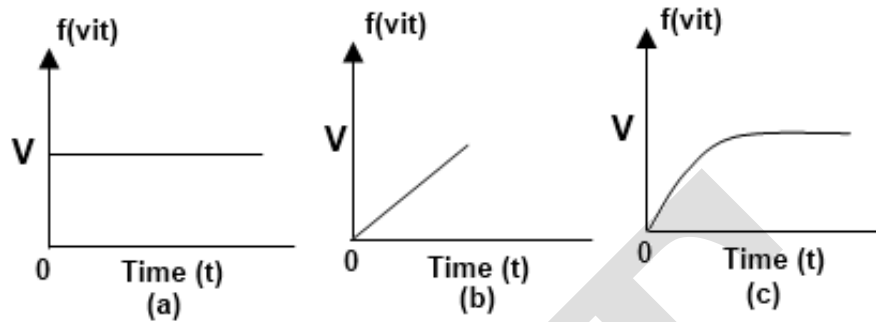
Figure 1 *Functions*

In such a case, voltage maintains zero value for all times $t < 0$ and maintains the value V for all times t > 0 is called a step voltage.

Ramp Function:

A ramp function shown in Figure 1(b) isone that voltage increases or decreases linearly with time. Slope of the function is constant. In such a case, voltage is zero for $t < 0$ and increases linearly with time for $t > 0$.it is linear change in function with respect to time called a ramp.

Exponential Function:

An exponential function is a function of voltage that increases or decreases exponentially with time. In such a case, voltage is zero for $t < 0$ and increases nonlinearly with time t called an exponential voltage. The terms used for exponential are e^x and e^{-x}. Exponential quantity gap is known as an exponential curve.

Different Types of Waveforms

Let us now discus the pulse square, symmetrical square, Triangular and saw-tooth waveforms.

Pulse waveform

Figure 2(a) shows the waveform of an ideal pulse. The pulse amplitude is V and the pulse duration is t_p. It is evident from Fig. 2(b) and (c) that the pulse may be considered as the sum of the step voltage $+V$, whose discontinuity occur at $t = 0$ and a step voltage $—V$, whose discontinuity occurs at $t = t_p$. The pulse waveform find extensive use is almost every field of electronics such as communication, computer, defense equipment, etc.

(a)Pulse   (b)Positive step Voltage   (c)Negative step voltage
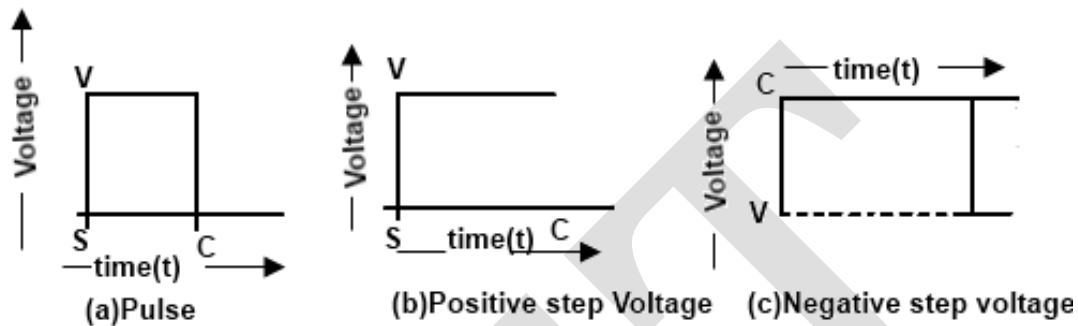
Figure 2

Square waveform

A waveform which maintains itself at one constant voltage level V_1 for a time T_1 and at another constant level V_2 for time T_2 and is repetitive with a period $T = T_1 + T_2$ as shown in Fig. 2 (a) is called a square waveform. The square waveform is used in digital electronic circuits, radars and as synchronizing pulses in television.

(a) Square waveform   (b)Symmetrical square waveform
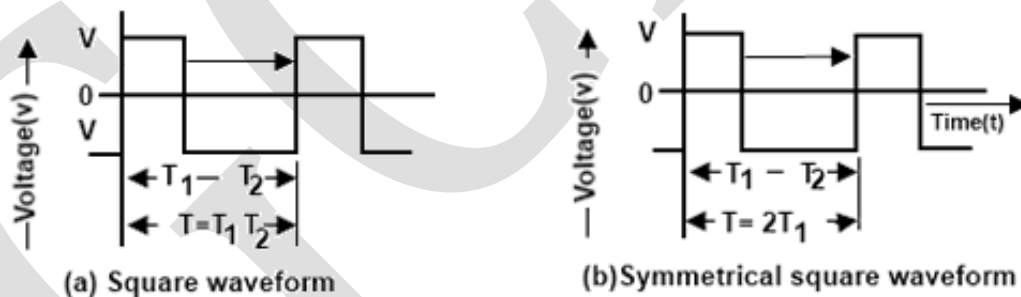
Figure 3

Symmetrical square waveform

A square waveform for which $T_1 = T_2 = T/2$ as shown in Fig. 3(b) is called a square waveform. It may be noted that because of the symmetry, the voltage levels V_1 and V_2 are equal and opposite $V_1 = —V_2$. The symmetrical square waveform is very useful in digital electronic circuits.

Ttriangular waveform

A waveform which increase linearly with time to a voltage level V for a time T/2 and then decreases linearly to its original level for a time T/2 and is repetitive with a period T as shown in Fig. 4(a) is called triangular waveform. It may be noted from this figure, that a triangular wave may be considered as the sum of ramp voltage, which increases at a rate of 2V/T for a time T/2 and the ramp voltage which decreases at a rate of —2V/T for the remaining time T/2. The triangular waveform is used in scanning circuits, where a uniform left-to-right scan is required as

In computer displays. These are also used in timing circuit for electronics applications.

(a) Trianglar waveform   (b) Saw-tooth waveform
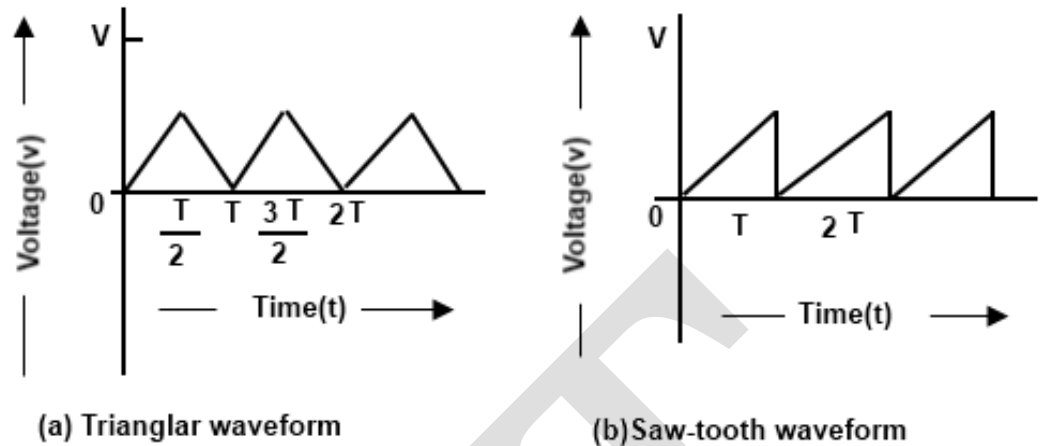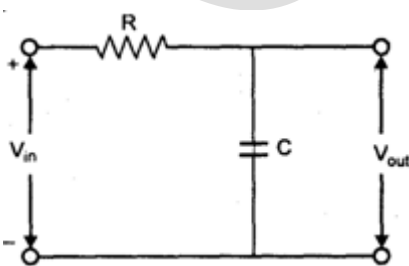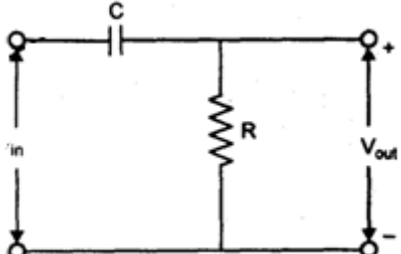
<u>Figure 4</u>

Saw tooth waveform

A waveform increases linearly with time to a voltage level V for a time T and then changes abruptly to its original level and is repetitive as shown in Fig. 4(b) is called saw tooth waveform. It is also called sweep waveform or time-base waveform. The saw tooth waveform is used in the scanning circuit of cathode ray oscilloscopes and televisions.

Differences between Low-pass and High-pass circuit showing circuit diagrams.

Low-Pass Circuit	High-Pass Circuits
(i) In a low pass circuit V_{out} is taken across the capacitor.	(i) In high pass RC data, the O/P voltage V_{out} is taken across the resistance.
(ii) It passes low frequency signals and blocks the high frequency signals.	(ii) It blocks P attenuates low frequencies, but allows high frequency signals to pass through it.
(iii)	(iii)
(iv) Current through the circuit is given as:	(iv) Current through the circuit is given as:

$$I = \frac{V_{in}}{R - j \times c}$$

(v) Output voltage is given as

$$V_{out} = \left[\frac{-j \times c}{R - j \times c}\right].V_{in}$$

(vi) Magnitude of amplitude is given by:

$$|A| = \frac{1}{\sqrt{1 + \left(\dfrac{f}{f_2}\right)^2}}$$

Where f_2 = cut off frequency.

(vii) Phase angle:

$$\theta = \tan^{-1}\left(\frac{f}{f_2}\right)$$

(viii) Frequency response curve:
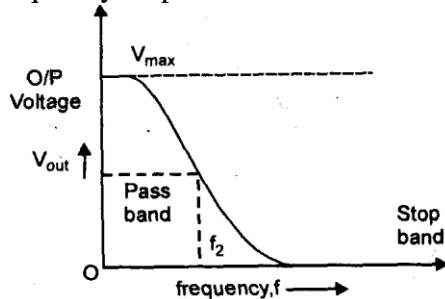
(ix) At very high frequencies the capacitive reactance become very small so 0/p becomes equal to i/p.

(x) R-C circuits with time constant larger than time period of the input signal are used as by-pass capacitors.

(xi) It is used is generation of triangular and ramp waveforms.

$$I = \frac{V_{in}}{R - j \times c}$$

(v) Output voltage is given as:

$$V_{out} = \left[\frac{R}{R - j \times c}\right].V_{in}$$

(vi) Magnitude amplitude is given by:

$$|A| = \frac{1}{\sqrt{1 + \left(\dfrac{f_1}{f}\right)^2}}$$

where f_1 = frequency at which $X_C = R$.

(vii) Phase angle:

$$\theta = \tan^{-1}\left(\frac{f_1}{f}\right)$$

(viii) Frequency response curve:
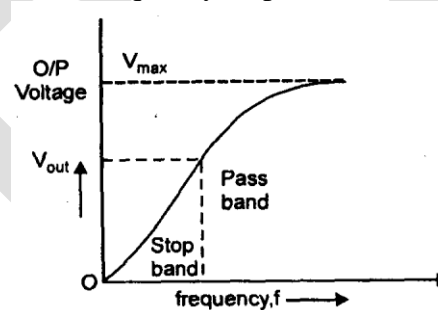
(ix) With the increase in frequency the reactance of the capacitor decreases and therefore, the output will be zero and gain increase.

(x) R-C circuits with RC >> T is employed in R-C coupling of amplifiers where distortion and differentiation of waveform is to be avoided.

(xi) R-C circuits with RC << T is employed generate pipes for triggering electronic circuit such as flip-flop multivibrators.

Draw the standard waveforms used to obtain response of a R-C circuit diagrams.

Ans. The standard waveforms used to obtain response of a RC circuit diagram are as under:
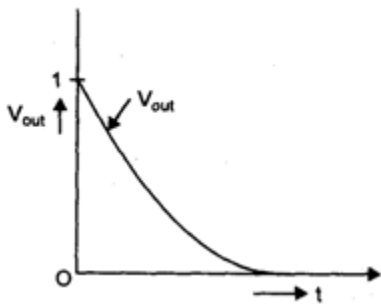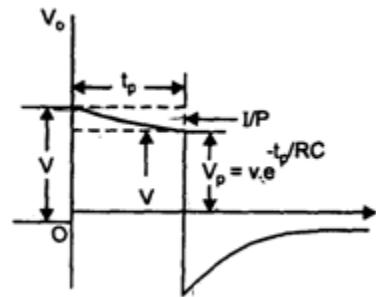
*Step voltage response of   **** A step pulse after transmission through High-pass R-C**
circuit   **high:pass RC circuit**
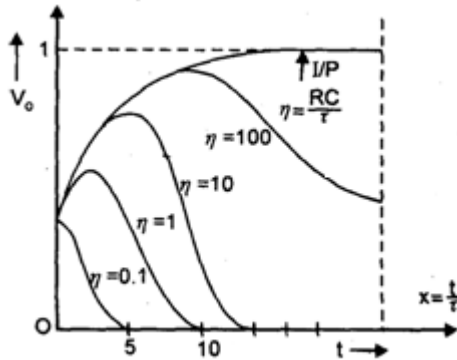
Response of a high-pass RC   **Response of a high-pass RC circuit**
circuit to an exponential input.   **to a ramp voltage for**
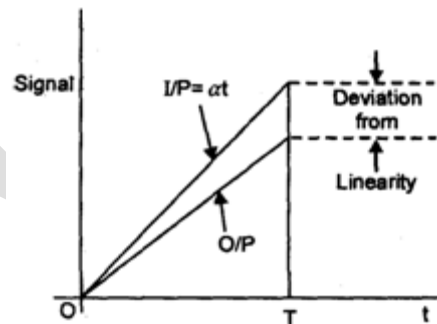
$$\frac{RC}{\tau} >> 1.$$
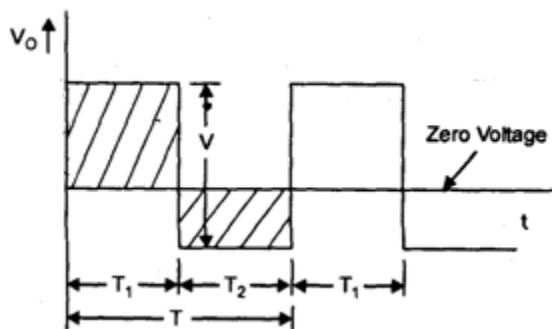
Output voltage for square wave input $\tau >> \text{T}.$ Area $A_1 =$ Area $A_2.$

In a low frequency series R-C circuit obtain unit step response if R = $1M\Omega$ and t (time constant) = 1 sec.

Ans. A step voltage v(t) is written as

$$v(t) = \begin{cases} 0 \text{ for } t < 0 \\ V \text{ for } t \geq 0 \end{cases}$$

General solution for a single time constant circuit having initial and final values $v_0(0)$ and $v_0(\infty)$
Respectively is,

$$v_0(t) = v_0(\infty) + [v_0(0) - v_0(\infty)].e^{-t/\tau}$$

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Substituting

$$v_0(t) = V\left[1 - e^{-\frac{t}{RC}}\right]$$

If
$$V = 1, RC = \tau = 1$$
$$v_0(t) = 1.[1-e^{-t/1}]$$
$$v_0(t) = (1-e^{-t/1})$$
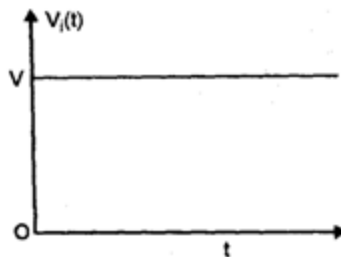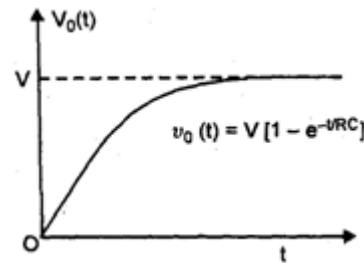
*The step waveform.   **Output waveform of Rc low-Para filter

Note: This waveform is exponentially raising waveform as shown in fig. (b). this response reaches almost 'V' after a time't' greater than 5RC.

Define delay time, rise time, storage time and fall time in response Characteristics.

Ans. Time constant definition: The required for a capacitive circuit to reach its steady state or final voltage can be specified in terms of the constant denoted by τ The time constant in an RC circuit is τ

$= RC$, while for an RL circuit is $\tau = \dfrac{L}{R}$

Time constant of a Raising exponential: Raising capacitor Voltage

$$v_0(t) = V\left[1 - e^{\frac{-t}{RC}}\right] \qquad \qquad ...(1)$$

$$\frac{dV_c(t)}{dt} = \frac{V}{RC}.e^{-t/RC}, \left[\frac{d}{dt}.v_c(t)\right]_{t=0} = \frac{V}{RC}$$

Differentiating,

Time constant can be defined in terms of exponentially rising voltage as

(i) τ can be defined for a rising voltage as the time required for the voltage to reach its final value if the voltage continues to rise at its initial rate.

(ii) Sometimes, τ is defined as the time required for the voltage to increase to 63.2 percent of its final value.

Time constant of a Decaying Exponential

The decaying capacitor voltage

$$v_0(t) = V.e^{-t/RC} \qquad \qquad ...(2)$$

By differentiating this equation initial slope of this decaying exponential as,

$$\frac{d}{dt}\big[V_c(t)\big] = -\frac{V}{RC}.e^{-t/RC}$$

$$\left[\frac{dV_c(t)}{dt}\right]_{t=0} = -\frac{V}{RC}$$

Taking the above decaying exponential voltage into account, time constant is defined in the following two ways:

(i) The time constant τ can be defined for an exponentially decaying voltage as the time required for the voltage to reach zero, if the voltage continues to decay at its initial rate.

(ii) Sometimes, the time constant τ is defined as the time required for the voltage to decay to 36.8 percent of its initial value.

Physical significance of time constant

The time constant 'τ' gives an indication of time needed for the circuit transient to disappear. After the disappearance of the transient state, the circuit reaches its steady state.

Theoretically a transient state persists for infinite time. However, we can always assume that the circuit has reached its steady state after a lapse of 5τ.

This implies that a circuit with a small 'r' ensures fast response that is, it reaches its steady state in a short-time.

Similarly, if the 'r' of a circuit is large that circuit takes long time to attain, its steady state.
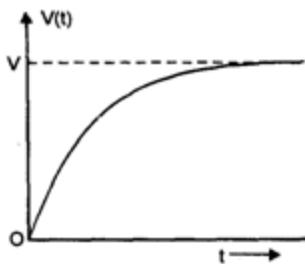
Fig. (a) Raising exponential waveform
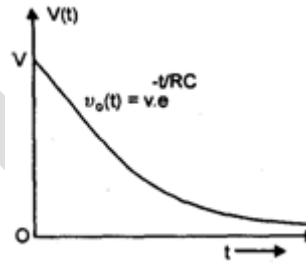
Fig. (b) Decaying exponential waveform
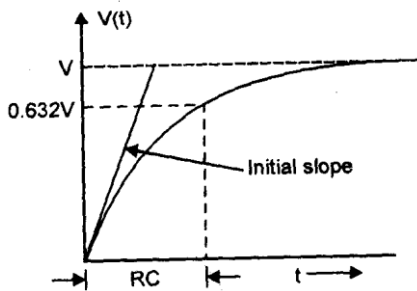
Fig. (c) Time constant of raising exponential waveform
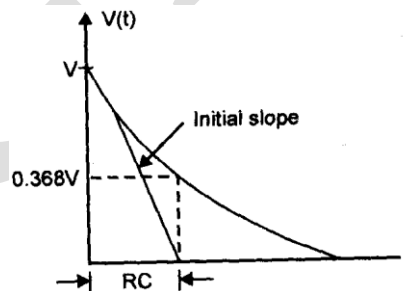
Fig. (d) Time constant of decaying exponential waveform

Rise time: The rise time of the step response is defind as the time taken for the exponentially raising output waveform to rise from 10% to 90% of its final value 'v'.
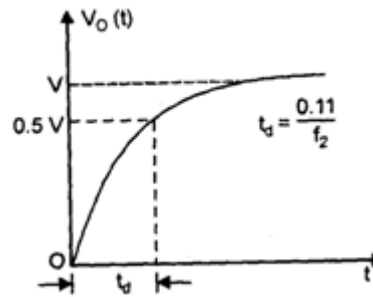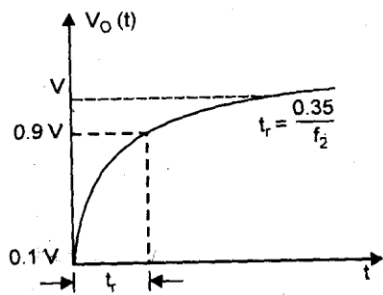
Fig. (a) Definition of Rise time   Fig. (b) Definition of Delay time.

The definition of rise time is graphically indicated in fig. (a). Let t_1 and t_2 are the times at which the waveform reaches 10% and 90% of its final value V_1 respectively,

$$0.1 \ V = V[1 - e^{-t_1/RC}]$$

$$0.9 \ V = V[1 - e^{-t_2/RC}]$$

From this, we can determine the values of $'t_1'$ and $'t_2'$

$$t_1 = 0.1 \ RC \qquad\qquad ...(1)$$

$$t_2 = 2.3 \ RC \qquad\qquad ...(2)$$

$$t_r = t_2 - t_1 = 2.2 \ RC$$

$$f_2 = \frac{1}{2\pi RC}$$

$$RC = \frac{1}{2\pi f_2}$$

$$t_r = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2} \qquad\qquad ...(3)$$

Expression for delay time: The delay time t_d is defind as the time taken for the exponentially raising output waveform to rise from Zero to 50 percent of its final value 'v'.

$$0.5V = V\left[1 - e^{-\frac{td}{RC}}\right]$$

$$t_d = 0.7RC = \frac{0.7}{2\pi f_2} = \frac{0.11}{f_2}$$

$$t_d = \frac{0.11}{f_2} \qquad\qquad ...(2)$$

Storage time: It is the time when the output waveform becomes constant or reaches the steady state.

Fall time: The time pulse takes to decreases from 90% to 10% of its normal amplitude is called fall time.
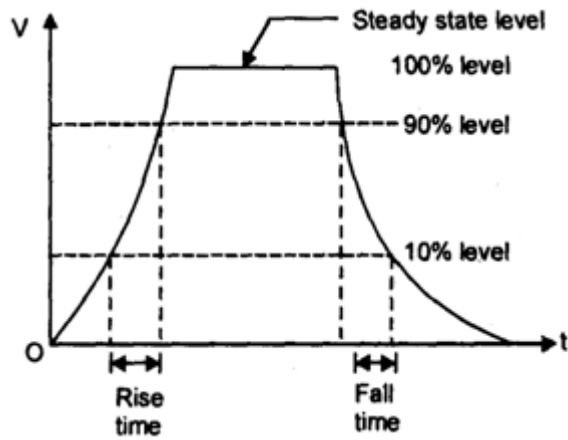
Q.5. If RC time constant of a high pass filter is made increasingly smaller in comparison of duration of input waveform. Is the width of the output pulse increased or decreased. Explain your answer.

Ans. Pulse input: The response to a pulse for times less than the pulse t_p width is the same as that for a step input and is given by

$$v_0(t) = V.\left[1 - e^{\frac{-t}{RC}}\right] \qquad ...(2)$$

At the end of the pulse, the voltage is V_p and the output must decrease to zero from this value with a time constant RC as indicated in Fig. (a). Note the waveform distortion that has resulted from passing a pulse through a low-pass RC circuit. In particular it should be observed that the output will always extend beyond the pulse width t_p, because whatever charge has accumulated on the capacitor 'C' during the pulse cannot leak off instantaneously.
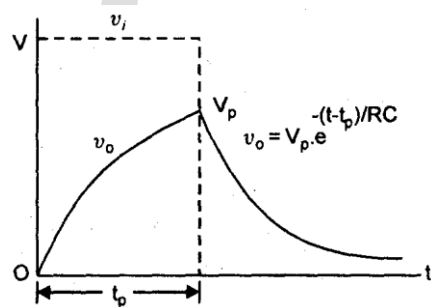
Fig. Pulse response of the Low-pass RC circuit.   **Fig. Pulse response for the case** $f_2 = \left(\dfrac{1}{t_p}\right)$
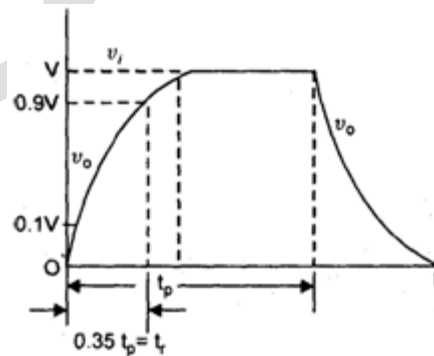
If it is desired to minimise the distortion then the rise time must be small compared with the pulse width. f_2 Is chosen equal to $\left(\dfrac{1}{t_p}\right)$, then, $t_r = 0.35\ t_p$.
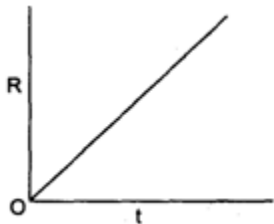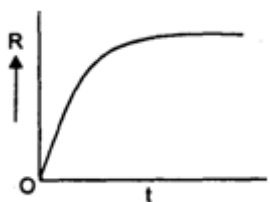
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The 0/P is as pictured in fig. (b), which for many applications in a reasonable reproduction- of the input.

We often use the rule of thumb that a pulse shape will be preserved if the 3^{-dB} Frequency is approximately equal to the reciprocal of the pulse width. Thus to pass a 0.5 μsec reasonably well requires a circuit with an upper 3^{-dB} frequency of the order of 2MHz.

For a high pass RC circuit, $f_1 = \dfrac{1}{2\pi RC}$. if RC is smaller, f_1 will increase. So pulse width is inversely proportional to frequency.
Pulse width of the output will decrease.

Difference between linear and non-linear wave shaping circuits.

Linear Wave Shaping	Non-Linear Wave Shaping
(i) It involves passage of signal through linear system.	(i) It involves passage of signal through non-linear systems.
(ii) The operation involved are linear operations such as integration, differentiation, summation, filtering etc.	(ii) It permits transformation of analog signal to digital signal and vice-versa.
(iii) Some of the important on-sinusoidal waveform are the step, pulse, square, wave, ramp and exponential waveform.	(iii) Eg. (1) Clipping operation; and (2) rejection of negative spikes by rectification are non-linear operation.
(iv) Typical example is low-pass and high-pass R-C circuit.	(iv) Clamping circuits. Example is an integrator using an OP-AMP.
(v) It includes R-C circuit R-L and R-L-C circuit.	(v) It includes diode, zener diode, transistor, vacuum tube, etc.
(vi) It can be described by linear differential wave equations.	(vi) When any wave form is applied at the input of non-linear circuit.

linear wave shaping and give examples.

Wave-shaping may be defined as the process of generating new waveforms from older waveforms by employing certain physical systems.

Linear wave shaping involves passage of signal through linear systems such as R-C , R-L and R-L-C circuits and the operations involved are linear such as integration , differentiation summation , filtering etc. example of linear wave shaping.

(i) High- pass and low- pass R-C circuit.
(ii) R-C differentiator.
(iii) R-C intergrator.
(iv) R-L circuits.
(v) R-L-C circuits.
(vi) Attenuators.

In pulse circuitry, there are number of non-sinusoidal waveform which appears regularly. The most important of them are : step, pulse, square wave, Ramp and exponential waveforms.

Attenuators

Compensated Attenuators	Uncompensated Attenuators
Compensated attenuators are those circuits which are use to reduce the rise time due to stray capacitance by introducing capacitors to balance the stray capacitance.	Normally the output of the attenuator is fed to a circuit that offers a reactive load. This reactive load is generally the stray input capacitance of an amplifier. When we consider the stray capacitance, the purely resistive attenuator becomes an uncompensated attenuator.

Perfect Attenuators : In most of the electronic applications, the amplitude of the signal is magnified with the help of an amplifier. There are also instances, where the signal amplitude has to be reduced without affecting the signal waveshape. Attenuator is a circuit that reduces the amplitude of the signal without leading to any distortion in the signal waveform. The CR0 probe can be cited as one such example. The high-pass filter and low-pass filter circuits, reduce the amplitude or attenuate the input signal.

In uncompensated attenuators, the stray capacitance makes attenuation frequency dependent.

The circuit in fig. 2(b) can be redrawn as a low-pass filter circuit by applying Thevenin's theorem. Here, R becomes the parallel combination of $'R_1'$ and $'R_2'$.

Since it is not possible to remove this stray capacitance, one can neutralise the presence of the stray capacitance. This is done by compensating the attenuator by connecting $'C_1'$ across $'R_1'$.

The condition for a circuit to be precisely satisfied for perfect compensation is,

$$R_1 C_1 = R_2 C_2.$$

This can be satisfied by redrawing the circuit in Fig 2(c) as a bridge circuit shown in Fig. 2(d). The current in the short circuit branch A-B becomes zero when the bridge is balanced. When no current flows through this branch, the output voltage can be again written as,

$$v_0(t) = \frac{R_2}{R_1 + R_2} \cdot v_i(t)$$

$$R_i \times \frac{1}{2\pi f\, C_2} = R_2 \times \frac{1}{2\pi f\, C_1}$$

$$\boxed{C_1 = \frac{R_2 C_2}{R_1}}$$

This is the condition for perfect compensation. However, it is difficult to satisfy this condition exactly in a practical situation.
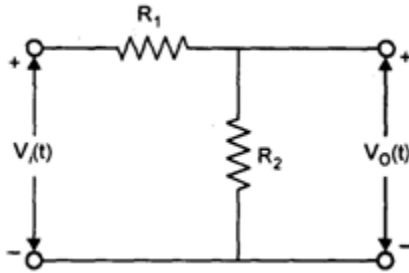
(a) The perfect Compensator
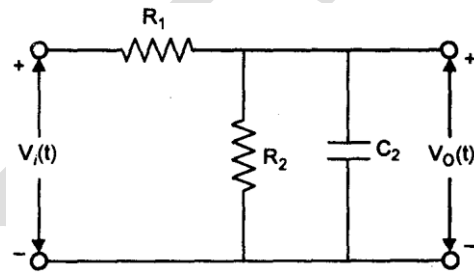
(b) The uncompensated attenuator
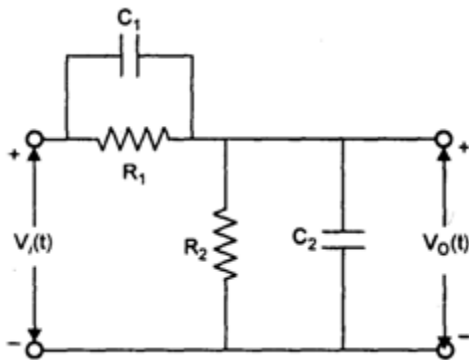
(c) The compensated attenuator
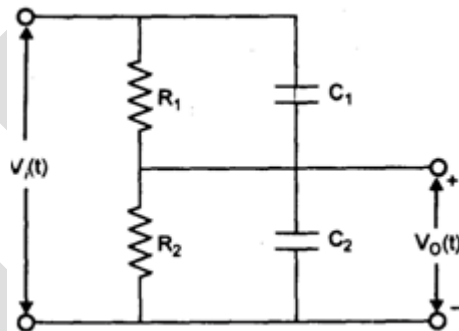
(d) The compensated attenuator redrawn as a bridge

Fig. 2 The compensated attenuator.

Problems:

What is the expression of time constant (τ) for an R-C circuit with R = 500 Ω and C = 20 μF ? Show that the unit of τ is second.

Ans. We have

Resistance   R = 500 Ω and C=20 μF

Time constant of an R-C circuit is given as

$$\tau = RC = 500 \times 20 \times 10^{-6} = 10{,}000 \times 10^{-6} = 10^{-2} \text{ sec}$$
$$= 0.01 \text{ seconds}$$

For a simple circuit

$$R = \frac{V}{I}, \text{ and } C = \frac{1}{V}\int i\, dt$$

$$\tau, \text{ the time constant} = RC = \frac{V}{I} \times \frac{1}{V}\int i\, dt = \frac{1}{I}\int i\, dt$$

Taking the units = $\dfrac{\text{Ampere} - \text{sec Ampere}}{\text{Ampere}}$

- Unit of τ' is seconds.

or

Dimensions of R and C are $[mL^2.T^{-3}.I^{-2}]$ and $[m^{-1}L^{-2}.T^4.I^2]$

- $$T = [mL^2.T^{-3}.I^{-2}].[m^{-1}L^{-2}.T^4.I^2] = [T]$$
- Unit of 'r' is second.

Ringing Circuit

Ans. Ringing circuits are those which generate asequence of pulses spaced regularly intime these circuits have undamped oxillations depending on the number of ringing duty cycles recuired Consider the ringing circuit of Fig. A.1. in which there is an initial voltage $\overline{V_0}$ across the capacitor 'C' as well as an initial inductor current I. It is now convenient to introduce a parameter Δ defined as the ratio of coil current to resistor current at t = 0.

$$\Delta = \frac{I}{V_0/R} = \frac{IR}{V_0} \qquad\qquad ...(A.1)$$
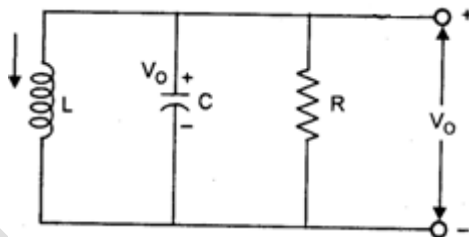
Fig. A. 1 Ringing circuit with initial current 'I' in inductor and initial voltage V_0 across capacitor.

The output $\dfrac{v_0(t)}{V_0}$ can be expressed as a function of a time $\left(x = \dfrac{t}{T_0}\right)$ with Δ and 'k' as a parameters the definations of 'k' and T_0' are

$$k = \frac{1}{2R}\sqrt{\frac{L}{C}} \text{ and } T_0 = 2\pi\sqrt{LC} \qquad\qquad ...(A.2)$$

Critical Damping, k=1

$$\frac{v_0(t)}{v_0} \quad [1-(1+2\Delta)(2\pi x)]\,\varepsilon^{-2\pi x} \qquad\qquad\qquad ...(A.3)$$

Overdamped with $4k^2 \gg 1$,

$$\frac{v_0(t)}{V_0} = -\left[\frac{\frac{1}{4k^2}+\Delta}{}\right]\varepsilon^{-\pi x/k} + (1+\Delta)\,\varepsilon^{-4\pi kx} \qquad\qquad ...(A.4)$$

Underdamped, $k < 1$

$$-\frac{v_0(t)}{V_0}\left[-(1+2\Delta)\cdot\frac{k}{\sqrt{1-k^2}}\cdot\sin 2\pi\sqrt{1-k^2}x + \cos 2\pi\sqrt{1-k^2}x\right]\varepsilon^{-2\pi kx} \qquad ...(A.5)$$

These responses are plotted in Figs. A.2, A.3 and A.4.

We note that even for the critically damped case, there may be an undershoot i.e., the output which starts at a positive value drops to a negative value before returning asymtotically to zero.
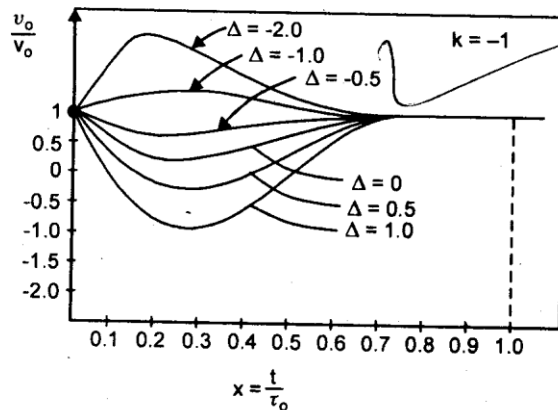
Fig. A.2. of equation (A.3).
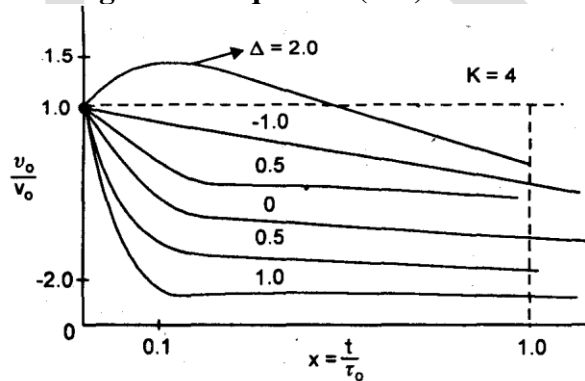
Fig. A. 3. (Plot of eq. (A.4) with k = 4.

If V_0 ad I have the relative polarities indicated in Fig. A. 1 then Δ is positive. If the relative polarities differ from those indicated, the 'Δ' is negative. For a negative A, the output may rise first (see the curve for 'Δ' = —2.0) ; before falling to zero. The physical reason for this initial increase in output is that the inductor current (with the polarity opposite to that in Fig. A.1.) may charge the capacitor to a more positive voltage before 'C' discharges through the resistor.
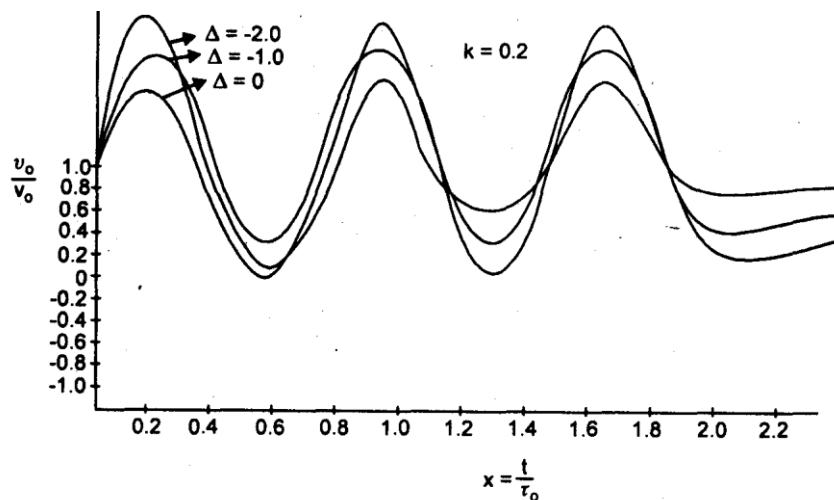
Fig. (A.4) Plot of equation (4.5) with k = 0.2.

We see that the waveform depends upon the inductor and resistor currents (the sign and magnitude of Δ) and upon the amount of the damping (the value of k).

The areas under each curve of Fig. A.3, Fig. A.2 and Fig A. 4. is $\left(\dfrac{-k.\Delta}{\pi}\right)$. This canbe verified by direct integration or much more easily by proceeding as follows:

$$v_0(t) = \alpha.\frac{di}{dt}(t)$$

Since

$$\frac{v_0(t)}{V_0} = \frac{L}{V_0.T_0}.\frac{di}{dx}(t)$$

Or

Then   Area $= \displaystyle\int_0^\infty \frac{v_0(t)}{V_0}dx = \frac{L}{V_0.T_0}\int_0^\infty di(t)$

$$= \frac{-LI}{V_0.T_0} \times \frac{-L.\Delta}{R.T_0}$$

Area $= \dfrac{-L.\Delta}{\left(\dfrac{1}{2}K\right):\sqrt{L/C}} \times \dfrac{1}{2\pi\sqrt{LC}}$

$$= \frac{-K\Delta}{\pi} \qquad\qquad ...(A.6)$$

User : These circuits are employed in timing circuit in automatic control circuit.

Why RC circuit is preferred over RL circuit in wave shaping?

Ans. Practically, RL circuit is rarely used if a large time constant is required. This is because the time constant of RL circuit is $= \left(\dfrac{L}{R}\right)$ and to get large time consntant 'L' should be large. This is possible only with iron core inductor which is very large, heavy and expensive compared to capacitor for a

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similar application. Such an inductor is shunted with a large amount of stray capacitance. The iron properties are also non linear. These things cause distortions which is not desirable.

Thus, RL circuit is used only if small time constant is required. For such a case, small and in expensive air core inductor is used.

The transient response of a series RLC circuit with step input.
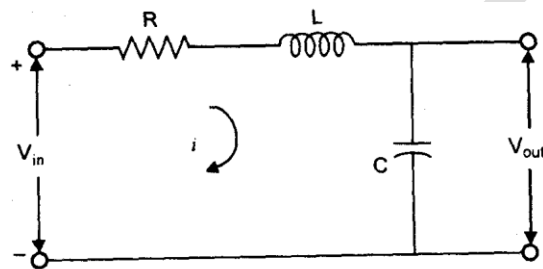
$$i(t) = iR + L\frac{di}{dt} + \frac{1}{C}\int idt$$

$$I(s) = \frac{1}{L} \times \left[\frac{1}{s^2 + \frac{R}{L}s + \frac{1}{LC}} \right]$$

$$s_1, s_2 = \frac{-R}{2L} \mp \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

Case I: When $\left(\frac{R}{2L}\right)^2 > \frac{1}{LC}$;

i.e. $\qquad\qquad R > 2.\sqrt{\frac{L}{C}}$, Roots are real and different.

Circuit is over-damped.

No oscillation in the output.

Case II: When $\qquad R = 2.\sqrt{\frac{L}{C}}$;

both roots are real and equal.

$$S_1 = S_2 = \frac{-R}{2L}$$

$$i(t) = \frac{1}{L}\left[t.e^{-\frac{R}{2L}.t}\right]$$

Circuit is critically damped.

Case III : When $\quad R < 2.\sqrt{\dfrac{L}{C}}$,

Roots are complex and conjugate of each other.
Circuit is under-damped and output will have oscillations.

$$S_1, S_2 = \frac{-R}{2L} \mp 2j\omega_0$$

$$i(t) = \frac{1}{w_0 L}.e^{\left(-\frac{R}{2L}.t\right)}\sin w_0 t$$

And
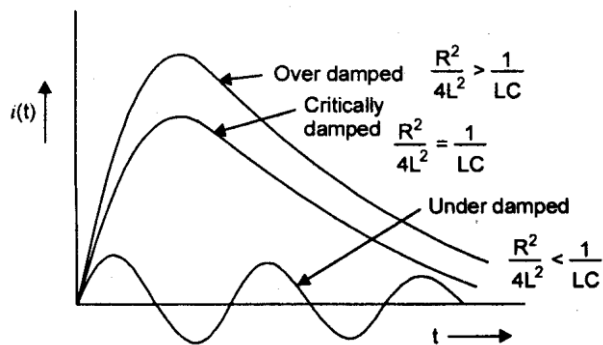
(a) Current Respons
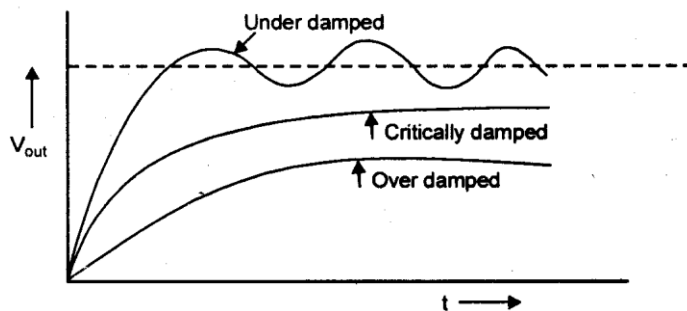
(b)Voltage Response
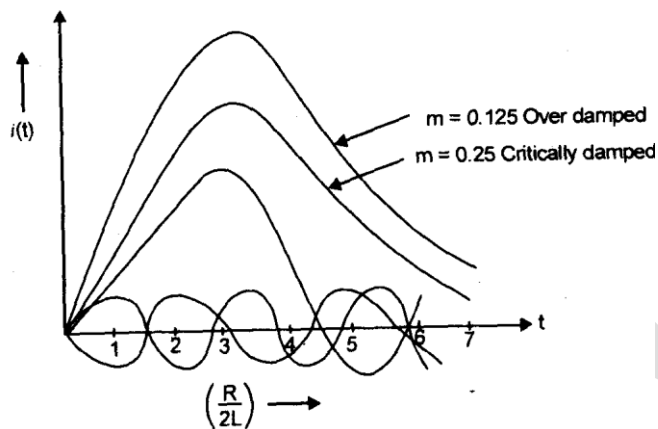
(c)Transient Response of senes RLC ckt. when step input is applied

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Q. 14. Define step response of a RC network. For the network obtain expression for the step response of R_1 9KΩ, $= 1$KΩ, $C_1=100$ pf and $C_2 = 20$ pf. Calculate rise-time with C_1 absent, suggest step to have overshoot free response with C_1 and C_2 present and C_2 fixed in the circuit.

Ans.
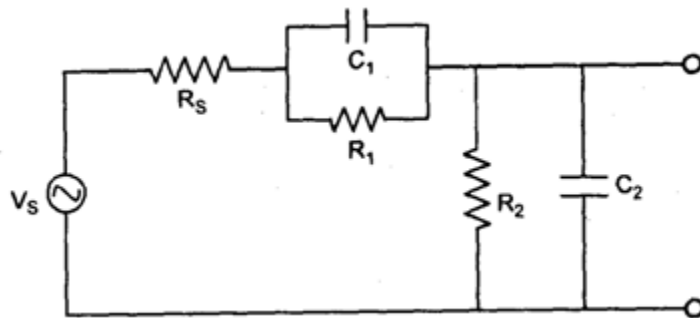
$$\frac{V_0(s)}{V_1(s)} = \frac{R_2}{R_1 + R_2} = \frac{1 + sR_1.C_1}{1 + s.R_{ss}(C_1 + C_2)}$$

Let

$$\frac{R_2}{R_1 + R_2} = k. \frac{1}{R_1 C_1} = a \text{ and}$$

$$\frac{1}{R_{ss}(C_1 + C_2)} = b$$

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Where
$$R_{ss} = R_1 || R_2$$

$$\frac{V_0(s)}{V_s(s)} = k.\frac{b}{a}.\frac{s+a}{s+b}$$

For unit step input, $V(s) = \dfrac{1}{s}$

$$V_0(s) = k.\frac{b}{a}\left[\frac{1}{s+b} + \frac{a}{b}\left(\frac{1}{s} - \frac{1}{s+b}\right)\right]$$

$$V_0(s) = \frac{kb}{a}\left[e^{-bt} + \frac{a}{b}u(t) - \frac{a}{b}.e^{-bt}\right]$$

$$= k.u(t) + k.e^{-st} + \left(1 - \frac{a}{b}\right)$$

$$V_0(t) = \left(\frac{R_2}{R_1+R_2}\right).u(t) + \left(\frac{R_2}{R_1+R_2}\right)\left(\frac{-t}{R_{ss}(C_1+C_2)}\right)$$

(i) Rise time

$$t_r = 2.2 \times (R_1||R_2) \times C_2 = 39.6 \text{ ns}$$

(ii)
$$V_0(t) = 0.1\mu(t) + 0.1e^{-9.3\times10^6 t\left[1-10^8\right]}$$

$$t = 0 \; ; v_0(t) = 0.199$$

(iii) For avoiding overshoot,
$$R_1C_1 = R_2C_2.$$

$$C_1 = R_1||R_2 = \frac{1\times20\times10^{-12}}{9}F = 2.1F.$$

Q.15. Find the output of a ringing circuit consisting of R, L and C when a step voltage is applied to it? What are the uses of ringing circuit?

Ans.
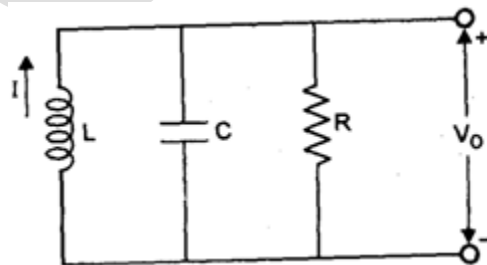
Definition: The RLC circuit which provides nearly undamped oscillations is called ringing circuit.

Consider a R-L-C circuit is as shown below:
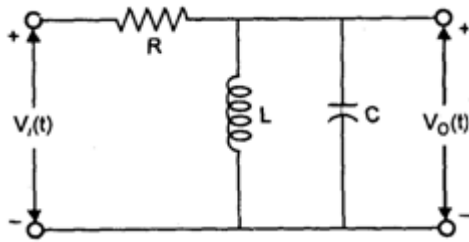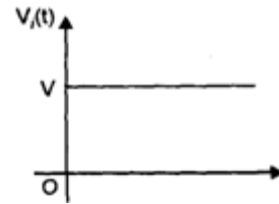
Fig. The RLC ckt.   Fig. The step input

We can combine the parallel combination of the inductor 'L' and the capacitor 'C' into impedance 'Z'.

$$Z = \frac{SL\left(\frac{1}{SC}\right)}{sL + \frac{1}{sC}} = \frac{sL}{1 + s^2 LC}$$

$$I(s) = \frac{V_i(s)}{R + Z}$$

$$V_0(s) = I(s).Z = \frac{V_i(s).z}{R + Z}$$

$$\frac{V_0(s)}{V_i(s)} = \frac{Z}{R + Z} = \left[\frac{\frac{sL}{1 + s^2 LC}}{R + \frac{sL}{1 + s^2 LC}}\right]$$

$$\frac{V_0(s)}{V_i(s)} = \frac{sL}{R(1 + s^2 LC) + sL} = \left[\frac{sL}{RLCs^2 + Ls + R}\right]$$

$$G(s) = \left[\frac{sL}{RLCs^2 + Ls + R}\right] \qquad ...(i)$$

The ratio G(s) is known as the transfer function of the circuit. The characteristics equation of the circuit can be written by equating the denominator polynomial of G(s) o zero as shown in equation (ii)

$$RLCs^2 + Ls + R = 0 \qquad ...(ii)$$

$$s = \frac{-L \pm \sqrt{L^2 - 4R^2 LC}}{2RLC} \qquad ...(iii)$$

$$s = -\frac{1}{2RC} \pm \sqrt{\left(\frac{1}{2RC}\right)^2 - \frac{1}{LC}} \qquad ...(iv)$$

This is a quadratic equation –which can be solved to find its roots, 's_1' and 's_2'. The poles of the transfer function G(s) are same as the roots of the characteristic equation 's_1' and 's_2'.

Let us introduce the dumping constant 'k' and undamped period by equation (v) and (vi)

$$k = \frac{1}{2R}\sqrt{\frac{L}{C}}$$

And
...(v)

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$$T_0 = 2\pi\sqrt{LC} \qquad \qquad \text{... (vi)}$$

When we introduce these value in equation (i) we obtain the following form,

$$s = \frac{-2\pi k}{T_0} \pm j.\frac{2\pi}{T_0}\sqrt{1-k^2}$$

We can see that roots are, purely imaginary, $s = \pm j.\frac{2\pi}{T_0}.$

In this case, the response is an un-damped sinusoidal waveform of period T_0. If k = 1, we can see that the roots are equal, corresponding to the critically damped case.

If k> 1, there would not be any oscillations in the output waveform and the response is said to be over-damped. If k < 1, the output would be a sinusoidal waveform whose amplitude decays with time and the response is said to be under-damped.

The quality factor of the RLC circuit can be written as equation (vii).

$$Q = w_0 RC \qquad \qquad \text{... (vii).}$$

We have already defined the damping constant as

$$k = \frac{1}{2R}\sqrt{\frac{L}{C}}$$

We can verify that,

$$Q = w_0 RC = \frac{2\pi RC}{T_0} = \frac{RC}{\sqrt{LC}} = R.\sqrt{\frac{C}{L}} = \frac{1}{2k}$$

$$Q = \frac{1}{2k} \qquad \qquad ...(viii)$$

$$k = \frac{1}{2Q} \qquad \qquad ...(ix)$$

Now we can see that the damping constant 'k' is inversely proportional to the quality factor 'Q'. Now, we can write the transfer function a (s) written as equation (i) in the following form.
Equation (x)

$$G(s) = \frac{sL}{(s-s_1)(s-s_2)} \qquad \qquad ...(x)$$

We already know as indicated in equation (v) that the poles of the transfer function G(s) are same as the roots of the characteristic equation $'s_1'$ and $'s_2'$.

$$s_1 = -\frac{2\pi k}{T_0} + j.\frac{2\pi}{T_0}.\sqrt{1-k^2}$$

$$s_2 = -\frac{2\pi k}{T_0} - j.\frac{2\pi}{T_0}.\sqrt{1-k^2}$$

Response of the RLC circuit to a step waveform:
The input to this RLC circuit is a step waveform defined below. This waveform is plotted in Fig. (i)(b)

$$v(t) = 0 \; \Big] \text{ for } t < 0$$
$$\quad\;\; = V \Big] \text{ for } t \geq 0,$$

We know the L.T. of the step waveform

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$$v_i(s) = \left[\frac{V}{s}\right]$$

Employing this relation, following equation can be written as

$$\frac{v_0(s)}{v_i(\Delta)} = \left[\frac{sL}{RLC\,s^2 + Ls + R}\right]$$

$$\frac{v_0(s)}{v/s} = \left[\frac{L}{RLC\left(s^2 + \dfrac{1}{RC}s + \dfrac{1}{LC}\right)}\right]$$

$$\frac{V_0(s)}{V} = \left[\frac{L}{RC\left(s^2 + \dfrac{1}{RC}s + \dfrac{1}{LC}\right)}\right]$$

$$\frac{v_0(s)}{V} = \frac{1}{RC\,(s-s_1)(s-s_2)} \qquad\qquad ...(xi)$$

Where 's_1' and 's_2' 'are the roots of 's'.

Slow-decay under-damped Oscillatory Response: —

In this kind of response 'k' is +ve but far less than '1'. In other words, k<<1 and close to zero. Since there is almost no damping in this case, the output response would closely resemble a sinusoidal waveform.
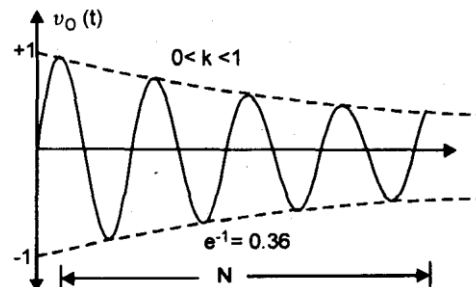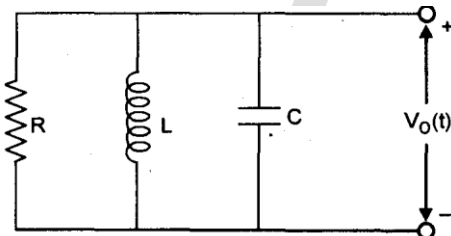
1. RLC circuit functioning   (b) Response of the ringing ckt.

as a ringing circuit.

Fig.2. RLC circuit functioning as a ringing circuit.

The damping constant 'k' is +ive close to zero. Making use of the relation k = 0, we find that both the roots become imaginary

$$s_1 = j\cdot\frac{2\pi}{T_0} \text{ and } s_2 = -j\cdot\frac{2\pi}{T_0}.$$

The RLC circuit shown in Fig. 2(a) operating in this condition is popularly known as the ringing circuit. A typical output response for this case is indicated in Fig. 2(b)

High-pass R-C circuit. Derive for step voltage response of this circuit and show the input-output characteristics of this circuit.

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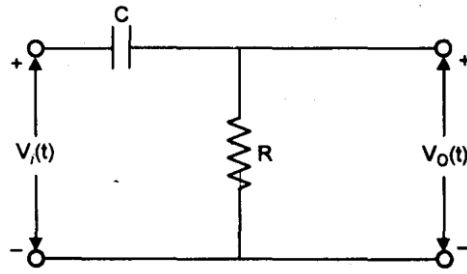
Fig. (a) The RC high-pass fitter

A step waveform is defined by the following expression:

$$v(t)' = \begin{cases} 0 \text{ for } t < 0 \\ V \text{ for } t \geq 0 \end{cases}$$
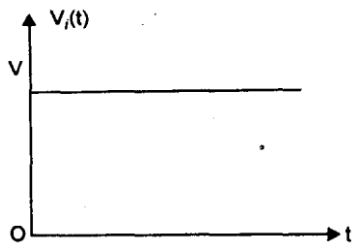
Fig. (ii)(a)The step waveform
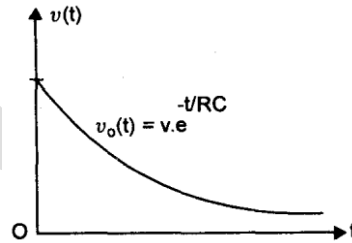
Fig. (b) Output waveform of R.C. high pass fitter.

The generalised transient expression has been derived at,

$$v_0(t) = v_0(\infty) + [v_0(0) - v_0(\infty)].e^{-t/RC} \qquad \ldots(1)$$

The expression for v (t) can be found if we know the initial conditin v (0) final condition $v(\infty)$, and the time constant 'RC' of the circuit.

$$v_0(t) = 0 + (V - 0).e^{-t/RC}$$
$$v_0(t) = V.e^{-t/RC} \qquad \ldots (2)$$

The output waveform for the step input to an RC high pass fitter is an exponentially falling waveform as shown in Fig. 2(b). This response reaches almost zero after a time 't' greater than '5RC'.

Practical step Input waveform: ─

It has to be emphasized here that it is not possible to obtain a step waveform as defined by equation (2) plotted in Fig. 2(b). The infinite slope of this waveform at t = 0 can't be attained in reality. Limited ramp waveform and exponential waveform are used as substitutes for the step input waveform in practice. The limited ramp waveform is defined as,

$$v(t) = \begin{cases} (V/T) \, t \text{ for } 0 \leq t \leq T \\ V \qquad \text{ for } t > T \end{cases}$$

When T is very small, the limited ramp waveform closely resembles as a step waveform. The exponential waveform defined as

---

Consider an R-C circuit shown in Fig - 1. A symmetrical square wave shown in Fig - 2 is applied as input to this circuit. Obtain an expression for peak-to peak value of the output voltage. What is peak-to-peak voltage for τ =RC.

Ans. Since the input waveform is periodic and symmetrical with zero mean value, the output waveform will also be symmetrical and periodic with zero mean value.
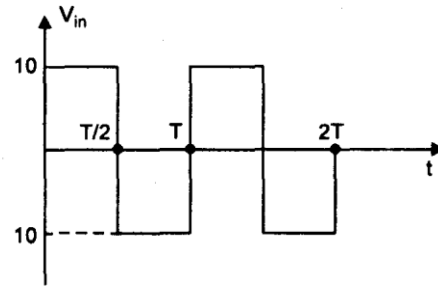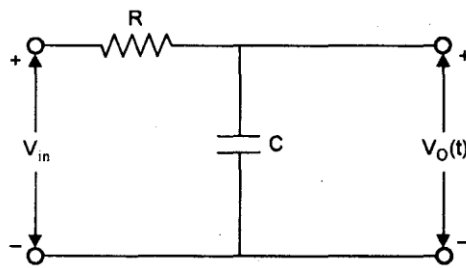
Hence (i) $$V_0|_{(t=0)} = -V_0|_{(t=T/2)}$$

(ii) Output waveform in the time $\left[\dfrac{T}{2} < t < T\right]$ is inverted replica of the output waveform in time interval $\left[0 < t < \dfrac{T}{2}\right]$; but shifted by $\left(\dfrac{T}{2}\right)$

From the equation

$$\left[V_0|_{(0<t<T)}\right] = \left[+V_0|_{(t=0)}\right] + \left[E_1 - V_0|_{(t=0)}\right]\left[1 - e^{\frac{-T}{2RC}}\right]$$

... (2)

We get

$$V_0|_{\left(0<t<\frac{T}{2}\right)} = V_0|_{(t=0)} + E - V_0|_{t=0}\left[1 - e^{\frac{-T}{2RC}}\right]$$

$$V_0|_{\left(t=\frac{T}{2}\right)} = V_0|_{(t=0)} + E - V_0|_{t=0}\left[1 - e^{\frac{-T}{2RC}}\right]$$

Substituting

$$V_0|_{\left(t=\frac{T}{2}\right)} = -V_0|_{(t=0)}$$

$$V_0|_{\left(t=\frac{T}{2}\right)} = -V_0|_{\left(t=\frac{T}{2}\right)} + E + V_0|_{\left(t=\frac{T}{2}\right)}\left[1 - e^{\frac{-T}{2RC}}\right]$$

We get

Solving $V_0|_{\left(t=\frac{T}{2}\right)}$, we get

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$$V_0\Big|_{\left(t=\frac{T}{2}\right)} = \frac{10.\left(1-e^{-\frac{T}{2RC}}\right)}{\left(1+e^{-\frac{T}{2RC}}\right)}$$

Substituting E 10 Volts, τ = RC= T.

$$V_0\Big|_{\left(t=\frac{T}{2}\right)} = \frac{10.\left(1-e^{-\frac{\tau}{2}}\right)}{\left(1+e^{-\frac{\tau}{2}}\right)} = \frac{10 \times 0.394}{1.606}$$

$$= \frac{3.94}{1.606} = 2.45 \text{ Volt}$$

Peak to peak value of output voltage = 2 x 2.45 4.90 Volts.

. Design an RC differentiator network of square pulses of 1ms repetition rate and 1OV amplitude. It is desired to have output trigger pulses of 8V amplitude. Assume source resistance of 50Ω and load resistance of 50Ω .

Ans. Effective time constant

$$= 0.1 \times T= 0.1 \times 1ms \; 100^u s$$

At time   t =0

$$V_{out}(0) = V_{in}\frac{R}{R+R_s}$$

$$= \frac{10 \times R}{R+50} = 8V$$
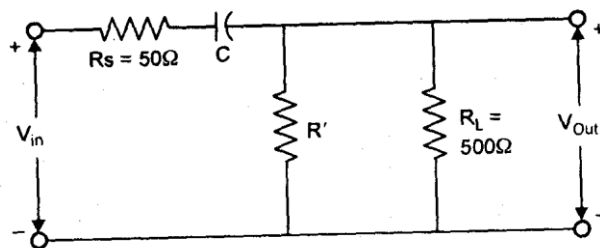
Fig. R—C differentiator

So   2R = 400 Q

                        R = 200 Q

Effective resistance

$$R_{eff} = 200 + 50 = 250\,\Omega$$
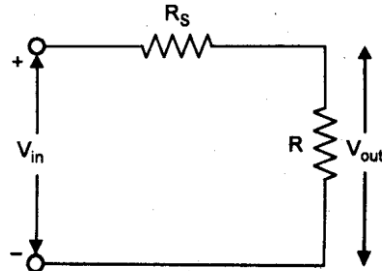
$$\tau = R_{eff} \times c = 100^\mu\,s$$

Or $c = \dfrac{\tau}{R_{eff}}$ Fig. Equivalent circuit of circuit shown in above

$$= \frac{100 \times 10^{-6}}{250} = 0.4\,\mu F$$

$$R = \frac{R_L \times R'}{R_L + R'} = 200$$

Also

$$\frac{500R'}{500 + R'} = 200$$

Or

$$R' = \frac{500 \times 200}{300} = 333\,\Omega$$

⇒ Or
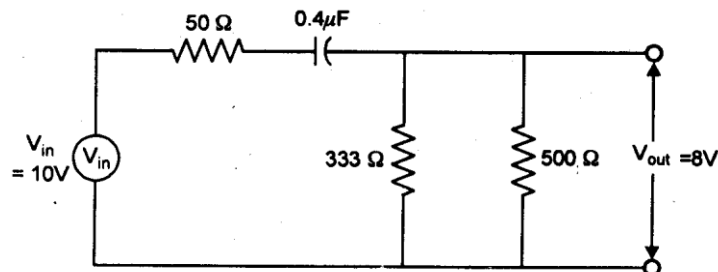
Fig. Differentiator circuit.

For the circuit shown, calculate and $V_0(t)$, $V_i(t) = 30\,u(t)$.

Ans. Given

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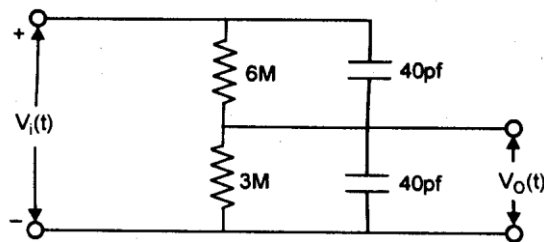
$$V_i(t) = 30\,\mu(t)$$
$$V_0(t) = ?$$

Final output voltage

$$V_0(0^+) = \left(\frac{C_1}{C_1 + C_2}\right).v_i(t) = \left[\frac{40 \times 10^{-12}}{40 \times 10^{-12} + 40 \times 10^{-12}}\right].[30]$$

$$= \frac{1}{2} \times 30 = 15 \text{ volts}$$

Initial output voltage

$$v_0(\infty) = \left(\frac{R_2}{R_1 + R_2}\right).v_i(t) = \left[\frac{3 \times 10^6}{3 \times 10^6 + 6 \times 10^6}\right].[30]$$

$$= \frac{\cancel{3}}{\cancel{9}} \times \cancel{30}^{10} $$

$$_3 \qquad = 10 \text{ Volts}$$

Overshoot, $\Delta v_0(t) = [v_0(t) \text{ (final)} - v_0(t) \text{ (initial)}]$

$$= [v_0(0^+) - v_0(\infty)] = 15 - 10 = 5 \text{ volts.}$$

Obtain the response of a high-pass circuit to ramp and square wave input. Discuss the effect of RC on the response.

Ans. Response of a high-pass RC circuit to Ramp input:
A waveform which is defined as:

$$v_i(t) = \begin{cases} 0 & \text{for } t < 0 \\ \infty t & \text{for } t > 0 \end{cases} \qquad \dots (1)$$

$$v_0(t) = i(t).R,$$

Then output is
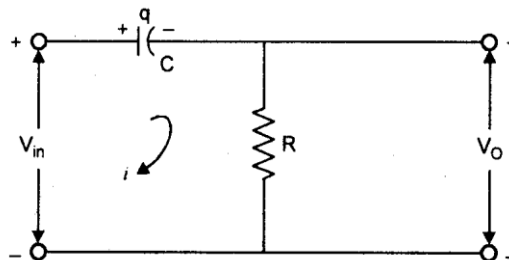
Fig. High pass RC circuit

$$\frac{dv_i(t)}{dt} = \frac{v_0(t)}{RC} + \frac{dv_0(t)}{dt}$$

…(2)

Which becomes

$$\alpha = \frac{v_0(t)}{RC} + \frac{dv_0(t)}{dt}$$

… (3)

This equation has the solution for v_0 (t) at t = 0. Taking Laplace Transform on both sides, equation (3) becomes,

$$\frac{\alpha}{s} = \frac{v_0(s)}{RC} + sV_0(s)$$

$$= V_0(s)\left[s + \frac{1}{RC}\right]$$

$$v_0(s) = \frac{\alpha}{s\left[s + \frac{1}{RC}\right]}$$

By taking Inverse Laplace Transform,

$$v_0(t) = \propto RC\left[1 - e^{-t/RC}\right]$$

…(4)

For times 't' <<RC,

$$v_0(t) = \alpha t\left[1 - \frac{t}{2RC} + ...\right]$$

…(5)

The output signal falls away slightly from the input. As a measure of the departure from linearity let us define the transmission error $"e_t"$., as the difference between input and output divided by the input. The error at a time t = T, is then

$$e_t = \frac{v_i(\tau) - v_0(\tau)}{v_i(\tau)}$$

…(6)

$$e_t = \frac{T}{2RC} = \pi f_1 T$$

…(7)

where f1 = $\left(\frac{1}{2\pi RC}\right)$ is again the low frequency 3-dB point. For example, if we desire to pass 2-m sec sweep with less than 0.1 percent duration from linearity the above equation yields,

$$f_1 < 0.16 \text{ Hz}$$

Or   RC>1sec
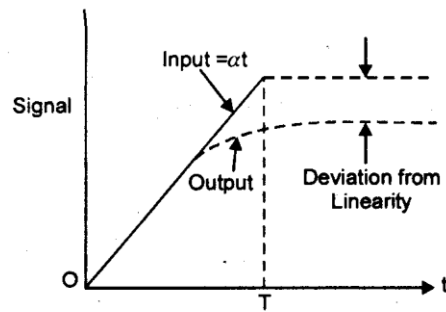
Fig. 1 (a) Response of a high-pass RC circuit to a ramp voltage for $\dfrac{RC}{T} >> 1$
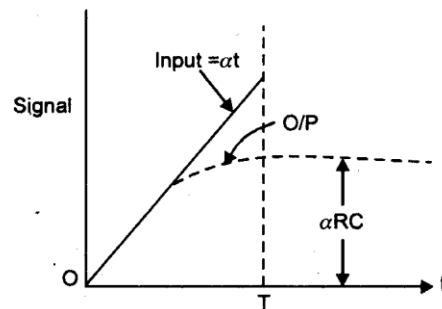
Fig. 1 (b) Response to a ramp voltage for $\dfrac{RC}{T} << 1$

For large values of 't' in comparison with. 'RC' and the output approaches the constant value 'aRC', as indicated in Fig. I (b) and equation (4).
RC

For $\dfrac{RC}{T} >> 1$, from equation 4, we can write

$$v_0(t) = \alpha t$$

… (8)

For $\dfrac{RC}{T} << 1$, from equation (4), we can write $v_0(t) = RC\alpha$.

Find the input impedance of RC differentiating circuit and compare it with that of RL differentiating circuit.

Ans. A Circuit gives an output voltage proportional to derivation of input is known as differentiating circuit.

i.e.
$$\text{output} \propto \frac{d}{dt}(\text{input})$$

The conditions to be fulfilled are:
(1) RC << T, time constant of circuit should be much smaller.
(2) X_C Should be smaller than wR.

If v_{in} = input voltage, i = Resultant current,

$$q = CV_C \qquad V_C = \text{instantaneous value of capacitor.}$$

$$i = \frac{dq}{dt} = \frac{d}{dt}q = \frac{d}{dt}(CV_C)$$

$$= C.\frac{d}{dt}V_C$$

The voltage across the capacitor equal to input voltage

$$i = C.\frac{d}{dt}V_{in}$$

$$V_{out} = iR = RC.\frac{d}{dt}v_{min}$$

$$v_{out} \propto \frac{d}{dt}(v_{in})$$

$$\propto \frac{d}{dt}$$

i.e. Output $\quad\propto\dfrac{d}{dt}$ (input)

(a) Low Pass   (b) High Pass
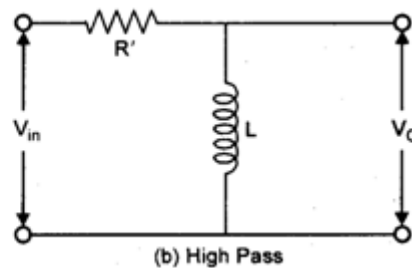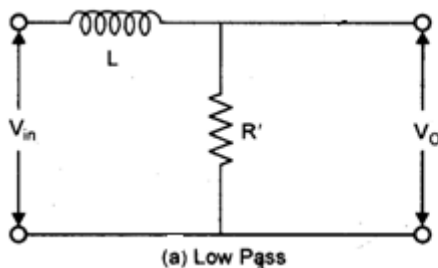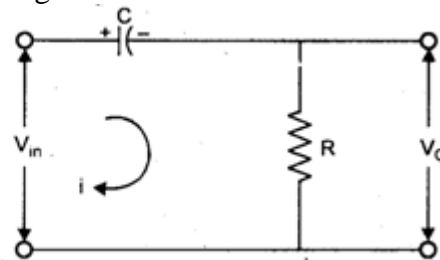
At low frequencies the reactance of the inductor is very small so the output across 'R' is almost equal to the input. With the increase in frequency, reactance of the inductor increase and therefore, the signal is attenuated. At very frequencies the output becomes almost zero. Thus, the circuit (a) acts as a low – pass filter. The circuit depicted in (b)
acts as a high – pass circuit because at low frequencies the output is very small and with the increase in frequency, the output increases. At very high frequencies, the output becomes almost equal to the input.

Ringing Circuit.

Ringing circuit those which generate a sequence of pulses spared regularly. In timing operations in automatic control circuits.

Ringing circuits have undamped oscillations dependind on the number of ringing duty cycles required. It is sometime required to obtain the values of 'Q' of a circuit.

Which is to ring for a given number of 'N' cycles before the amplitude falls to $\left(\dfrac{1}{e}\right)$ of its initial value.
From equation

$$\frac{v_{out}}{v_{in}} = \left(\frac{2k}{\sqrt{4-k^2}}\right).e^{-2\pi kx}.\sin 2\pi\sqrt{(1-k^2x)} \qquad \ldots (1)$$

Where $\qquad x = \left(\dfrac{t}{T_0}\right)$

It is seen that decrement is obtained

Where $2\pi k x = 1$

Since $x = \dfrac{t}{T_0} = \dfrac{NT_0}{T_0}$ = N and

$k = \dfrac{1}{2Q}$, We have

$$Q = \pi N \qquad\qquad\qquad \dots (2)$$

For Q =12 the circuit will ring for $\dfrac{Q}{\pi} \approx 4$ cycles before the amplitude falls to 37% of its initial value.

UNIT-II

Non-Linear Wave Shaping

   Diodes, transistors and field-effect transistors (FETs) can be used as linear circuit elements if the operation is restricted to that limited region in the characteristic in which it can be approximated to a straight-line characteristic (small-signal conditions). However, when the input is increased further (under large-signal conditions), these devices no longer behave as linear circuit elements; and the operation can go into the nonlinear region of the characteristic. When these non-linear circuit elements are used in waveshaping applications, the resultant process is termed *non-linear wave shaping*. In communication systems, sometimes it becomes necessary to eliminate a portion of the input signal, either at a single level or at two independent levels. The circuits that accomplish this task are called clipping circuits. These circuits can also be used to eliminate the noise associated with an input signal. Such clipping circuits are called noise clippers. The parameters of these devices can change with variations in temperature. Thus, in applications where precision is required, it becomes necessary to provide temperature compensation so that temperature variations do not influence the behaviour of the circuit.

Amplitude comparators (also called comparators) are circuits that compare an input with a reference signal and deliver a high output the moment the input reaches the reference level. A simple diode comparator circuit is discussed and possible techniques to improve the sharpness of the break region are presented in this chapter. A comparator circuit may be used to control other circuits with the help of its output; the instant the input reaches a predefined reference level.

CLIPPING CIRCUITS

Clipping circuits select that part of the signal which lies above and below a reference level. Depending on whether the diode is connected in series with the load or in shunt with the load, these circuits are called either series-clipping circuits or shunt-clipping circuits.
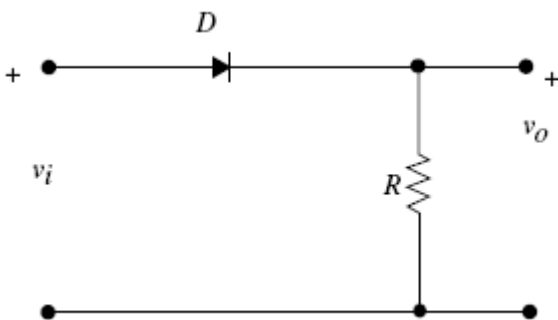
FIGURE 4.7(a) Series clipper that clips the negative half-cycles
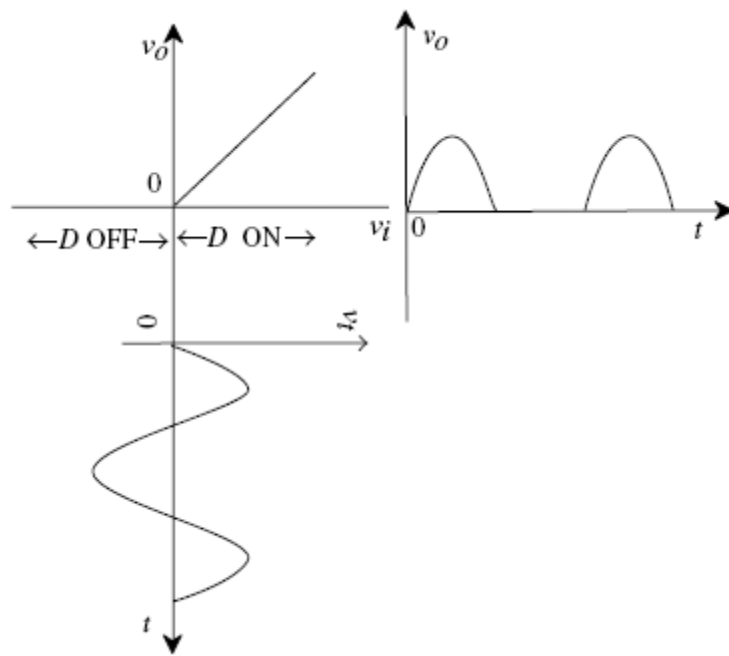
FIGURE 4.7(b) The transfer characteristic, input waveform and output waveform of a series clipper that clips negative half-cycles

Series Clippers

Consider the series-clipping circuit shown in **Fig. 4.7(a)** and its transfer characteristic (a plot that gives the relationship between the input and the output voltages) with input and output waveforms in **Fig. 4.7(b)**. When v_i is positive, D conducts and the input signal is transmitted to the output, $v_o = v_i$ When v_i is negative, $v_o = 0$. There is no transmission of the signal as the diode is assumed to be ideal. The output is in the form of half-cycles, similar to the output of a half-wave rectifier; in fact, it is a half-wave rectifier.

Consider another clipping circuit shown in **Fig. 4.8(a)** and its transfer characteristic with input and output waveforms in **Fig. 4.8(b)**. When v_i is negative, D conducts and the input v_i is transmitted to the output (i.e., $v_o = v_i$). When v_i is positive, D is OFF and $v_o = 0$. The signal is not transmitted to the output. The output once again is in the form of half-cycles.

In our discussion so far, we have assumed the diode to be ideal and have neglected the influence of the transition capacitance C_T that exists between the anode and the cathode of a reverse-biased diode. We now take into account this parameter to understand how this affects the output of a series clipper. Consider the circuit shown in **Fig. 4.8(a)** when reverse-biased (during the positive half-cycle), to which, instead of a sinusoidal signal, a square-wave input is applied. So far we have

assumed that during the period when the diode is OFF, there is no transmission. However, on account of the transition capacitance C_T being present, the circuit now behaves as a high-pass circuit [see Fig. 4.8(c)] and the input can now be transmitted to the output, though with distortion. Also, even if a sinusoidal signal is applied as input, at high frequencies, the capacitor offers a smaller reactance due to which the input can be transmitted to the output. This is the major limitation of a series clipper. Thus, a series clipper works best at low frequencies.
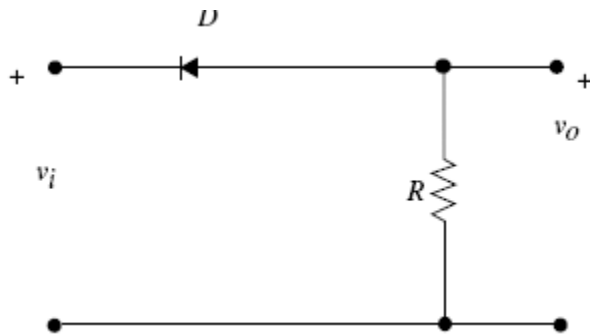
FIGURE 4.8(a) Series clipper that clips positive half-cycles
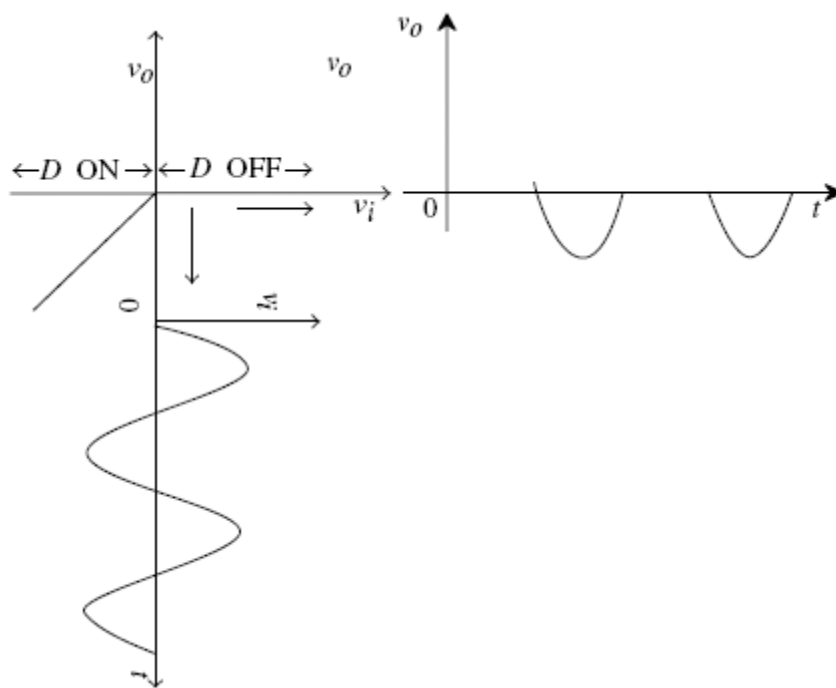
FIGURE 4.8(b) The transfer characteristic, input waveform and output waveform of a series clipper that clips positive half-cycles
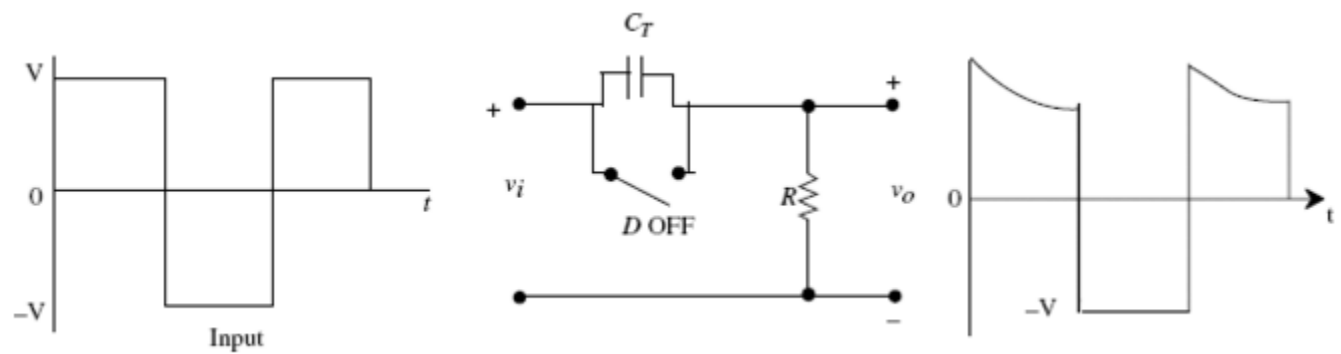
FIGURE 4.8(c) Series clipper that is expected to eliminate positive half-cycles

Base Clipper. If a battery (V_R) is included in the series-clipping circuit, such that the diode is connected in series with the load, as shown in **Fig. 4.9(a)**, these circuits are called biased series clippers. The circuit in **Fig. 4.9(a)** clips the positive going input at its base, so it is also referred to as a base clipper.

Assume that the diode is ideal in the circuit shown in **Fig. 4.9(a)**.

For $v_i < V_R$, D is OFF; hence, $v_o = V_R$. The resultant circuit is shown in **Fig. 4.9(b)**.

For $v_i \geq V_R$, D is ON; hence, $v_o = v_i$. The resultant circuit is shown in **Fig. 4.9(c)**.

The transfer characteristic is shown in **Fig. 4.9 (d)**.

In the output of this circuit, the base portion of the input during the positive half-cycle is eliminated and only the positive peak is available when the input is either more than or equal to V_R. Hence, the name base clipper. The battery V_R is assumed to have zero internal resistance. However, in practice, any voltage source will have some internal resistance R_S which appears in series with the battery. Now, as this R_S in the present case appears in series with R, where $R >> R_S$, the performance of the circuit is not affected. This could be termed as an advantage of series clippers.
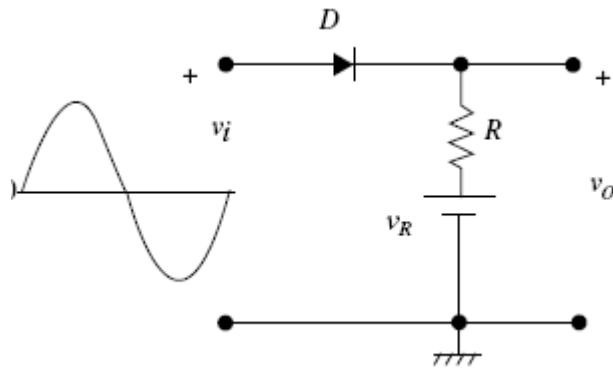
FIGURE 4.9(a) A base clipper
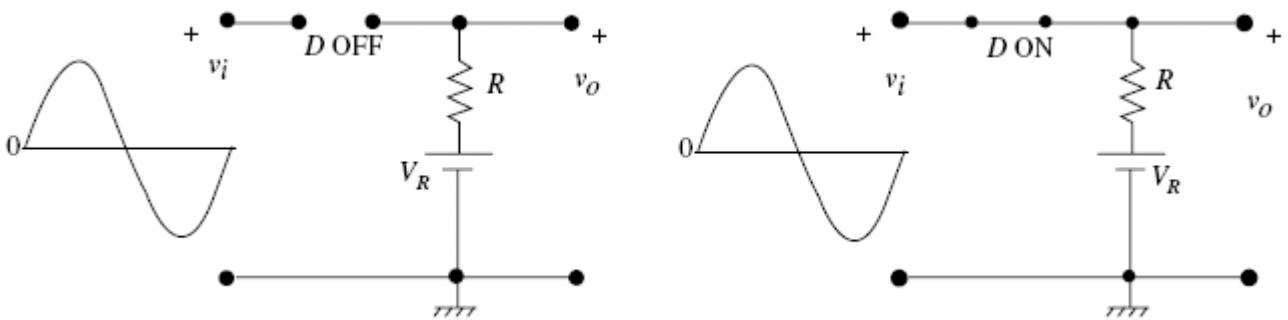
FIGURE 4.9(b) A base clipper with D OFF; and (c) with D ON

Positive-Peak Clipper. Consider the circuit shown in **Fig. 4.10(a)**. As this circuit eliminates the positive peak of the input at the output, it is called a positive peak clipper.

For $v_i < V_R$, D is ON, and the resultant circuit is shown in **Fig. 4.10(b)**. Hence, $v_o = v_i$. And for $v_i > V_R$, D is OFF, as shown in **Fig. 4.10(c)**. Hence, $v_o = V_R$. Thus, the transfer characteristic, the input and output waveforms are as shown in **Fig. 4.10(d)**. In the output of the circuit, the positive peak of the input above V_R is eliminated. Hence, this circuit is called a positive peak clipper.
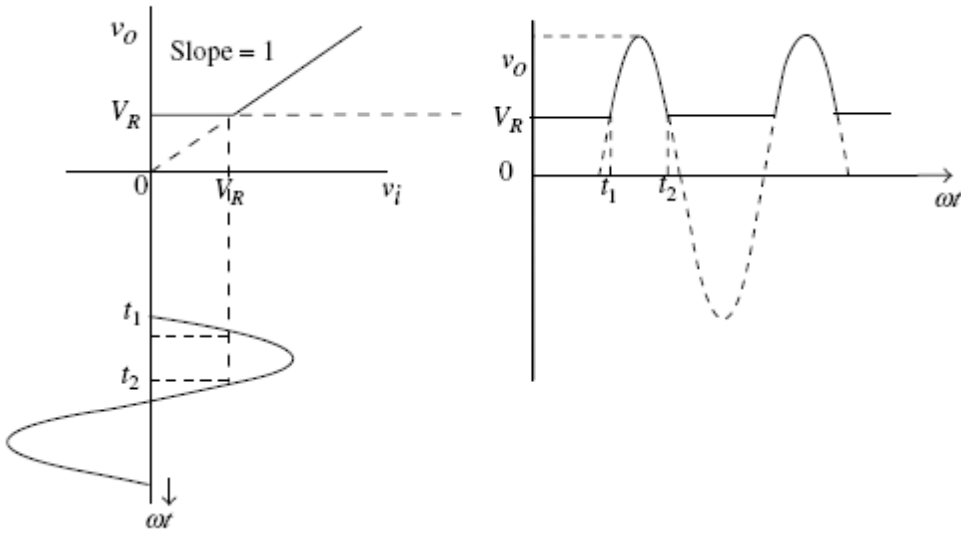
FIGURE 4.9(d) The transfer characteristic of a base clipper with input and output waveforms
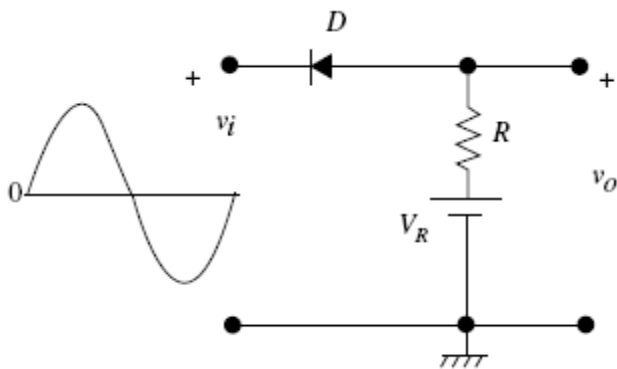
FIGURE 4.10(a) Positive-peak clipper
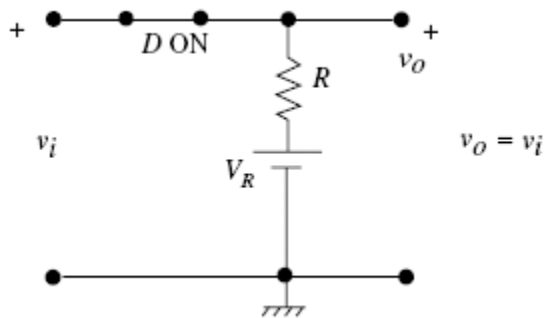
FIGURE 4.10(b) Circuit of Fig. 4.10(a) when D is ON
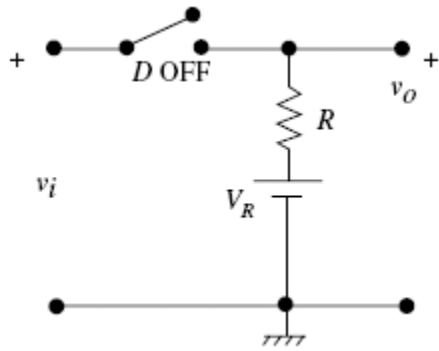
FIGURE 4.10(c) Circuit of Fig. 4.10(a) when D is OFF
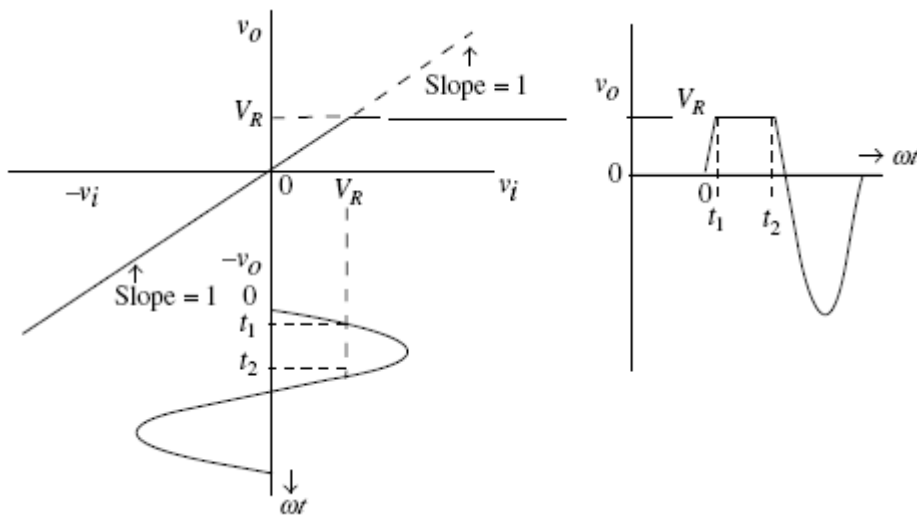
FIGURE 4.10(d) Transfer characteristic of a positive peak clipper in Fig. 4.10(a) with input and output waveforms

Shunt Clippers

A shunt clipper is one in which the diode is used as a shunt element. Consider a simple shunt clipper shown in Fig. 4.11(a). As long as the input is positive, D conducts and the output $v_o = 0$.When the input is negative, D is OFF and an open circuit. The input is transmitted to the output. The transfer characteristic, the input and output waveforms are shown in Fig. 4.11(b). This circuit clips the positive half-cycle. The same thing is done by the circuit shown in Fig. 4.8(a). The only difference is that the former is a series clipper and the latter a shunt clipper.
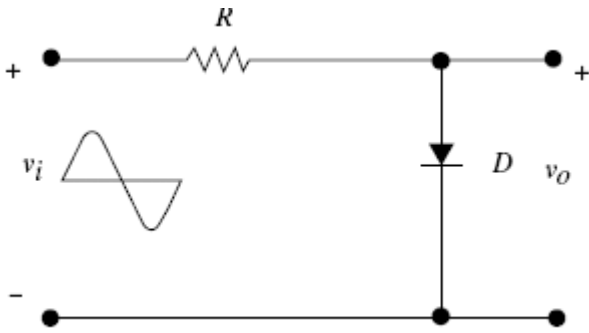
FIGURE 4.11(a) A shunt clipper that clips the positive half-cycle
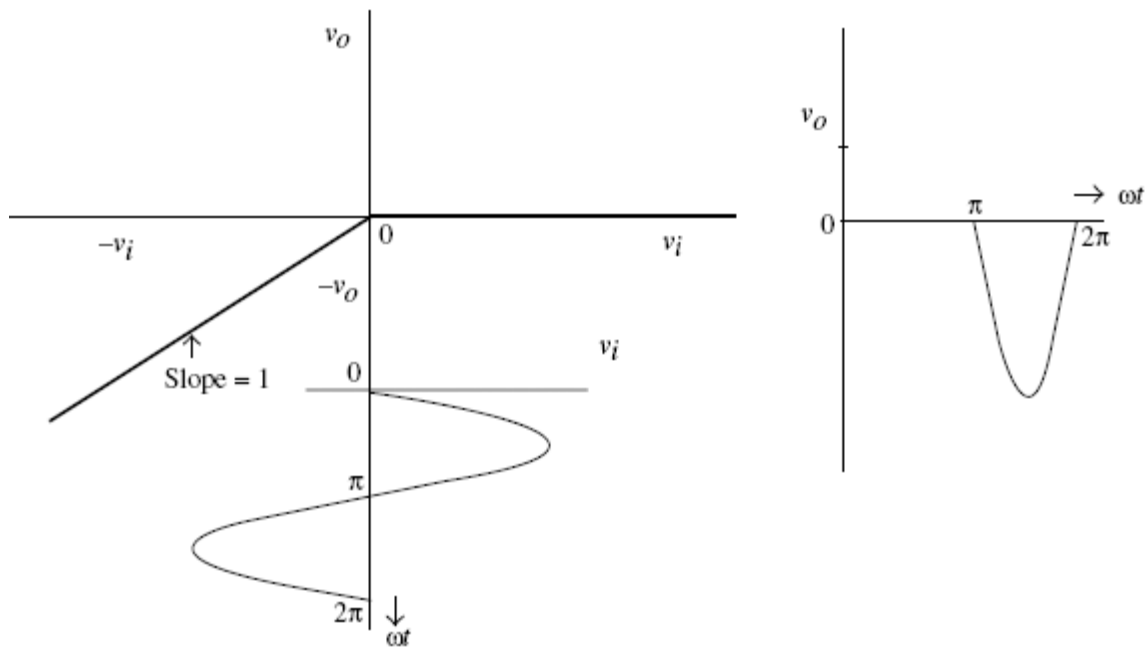
FIGURE 4.11(b) The transfer characteristic, the input and output waveforms
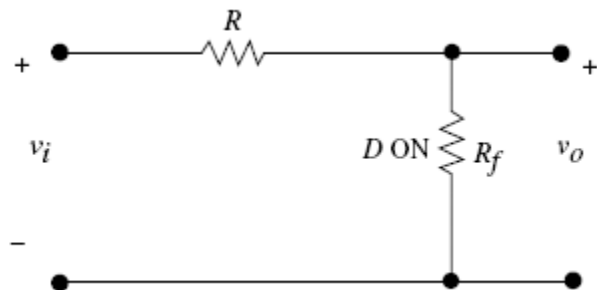
FIGURE 4.11(c) The shunt clipper in Fig. 4.11(a) when D in ON and R_f is considered

Till now we assumed that the diode to be ideal, that is, forward resistance of the diode was taken to be zero. A practical diode, however, has typically R_f in the range of 50 Ω to 100 Ω. Therefore,

when D is ON, with R_f taken into account, the circuit is as shown in Fig. 4.11(c). In this circuit: $v_o = v_i R_f/(R_f + R)$.

This means that though the output is expected to be 0, there is a small sinusoidal swing at the output. This is one limitation of a shunt clipper. When D is OFF, it should ideally behave as an open circuit. But in a reverse-biased diode, we have transition capacitance. Taking C_T into account, Fig. 4.11(a) can be redrawn as shown in Fig. 4.11(d).

Now, when the diode is OFF, with a square wave as the input, we ideally expect the negative half-cycle of the input only at the output. However, when C_T is considered, the shunt clipper is a low-pass circuit. Hence, the output would rise with a time constant RC_T. This is another limitation of a shunt clipper. Consider an alternative form of the shunt clipper as shown in Fig. 4.12(a). The transfer characteristic along with the input and output waveforms is shown inFig. 4.12(b). The negative half-cycle is completely eliminated as is done by the circuit in Fig. 4.7(a).

Now let us consider a slightly different shunt clipper called a biased shunt clipper that clips the positive half-cycle of the input waveform at a reference level V_R [see Fig. 4.13 (a)]. For the circuit in Fig. 4.13(a), the transfer characteristic is drawn in Fig. 4.13(b).
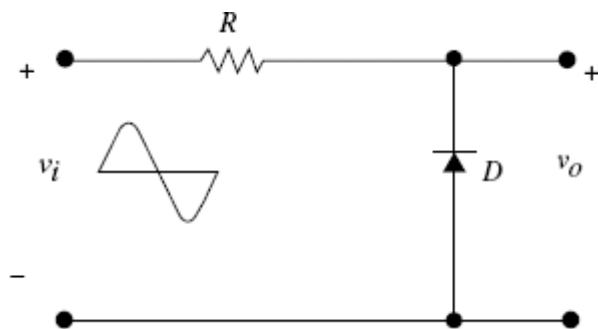
When $v_i < V_R$, D is OFF, hence, $v_o = v_i$.
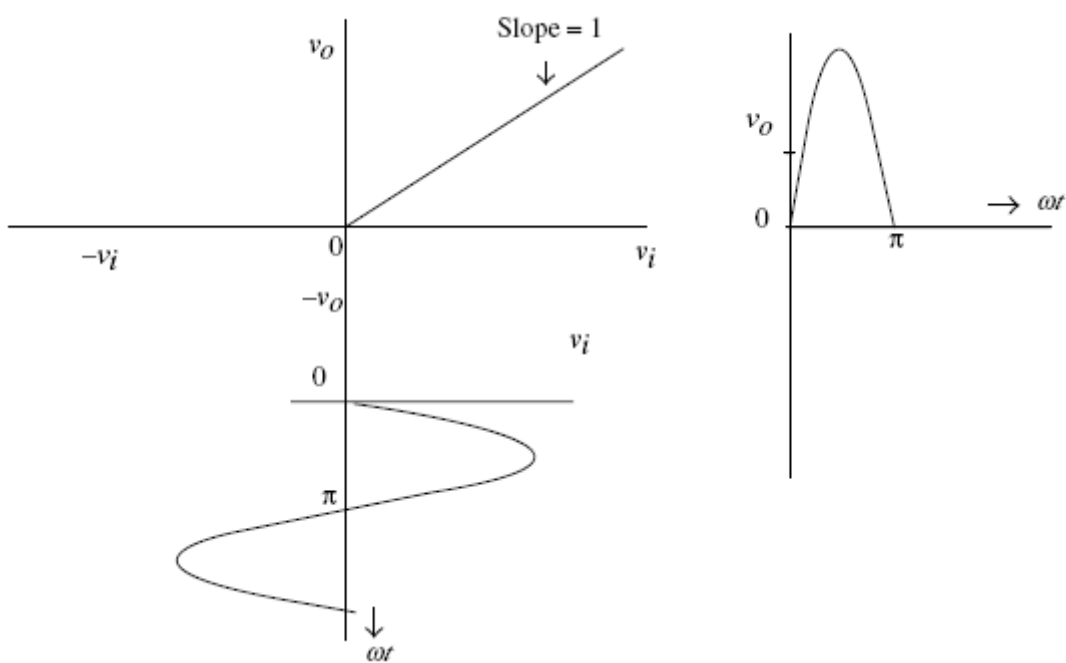
When $v_i \geq V_R$, D is ON, hence, $v_o = V_R$.

To calculate and plot the output of the clipping circuit shown in Fig. 4.13(a), consider a sinusoidal input signal varying as $V_m \sin \omega t$.
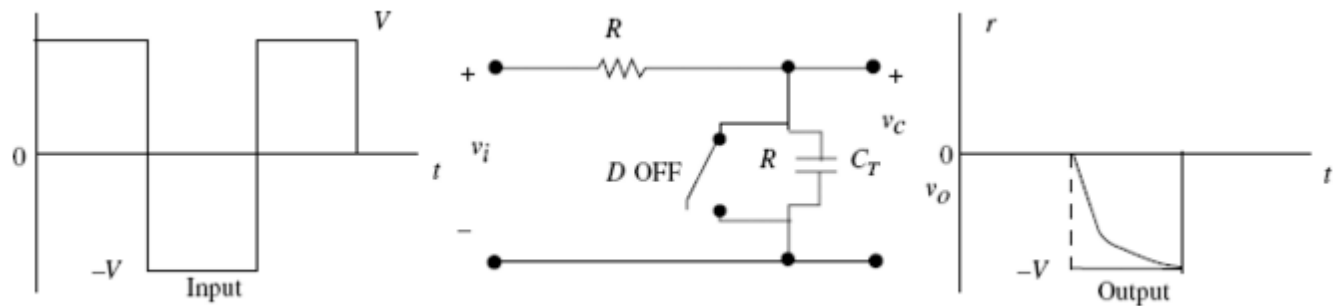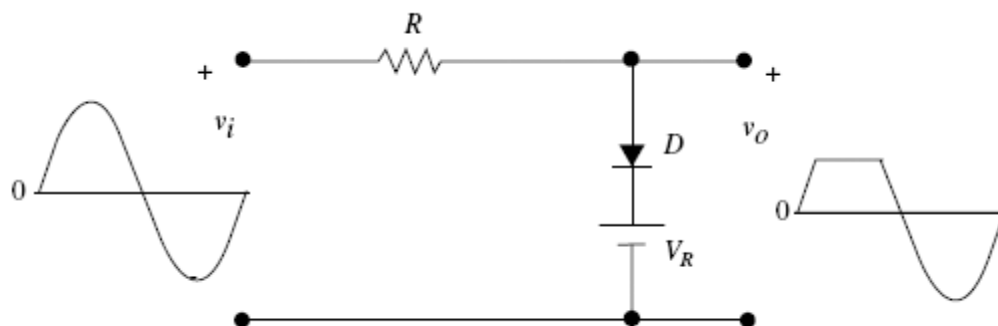

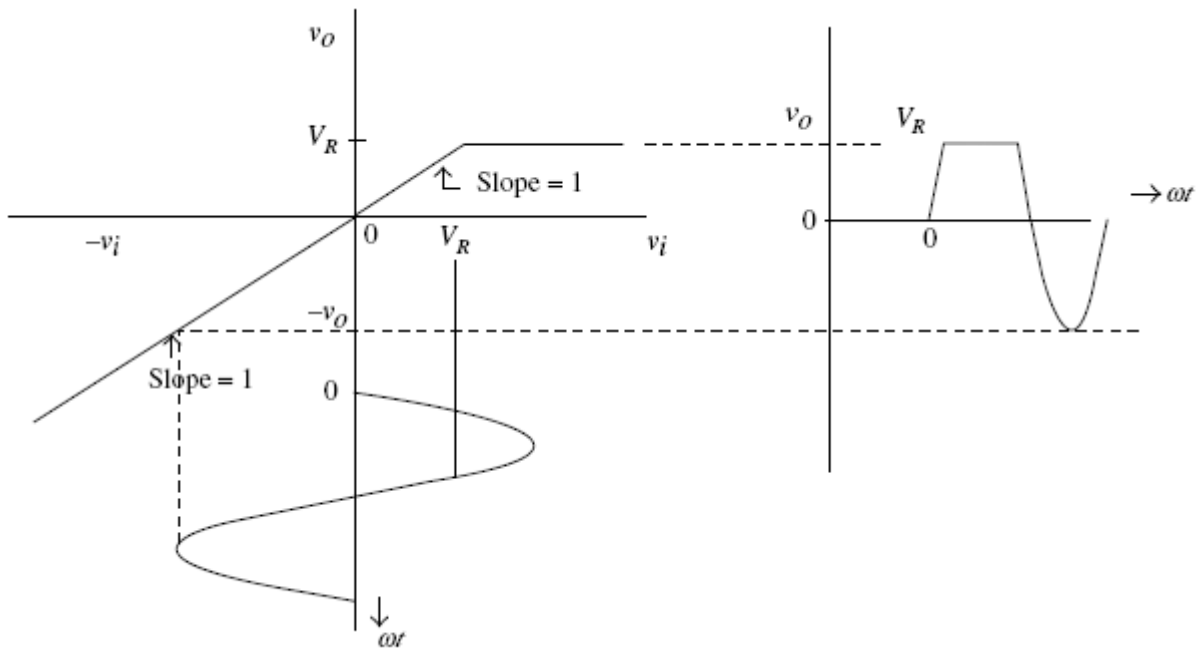**FIGURE 4.11(d)** The shunt clipper considering C_T

FIGURE 4.12(a) A shunt clipper that clips the negative half-cycle

FIGURE 4.12(b) The transfer characteristic of the clipper in Fig. 4.12(a)

FIGURE 4.13(a) A positive peak clipper

FIGURE 4.13(b) The transfer characteristic with input and output waveforms of the circuit in Fig. 4.13(a)

Case 1

When the diode is ideal, its R_f is 0 and R_r is ∞.

$v_i < V_R$, D is OFF, $v_o = v_i$

$v_i \geq V_R$, D is ON, $v_o = V_R$

The output is as shown in Fig. 4.13(b).

Case 2 When the diode is not ideal and has finite forward and reverse resistances

1.   When the diode is ON, it has a forward resistance R_f. For $v_i > V_R$ the resultant circuit is as shown in Fig. 4.13(c). Here:

$$v_o = (v_i - V_R) \times \frac{R_f}{R + R_f} + V_R$$

Thus, v_o is maximum when v_i is maximum that is when $v_i = V_m$.
If $V_m \approx 2V_R$

$$v_{o(\text{max})} = (2V_R - V_R) \times \frac{R_f}{R + R_f} + V_R = V_R\left(\frac{R_f}{R + R_f} + 1\right) = V_R\left(\frac{R + 2R_f}{R + R_f}\right)$$

If the source V_R has an internal resistance R_s, $v_{o(\text{max})}$ computed using $R_{f1} = (R_f + R_s)$, instead of R_f. R_S will influence the slope of the transfer characteristic. This could be another drawback of a shunt clipper.
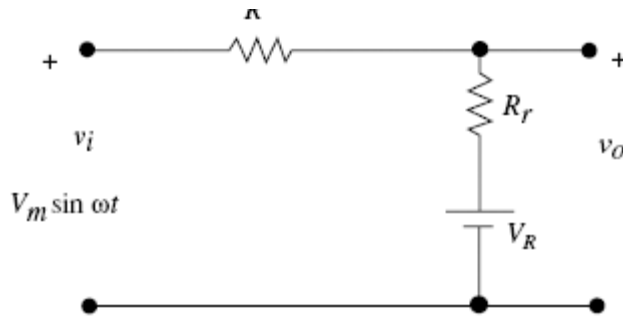
2.   When $v_i < V_R$, the diode is OFF and the reverse resistance of the diode is R_r. The resultant circuit that enables us to calculate v_o is given in Fig. 4.13(d).

v_o is minimum when v_i is at its negative maximum, i.e., $v_i = -V_m \approx -2V_R$. Therefore,

$$v_{o(\text{min})} = (v_i - V_R) \times \frac{R_r}{R + R_r} + V_R = (-2V_R - V_R) \times \frac{R_r}{R + R_r} + V_R$$

$$= (-3V_R) \times \frac{R_r}{R + R_r} + V_R = V_R\left(1 - \frac{3R_r}{R + R_r}\right) = V_R\left(\frac{R + R_r - 3R_r}{R + R_r}\right)$$

$$V_{o(\text{min})} = V_R\left(\frac{R - 2R_r}{R + R_r}\right)$$

In this case, R_S of the battery will not influence the output in any way because $R_r \gg R_S$. R is chosen based on the following considerations.
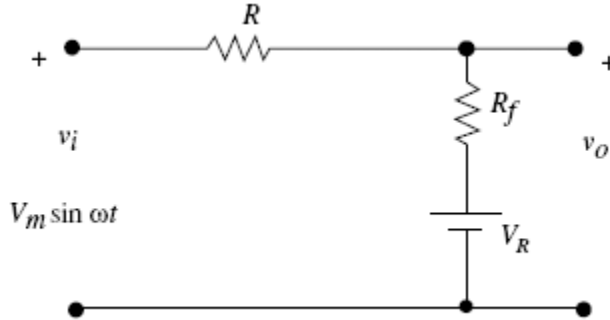
FIGURE 4.13(c) Circuit when D is ON and has a finite forward resistance R_f

FIGURE 4.13(d) Circuit when D is OFF and has a finite reverse resistance R_r

Consider the circuit shown in Fig. 4.11(a). During the transmission period, the diode is OFF, offering a large reverse resistance R_r. For the input to be transmitted to the output

terminals with negligible loss of signal, R_r should be much larger than R. This requirement says that:

$$R_r = aR$$

or

$$R = \frac{R_r}{a}$$

where a is a large number. Therefore,

When the diode is ON, the output signal is small and is said to be attenuated. This condition stipulates that R should be significantly larger than R_f, the forward resistance of the diode. This requirement means

$$R = aR_f$$

From Eqs. (4.2) and (4.3):

$$R^2 = R_r R_f$$

or

$$R = \sqrt{R_f R_r}$$

R is chosen as the geometric mean of R_f and R_r.

$$a = \sqrt{\frac{R_r}{R_f}}$$

To illustrate how to plot the output, consider Example 4.1.

Two-level Clippers

We have considered clippers which clip the input at one level. Let us now consider clippers which clip the signal at two independent levels. Two diode clippers may be used in a cascade to limit the output at two independent levels. If a positive-peak clipper and a negative-peak clipper are used

in a pair, the resultant circuit is called a two-level clipper. If the positive and negative peaks are clipped at the same level, the two-level clipper is called a limiter. On the other hand, if a positive-peak clipper and a positive-base clipper are connected in tandem, the circuit is called a positive slicer.

Slicers. The input can be clipped at two independent levels, either during the positive going half-cycle or during the negative going half-period. If the input is clipped at two levels during the positive going half-cycle, leaving only a slice of the input at the output, the circuit is called a positive slicer. If on the other hand, the signal is sliced during the negative half-cycle, the circuit is called a negative slicer.
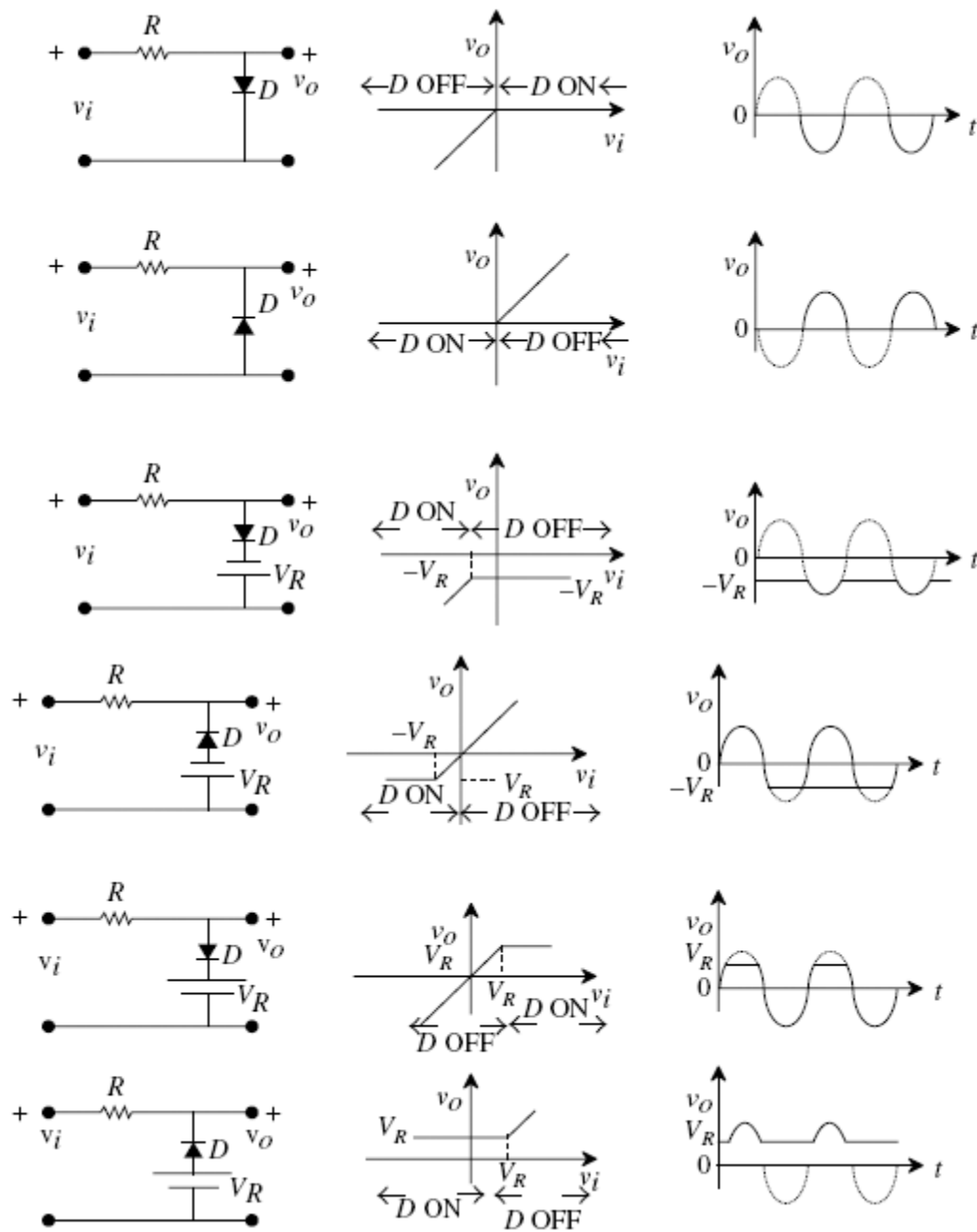
FIGURE 4.15(a) One-level shunt clippers

Positive Slicers: The circuit shown in Fig. 4.16(a) is a positive slicer, as it slices the positive going signal at two independent levels.
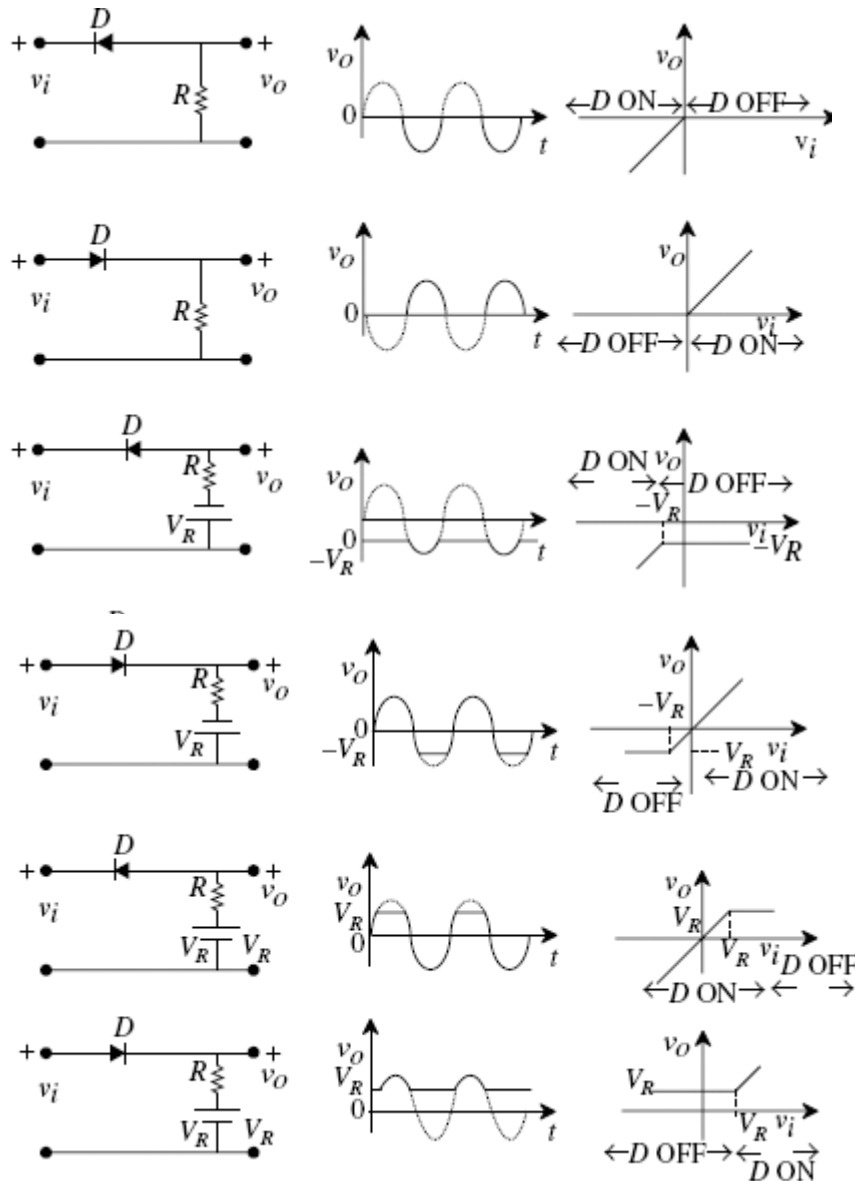
Consider the following conditions:

1.   When $v_i < V_{R1}$, D_1 is ON, D_2 is OFF. The circuit in Fig. 4.16(a) reduces to that in Fig. 4.16(b). From Fig. 4.16(b), $v_o = V_{R1}$.

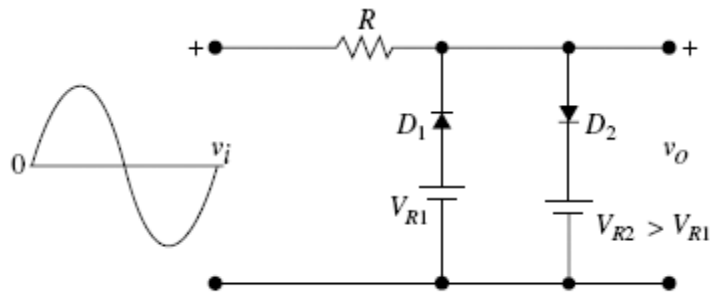2. When $V_{R1} < v_i < V_{R2}$, D_1 and D_2 are OFF. Hence, the resultant circuit is shown in Fig. 4.16(c). From Fig. 4.16(c), $v_o = v_i$.

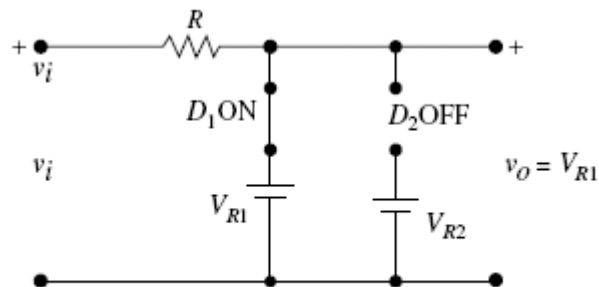3. When $v_i > V_{R2}$, D_1 is OFF and D_2 is ON. Hence, the circuit reduces to that shown in Fig. 4.16(d). Hence, $v_o = V_{R2}$. Figure 4.16(e) represents the transfer characteristic, input and output of a positive slicer. We observe that in the output only a portion of the positive going signal is selected.

FIGURE 4.15(b) One-level series clippers

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FIGURE 4.16(a) A positive slicer

FIGURE 4.16(b) The circuit of Fig. 4.16(a) when D_1 is ON and D_2 is OFF
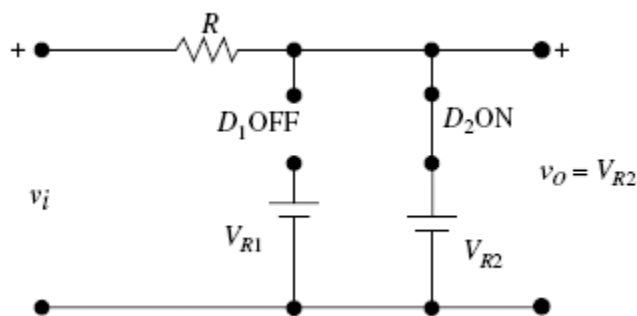
Negative Slicers: To implement a negative slicer, consider the circuit shown in Fig. 4.17(a).
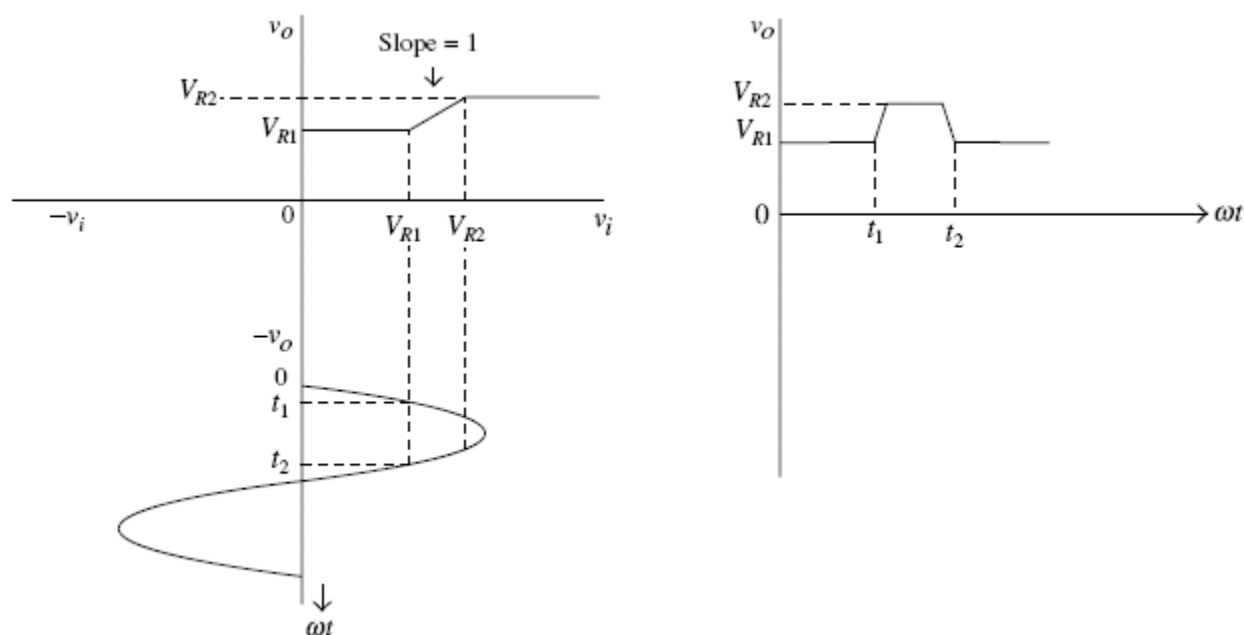
Consider the following conditions

1.   When $v_i \leq -V_{R1}$, D_1 is ON, D_2 is OFF. Hence, the circuit reduces to that shown in Fig. 4.17(b).
Therefore, $v_o = -V_{R1}$.

   2.   When $V_{R1} > v_i > -V_{R2}$, D_1 and D_2 are OFF. The resultant circuit is shown in Fig. 4.17(c). Hence, $v_o = v_i$
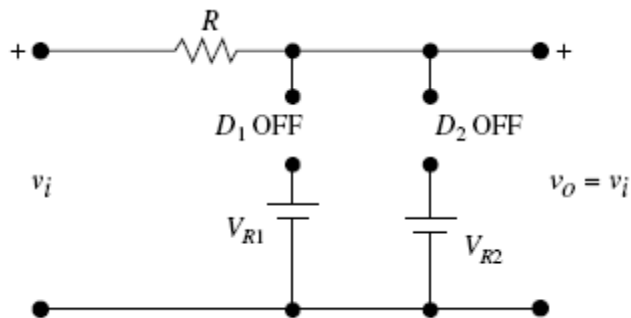
FIGURE 4.16(c) The circuit of Fig. 4.16(a) when D_1 and D_2 are OFF
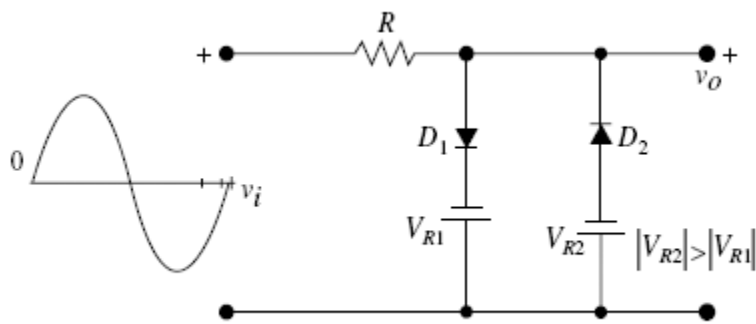
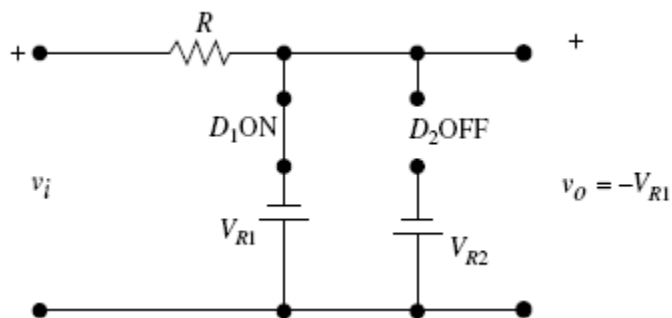**FIGURE 4.16(d)** Circuit of Fig. 4.16(a) when D_1 is OFF and D_2 is ON

FIGURE 4.16(e) The transfer characteristic of a positive slicer with input and output waveforms

3.   When $v_i \leq -V_{R2}$, D_1 is OFF and D_2 is ON, the resultant circuit is shown in Fig. 4.17(d). Hence, $v_o = -V_{R2}$. The transfer characteristic is plotted in Fig. 4.17(e). We see that in the output only a portion of the negative going signal is selected.

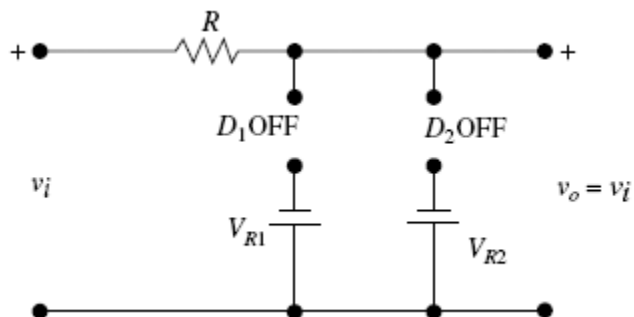**Limiters.** The combination of a positive-peak clipper and a negative-peak clipper, clipping the input symmetrically at the top and the bottom is called a limiter as shown in Fig. 4.18(a). Consider the following conditions:
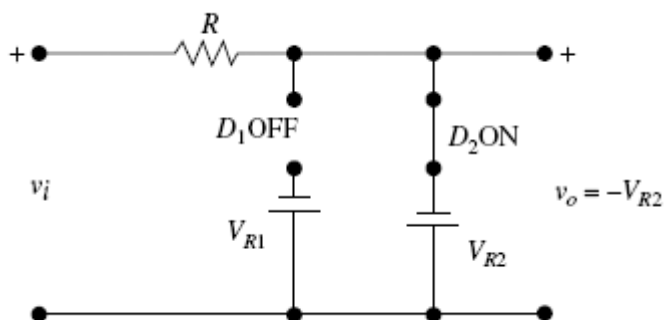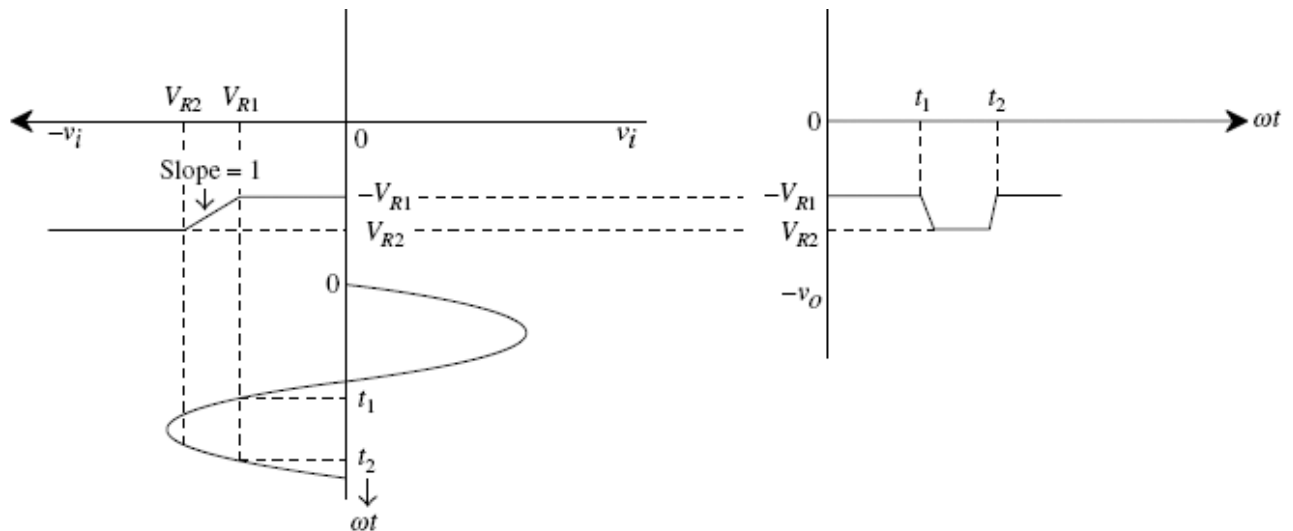
FIGURE 4.17(a) A negative slicer

FIGURE 4.17(b) The circuit of **Fig. 4.17(a)** when D_1 is ON D_2 is OFF

FIGURE 4.17(c) The circuit of **Fig. 4.16(a)** when D_1 and D_2 are OFF

FIGURE 4.17(d) The circuit of Fig. 4.17(a) when D_1 is OFF and D_2 is ON

FIGURE 4.17(e) The transfer characteristic of the negative slicer with input and output waveforms

1. When $-V_R < v_i < V_R$, D_1 and D_2 are OFF and the resultant circuit is shown in **Fig. 4.18(b)**.
    Hence, $v_o = v_i$.
    2. When $v_i \geq V_R$, D_1 is ON and D_2 is OFF. Under this condition, the resultant circuit is shown in **Fig. 4.18(c)**.
        Hence, $v_o = V_R$.
    3. When $v_i \leq -V_R$, D_1 is OFF, D_2 is ON. The circuit that is to be considered is shown in **Fig. 4.18(d)**.

Hence, $v_o = -V_R$. The transfer characteristic of the limiter is as shown in **Fig. 4.18(e)**.

FIGURE 4.18(a) A limiter

FIGURE 4.18(b) The circuit of Fig. 4.18(a) when both D_1 and D_2 are OFF
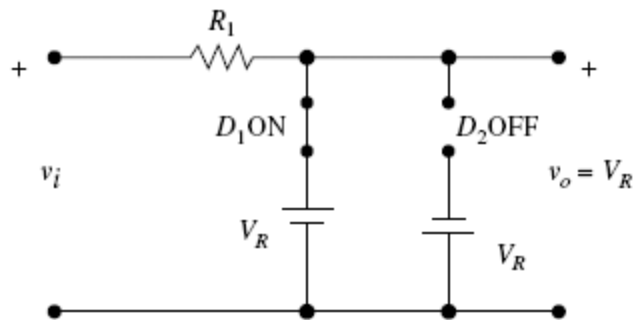
FIGURE 4.18(c) The circuit of Fig. 4.18(a) when, D_1 is ON and D_2 is OFF
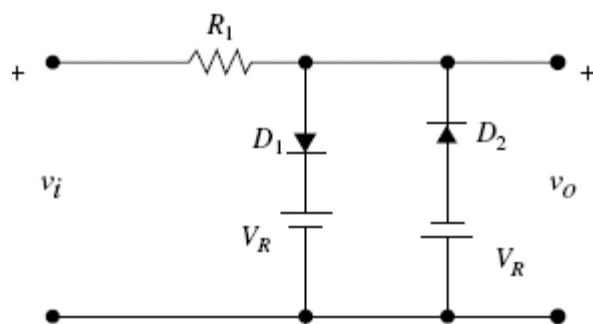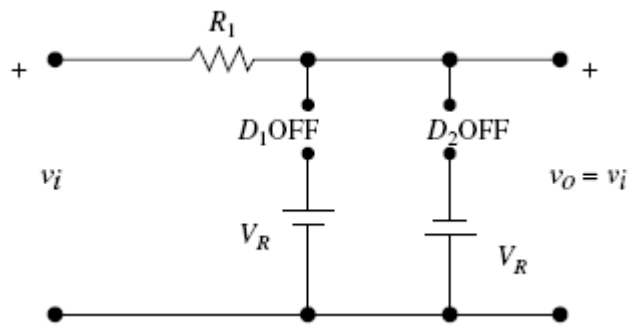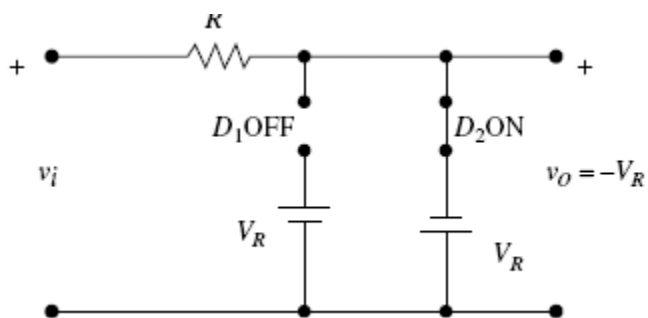

FIGURE 4.18(d) The circuit of Fig. 4.18(a) when D_1 is OFF, D_2 is ON
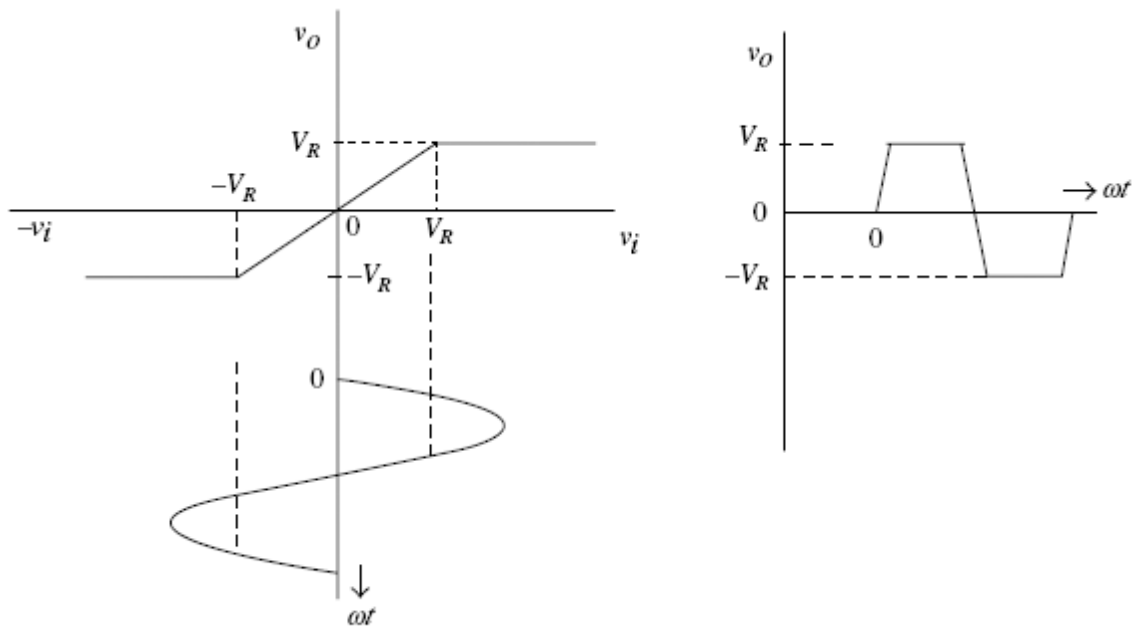
FIGURE 4.18(e) The transfer characteristic of a limiter with input and output waveforms
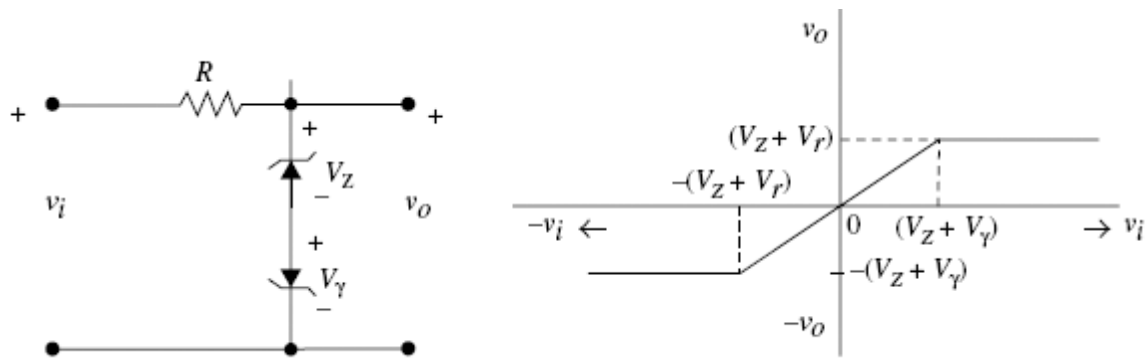
FIGURE 4.19(a) A limiter using Zener diodes and (b) the transfer characteristic

The limiter circuit can also be implemented using Zener diodes as shown in Fig. 4.19(a).

When $-(V_z + V_\gamma) < v_i < (V_z + V_\gamma)$, $\quad v_o = v_i$

When $v_i \geq (V_z + V_\gamma)$, $\quad v_o = (V_z + V_\gamma)$

When $v_i \leq -(V_z + V_\gamma)$, $\quad v_o = -(V_z + V_\gamma)$

The transfer characteristic is drawn in Fig. 4.19(b). Limiters are used in frequency-modulated systems where only the frequency of the carrier is varied, but its amplitude remains constant.

Two-level Emitter-coupled Transistor Clipper. The circuit shown in **Fig.** 4.20(a) is a two-level emitter-coupled transistor clipper. Let the input v_i to Q_1 be small enough ($< v_{i1}$) to keep Q_1 OFF. As a result, $I_{C_1} \approx I_{E_1} = 0$. If V_{BB} is adjusted such that Q_2 is in the active region, then the voltage $v_o = V_{CC} - I_{C_2}R_C$. When v_i is increased further so that Q_1 conducts, there is I_{E_1}through R_e, the drop across R_e increases which in turn reduces I_{B_2} of Q_2 resulting in reduction of I_{C_2}. Consequently, v_o increases. When v_i is increased further, v_o also rises. Thus, the output is proportional to the input in a limited region. A further increase in v_i to v_{i2} enables Q_1 to draw reasonably large I_{E_1} and the drop across R_e can now reverse-bias the base–emitter diode of Q_2, thereby driving Q_2 into the OFF state. As a result, v_o is limited to V_{CC}. The transfer characteristic with input and output waveforms is shown in **Fig.** 4.20(b). Thus, this circuit behaves as a two-level clipper (slicer). The region of linearity can be controlled by the choice of V_{BB}.
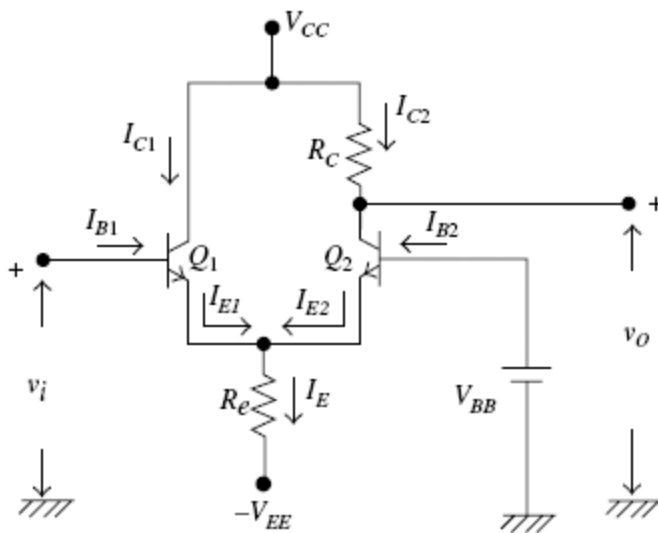
FIGURE 4.20(a) A two-level transistor clipper

Noise Clippers

If an input signal has an associated noise component, it will cause the signal amplitude to fluctuate. This noise component may sometimes trigger sensitive circuits. Now, consider **Figs.** 4.21(a) and (b) which represent two input signals with associated noise components.

Series and Shunt Noise Clippers. An input signal with noise components seen in **Fig.** 4.21(a), can be eliminated by a series noise clipper shown in **Fig.** 4.21(c). As long as the noise magnitudes are small ($< |V_\gamma|$), the diodes are OFF. Hence, the output is zero during the period noise is present. The output is devoid of noise. Now let the input signal have an associated noise as

represented in Fig. 4.21(b). This noise can be eliminated by a shunt noise clipper, as shown in Fig. 4.22(a).
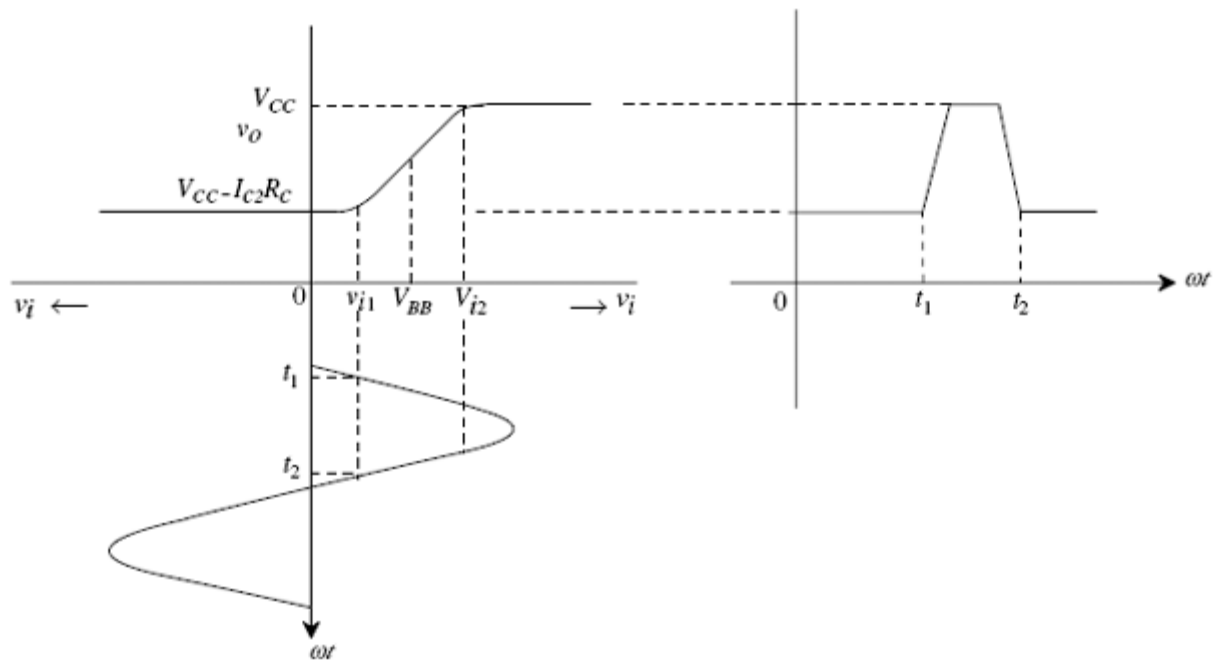
FIGURE 4.20(b) The transfer characteristic of a two-level transistor clipper with input and output waveforms
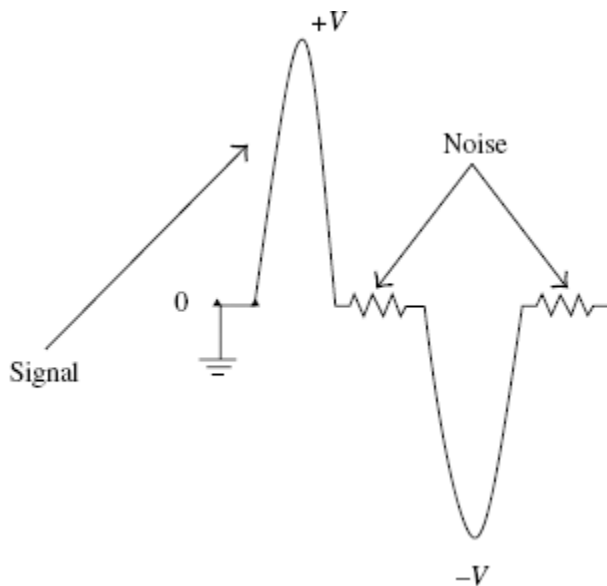
FIGURE 4.21(a) An input signal with an associated noise
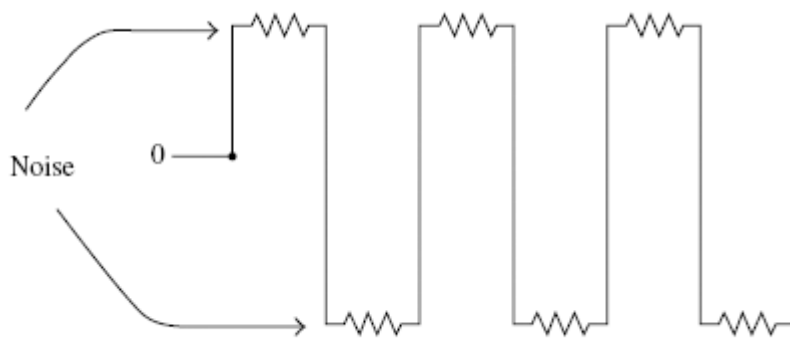
FIGURE 4.21(b) An input signal with an associated noise

Here, the magnitude of the output is limited to V_F, the forward voltage of the diode and noise is eliminated in the output. If only the noise is to be eliminated, the diodes can be biased by an appropriate voltage, V [see **Fig. 4.22 (b)**].
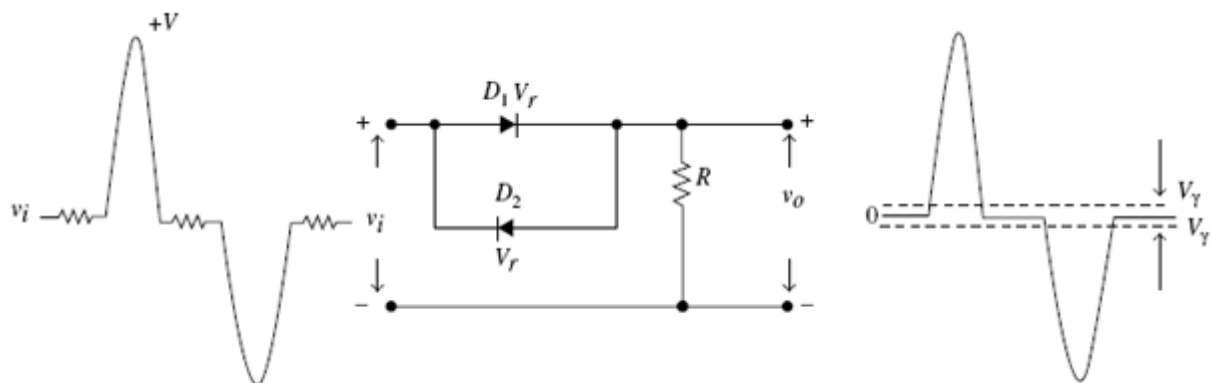
FIGURE 4.21(c) A series noise clipper
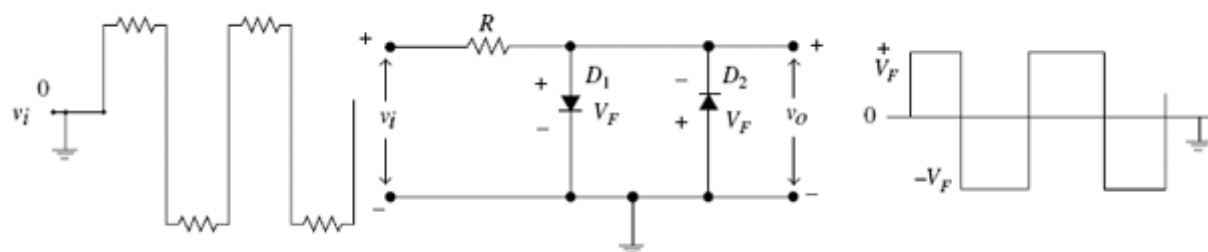
FIGURE 4.22(a) A shunt noise clipper
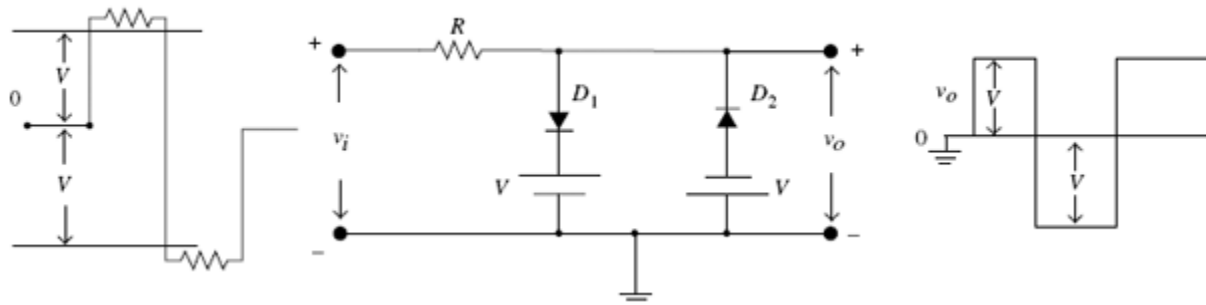
FIGURE 4.22(b) A biased noise clipper

Compensation for Changes with Temperature. We know that V_γ reduces by approximately 2.5 mV/°C rise in temperature. Consequently, the output of the clipping circuit can change. Compensation techniques may be employed in precision clipping circuits to take care of variation in V_γ by temperature changes. Let us consider the series clipping circuit inFig. 4.23(a).

If the diode is ideal, this is simply a switch. But an idealized diode is represented by an ideal diode in series with V_γ; hence the above circuit is redrawn as shown in **Fig. 4.23(b)**. If V_γ now changes, the output will also change accordingly. To make sure that the output does not vary with temperature, the circuit shown in **Fig. 4.23(c)** may be employed.

The two diodes D_1 and D_2 are identical, which means that the variation of V_γ with temperature, is identical in both the diodes; hence, changes in temperature will not alter the output. However, D_2 should be always ON. For this, V_1 and R_1 are provided to forward-biasD_2. The need for a separate source V_1 may be eliminated as shown in **Fig. 4.23(d)**. Here D_2 is kept ON by V_R and R_1. **Figure 4.23(e)** presents a modification of this circuit.

COMPARATORS

An amplitude comparator is a circuit that tells the time instant at which the input amplitude has reached a reference level. A comparator is shown in <u>Fig. 4.24</u>.

Ideally, in this comparator:

$v_o = 0$ for $t < t_1$

$v_o = V$ for $t \geq t_1$

The amplitude of the output abruptly rises from 0 to V at $t = t_1$, t_1 is the time instant at which v_i reaches V_R.

Diode Comparators

In this section, we discuss two types of diode comparators—pick-off and break-away diode comparators.

Pick-off Diode Comparators. A simple diode comparator circuit is shown in Fig. 4.25. A base clipper is used as a comparator. The input now is a ramp and V_R is the reference voltage. The circuit is required to tell the time instant at which the input reaches V_R.
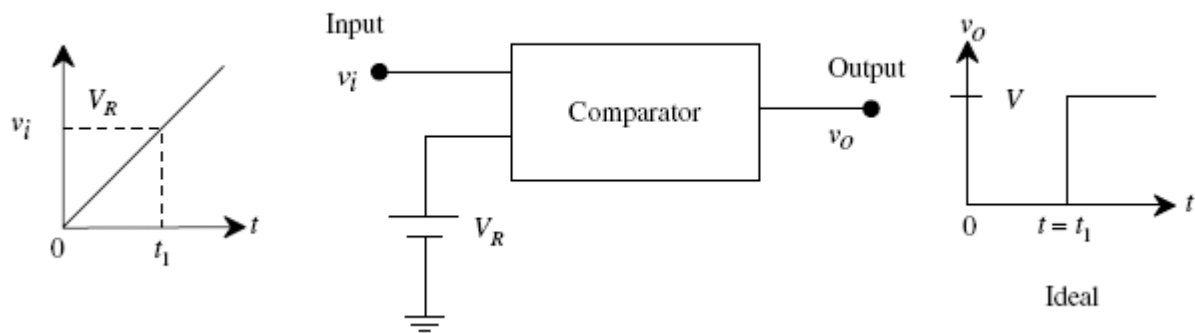
FIGURE 4.24 A comparator
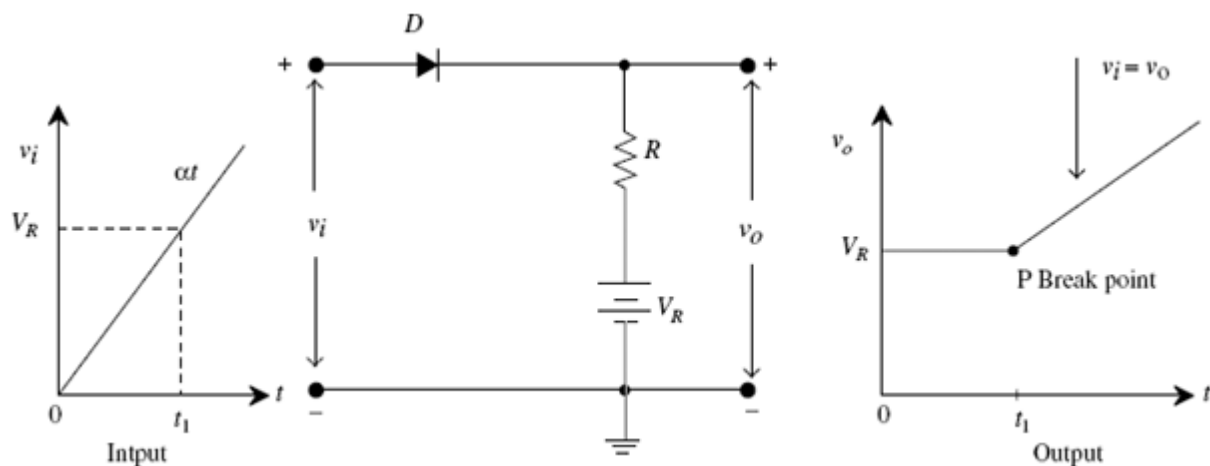
FIGURE 4.25 A pick-off diode comparator

Using an ideal diode, as long as, $v_i < V_R$, $v_o = V_R$. If $v_i \geq V_R$, $v_o = v_i$. Upto $t = t_1$, $v_o = V_R$ and the slope of the output is 0. At $t = t_1$, output suddenly rises as the input (the slope at the output has

changed) and this is the time instant at which the input reaches the reference level V_R. The point P where the slope changes when the diode conducts is called the break point. The diode in this case is called a "pick-off" diode.

As is evident from the Fig. 4.25, there is a sudden change in the slope of the output at the instant the input reaches V_R. However, due to ageing and temperature variations, the diode may not switch from OFF to ON at exactly $t = t_1$ (break point, P). It may switch state at any instant after t_1 and before t_2 (see Fig. 4.26).
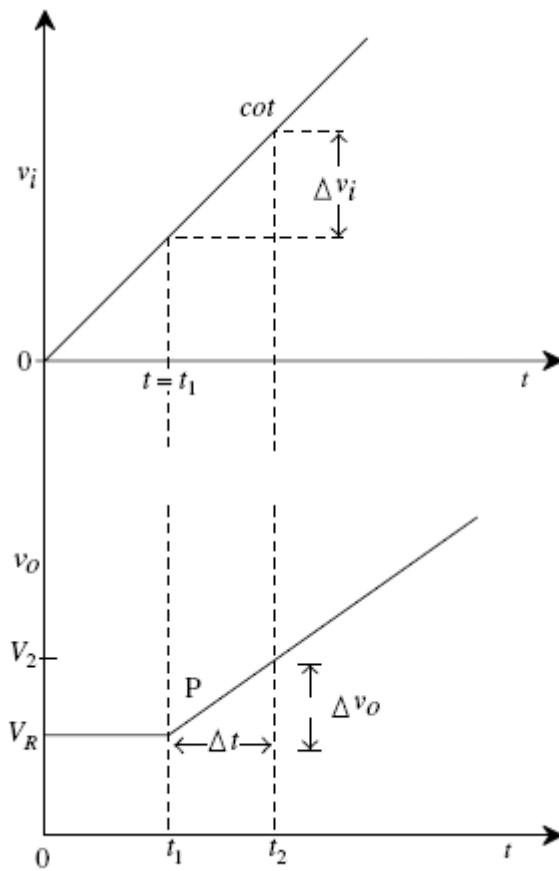
FIGURE 4.26 The input and output of the diode comparator

Hence, the break point (the point at which the device D changes state) may not exactly be at t_1. Instead, there is a break region (t_1 to t_2), within which, at any instant the device may switch state. Therefore, there is a large region of uncertainty. After the break point, the output follows the input—it has the same slope as the input. If this region of uncertainty is to be reduced to know precisely at which time instant the input reaches the reference level, the break region should be sharp. To achieve this, an amplifier may be placed before or after the comparator.

Consider the response of the comparator circuit shown in Fig. 4.25. To the left of the break point, the diode is OFF. Hence, the reverse incremental resistance of the diode is significantly larger when compared to R. To the right of the break point, the forward incremental resistance of the diode is much smaller than R. If the break point is located at a point where the incremental resistance of the diode, (r) is equal to the resistance (R) then the incremental change in the output voltage (Δv_o) for a corresponding change at the input (Δv_i) is calculated using Fig. 4.27.

$$\Delta v_o = \Delta v_i \frac{R}{r + R}$$

If $r = R$:

$$\frac{\Delta vo}{\Delta v_i} = \frac{R}{R + R} = \frac{1}{2}$$
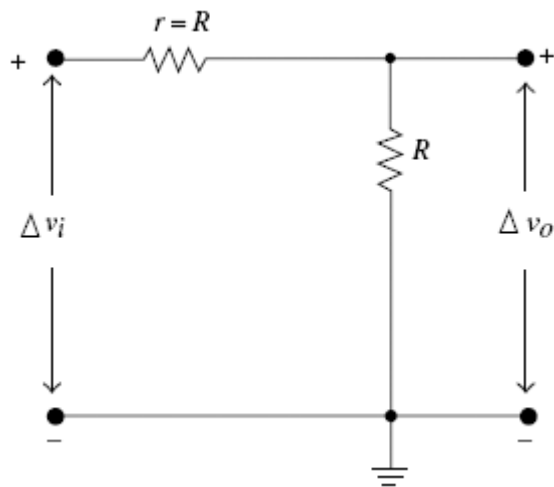
FIGURE 4.27 The circuit to calculate the incremental change in the output voltage

This relation tells that $\Delta v_i = 2\Delta v_o$. That is, for a larger incremental change in the input, there is a smaller incremental change in the output. The region of uncertainty is larger.

A device is connected at the output of the comparator, and is required to be activated when the diode current is say, I and has a drop across R as IR. If, now an amplifier is connected at the output of the comparator to reduce the region of uncertainty, the output of this amplifier activates

the device (see Fig. 4.28). Let the amplifier have a gain A. During $\Delta t = t_2 - t_1$, the output changes by $\Delta v_o = V_2 - V_R$, see Fig 4.26, the delay in the response is reduced to $\Delta t/A$ or $(t_2 - t_1)/A$.

Let the amplifier only amplify the change in the comparator input but not the reference voltage. The device to be activated is activated only when the drop across R is IR. However, now $I = I/A$. Hence, the device is activated when the drop across R is RI/A since the diode current is amplified by A and the dynamic diode resistance, $r = (\eta \, V_T/I)$, varies inversely with current. Therefore, it is evident that, the device to be activated by the comparator will respond at a current corresponding to $r = RA$.

$$\frac{\Delta v_o}{\Delta v_i} = A\frac{R}{r+R} = \frac{AR}{R+RA} = \frac{A}{1+A}$$

As $A \rightarrow \infty$, $\dfrac{\Delta v_o}{\Delta v_i} \rightarrow 1$

Without an amplifier, $\Delta v_o/\Delta v_i$ (the transmission gain) was half and with an amplifier connected as in Fig. 4.29, $\Delta v_o/\Delta v_i$ is one; i.e., there is no marked improvement in the response of the comparator arrangement of Fig. 4.28.

Now, consider a comparator circuit where the amplifier precedes a comparator and the output of the comparator is directly connected to the device to be actuated. Let the amplifier have a gain A and Δv_i be the incremental change in the input needed to actuate the device when the output is directly connected to the device. With a pre-amplifier with gain A connected to the comparator, $\Delta v_i/A$ is now the incremental change in the input needed to make the output change as in the previous case. As $\Delta v_i/A$ is small, the break region is reduced. Thus, this is a better comparator.
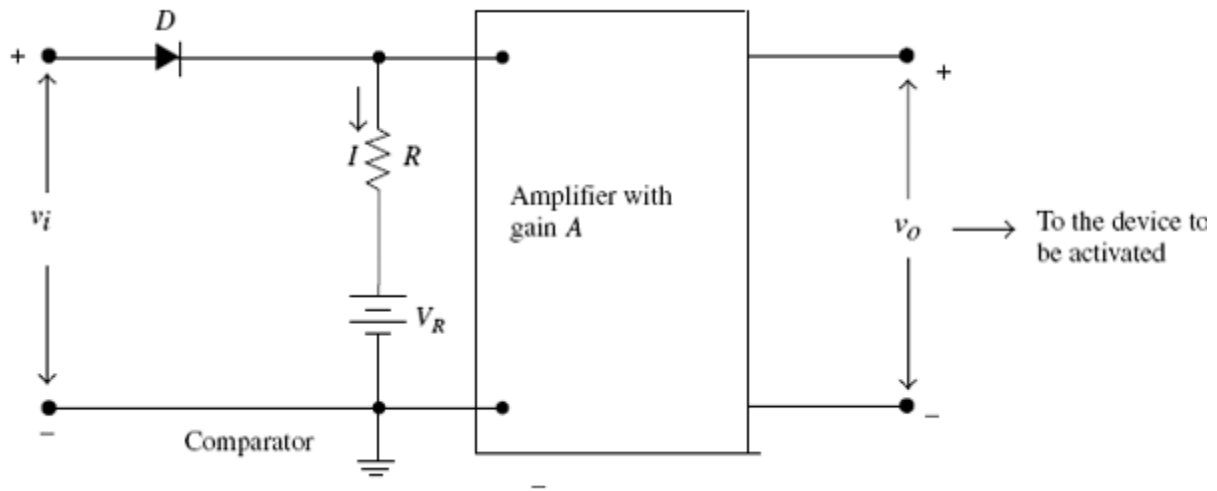
FIGURE 4.28 The output of the comparator connected to an amplifier
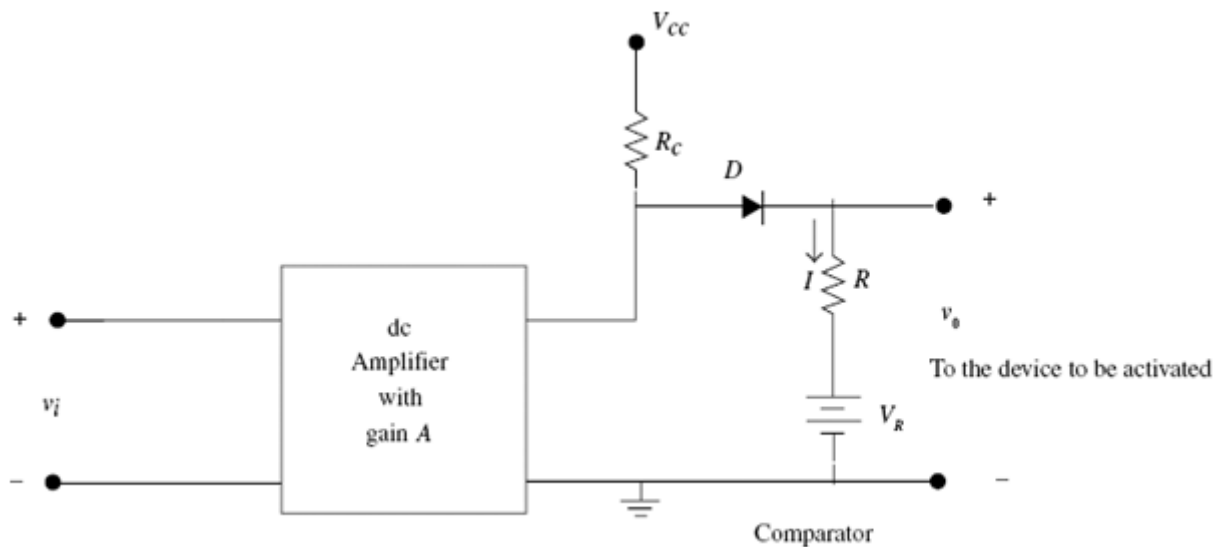
FIGURE 4.29 The output of the amplifier drives a comparator

Break-away Diode Comparators. Consider the circuit in Fig. 4.30. If the input to the circuit is a negative ramp, then the output is as shown. The diode in this case is called a "break-away" diode. Here:

As long as $v_i > V_R$, D is ON and $v_o = V_R$. When $v_i \leq V_R$, D is OFF and $v_o = v_i$.

The Double Differentiator as a Comparator

In any comparator, if the output activates a device, the comparator output should reach the device to be activated just at the moment of comparison. Once the device has been activated by the output of the comparator, it is also desirable that the signal is not present. A double differentiator [see Figs. 4.32(a) and (b)] does these twin jobs.

Let the input to the comparator be a ramp. The output of the diode comparator is a step voltage V_R up to t' and is a ramp beyond this time instant. As long as the input to the first differentiator is a step, its output is zero in no time because C_1 blocks dc. At t', the input to the high-pass circuit is ramp; hence, its output is an exponential. This signal is then connected to an amplifier with gain A and the resultant output, which is an exponential, is applied as an input to another high-pass circuit. The output of this is now a pulse whose amplitude and duration can be controlled.
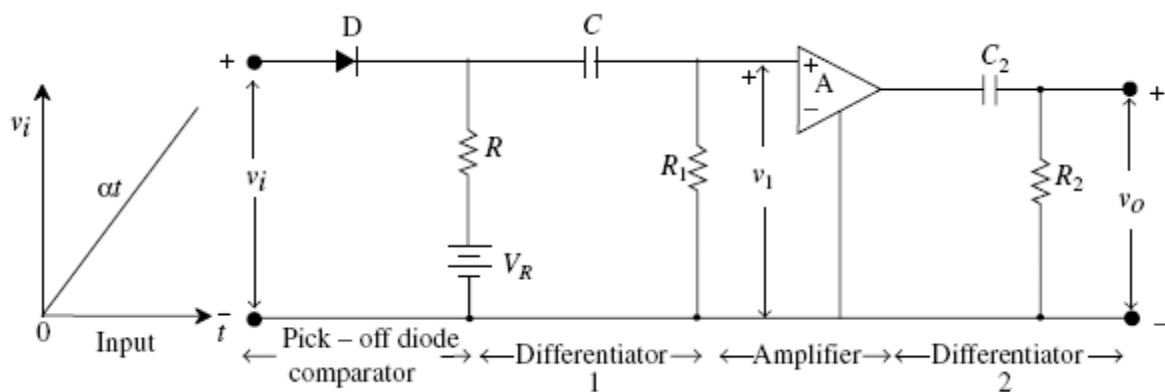
FIGURE 4.32(a) A double differentiator as a comparator

In a double differentiator comparator, the device to be activated receives the signal only when the input reaches a reference level. Soon after, as the amplitude of the pulse dies down, no signal reaches the device to be activated. This could be called a practical comparator.
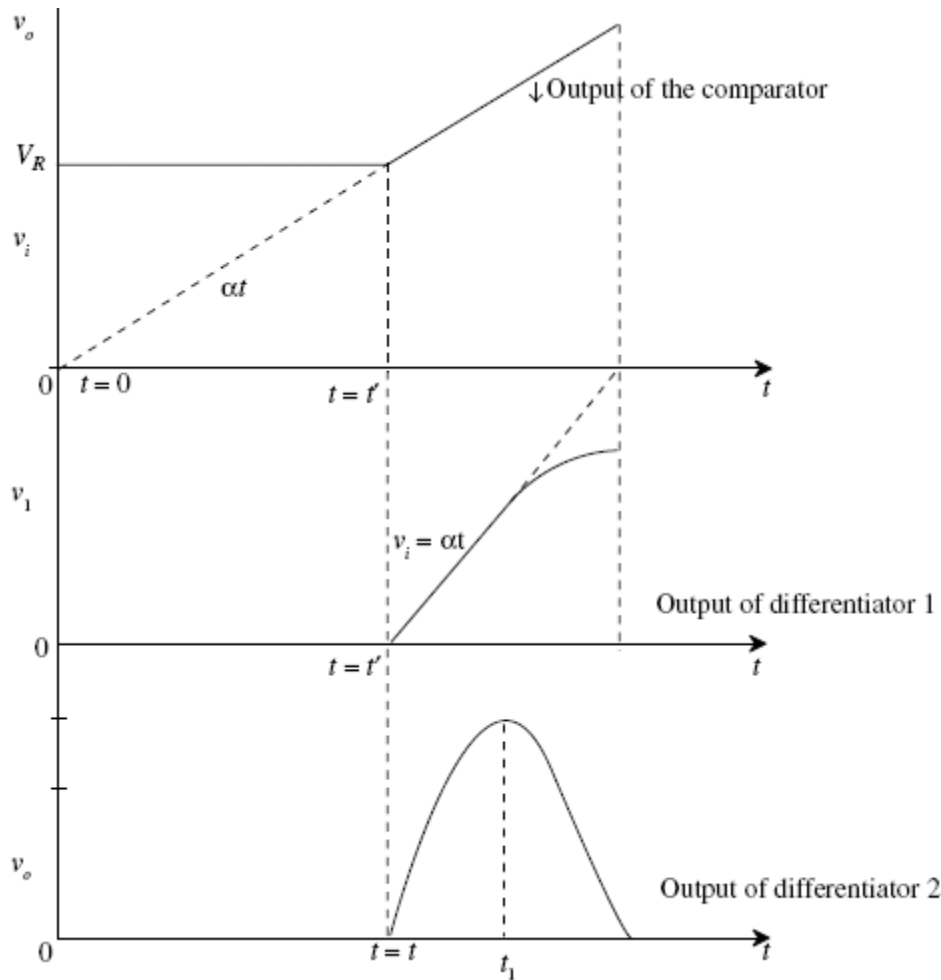
FIGURE 4.32(b) The waveforms of a double differentiator

APPLICATIONS OF COMPARATORS

Apart from being used as amplitude comparators, comparator circuits can be used for many applications. A few applications are presented in this section.

1. Measurement of time delays: In the comparator shown before, if V_{R1} is the reference level in the first comparator (double differentiator), then a pulse is generated with a peak at $t= t_1$. If V_{R2} is the reference level set in a second comparator then the pulse is generated with peak at $t = t_2$. Then the time difference between the two pulses is $(t_2 − t_1) = (V_{R2} − V_{R1})/\alpha$ where, α is the slope of the input ramp.

2. Timing markers generated from a sine wave: If a sine wave is applied as input, when the input reaches V_R, the output of the comparator is high till the input reaches V_R again. After

differentiating and clipping negative spikes, we get positive spikes which can be implemented as timing markers, as shown in Fig. 4.33.

3. Phase meter: Let two sinusoidal inputs having a phase difference be applied to a comparator whose reference voltage is zero, as shown in Fig. 4.34. Here, the output pulses are differentiated and the time difference between the output spikes is proportional to the phase difference.
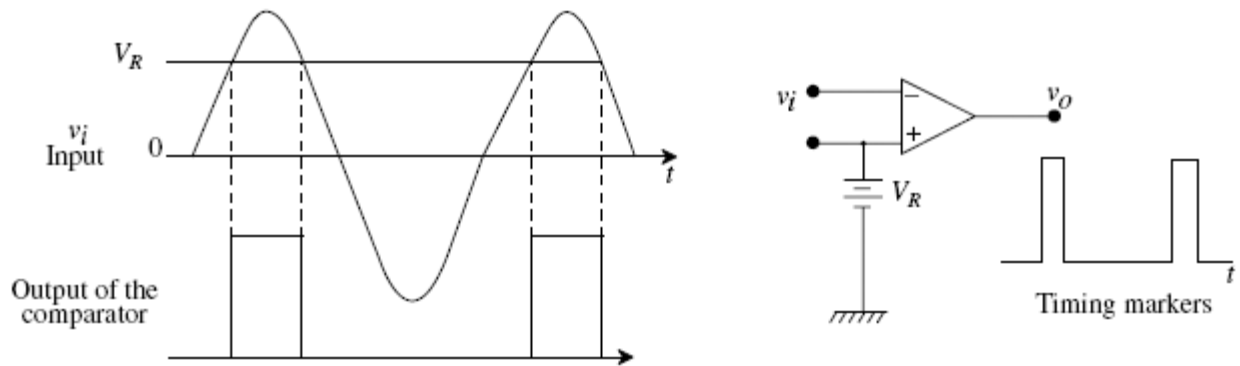
FIGURE 4.33 Comparator used to generate timing markers
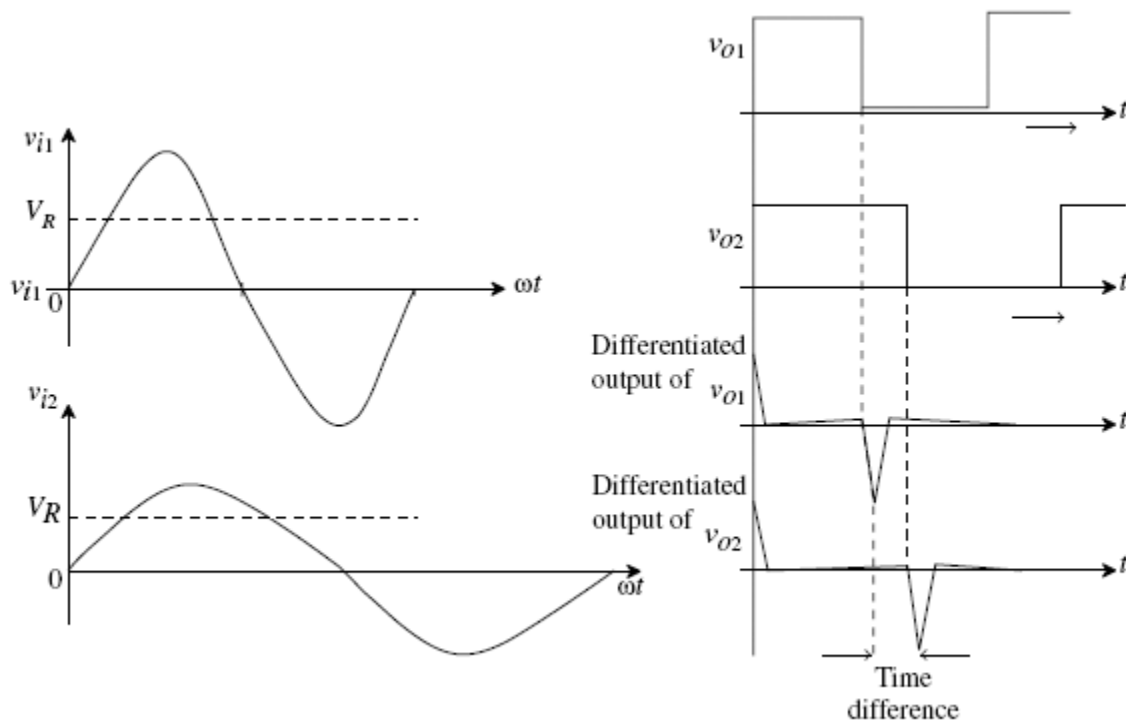
FIGURE 4.34 The Waveforms of a comparator used for the measurement of phase difference

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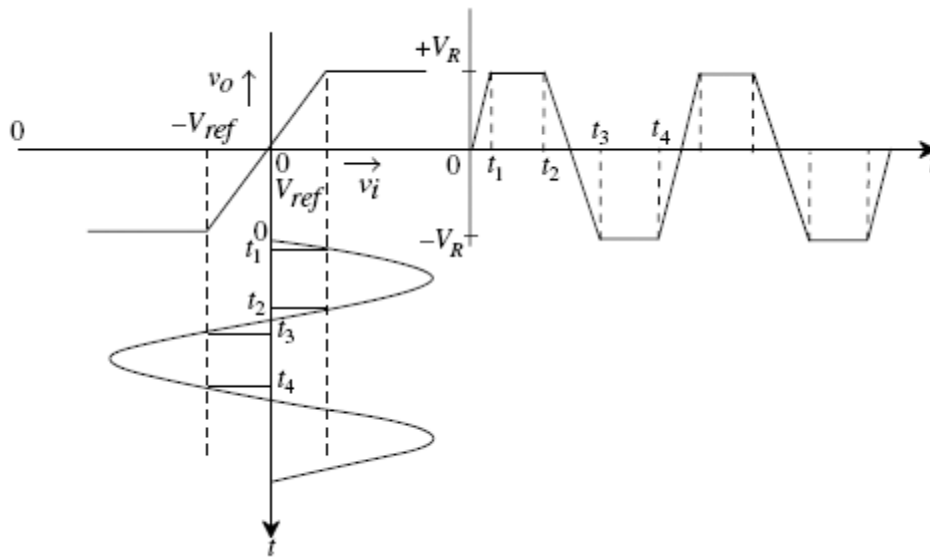
FIGURE 4.35 The comparator used to convert a sinusoidal input into a square-wave output

4. Square waves from sine waves: In a regenerative comparator (Schmitt trigger), as long as v_i is less than V_{ref}, v_o is the same as v_i, as shown in **Fig. 4.35**. If the input goes beyond $\pm V_{ref}$, the output of the comparator remains at either $+V$ or $-V$, thereby converting a sinusoidal input into a square-wave output, when the frequency is sufficiently large.

Non-linear Waveshaping: Clamping Circuits

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Describe various clamping circuits
- Derive the necessary relations to plot steady-state output
- Describe the effect of diode characteristics on the clamping voltage
- Describe synchronized clamping
- State and derive the clamping circuit theorem

INTRODUCTION

When a signal is transmitted through a capacitive coupled network, the dc component associated with the input is lost in the output since the capacitor blocks the dc. If the dc component needs to

be restored, a clamping circuit is used. Thus, clamping circuits reintroduce the dc component lost during transmission through a capacitive coupled network and hence, are called either dc restorers or dc re-inserters. The output reaches the steady-state value in a few cycles after the application of the input to the clamping circuit (transient period). Circuits that clamp the positive peak of the signal to the zero level are called negative clampers and those that clamp the negative peak of the signal to the zero level are called positive clampers. In general, the output can be referenced to any arbitrarily chosen reference voltage. Circuits that clamp the output to zero or to any dc level are considered here. The necessary relations that enable us to plot the steady-state responses are then derived. The effect of the internal resistance of the source on the output and the influence of diode characteristics on the clamping voltage are also examined. In some applications, clamping is needed only for a finite duration and the time interval for which this is to be accomplished is determined by an external signal called the control signal. The circuit that performs this operation, called synchronized clamping circuit, is also discussed.

THE CLAMPING CIRCUIT

The clamping circuit essentially consists of an input source, a capacitor of a suitable value and a diode connected in shunt with the output terminals. This clamps the positive peak of the input signal (sinusoidal, in this case) to the zero level. The diode is assumed to be ideal and initially there is no charge on the condenser. v_A is the charge built up on the condenser, C. Figure 5.1 shows a basic clamping circuit.
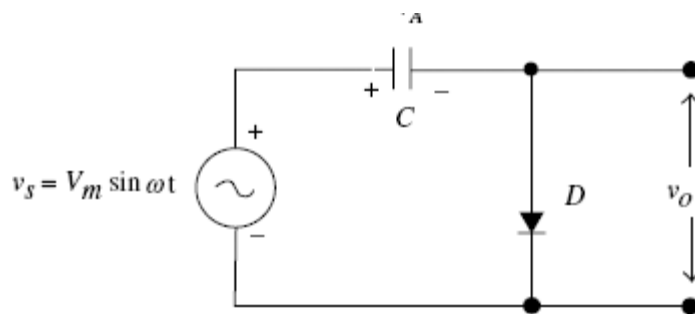
FIGURE 5.1 A negative clamping circuit

As the input rises from 0 to V_m in the first quarter cycle, D conducts [see Figs 5.2(a) and 5.3(a)], C charges to V_m. During this period, $v_o = 0$ if the diode is ideal. The input falls after the first quarter cycle. $v_s < V_m$, where V_m is the charge on the condenser. As a result, the diode is reverse-biased by a voltage ($v_s - V_m$). Hence, D is OFF, as shown in Fig. 5.2(b). Thus:
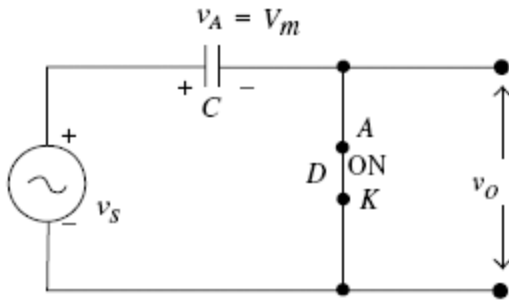
FIGURE 5.2(a) The clamping circuit when the diode is ON
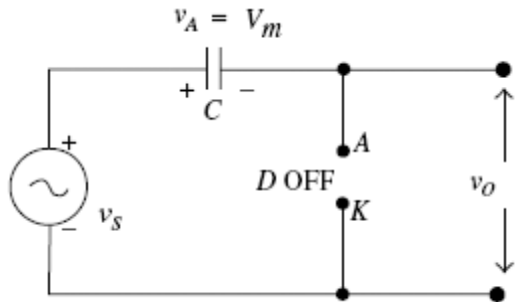
FIGURE 5.2(b) The clamping circuit when the diode is OFF

The voltage across C remains unchanged. From Eq. (5.1) at $v_s = 0$, $v_o = -V_m$. And if, $v_s = -V_m$, $v_o = -V_m - V_m = -2\,V_m$ and at $v_s = V_m$, $v_o = V_m - V_m = 0$

During the next cycle, the positive peak of the output just reaches the zero level. Hence, in the output, the positive peak is clamped to the zero level. To clamp the positive peak to zero, a negative dc voltage is introduced in this circuit. Therefore, this circuit is called a negative clamp.

Alternatively, if a positive dc voltage is inserted by the clamping circuit so that the negative peak of the input signal is clamped to the zero level, the circuit is called a positive clamp [seeFig. 5.3(b)]. The input to this circuit in Fig. 5.3(b) is a sinusoidal waveform with zero reference level. The output is referenced to $+V_m$ and the negative peak is clamped to zero. The input and output waveforms of negative and positive clamp circuits are represented inFigs. 5.3(a) and 5.3(b), respectively.
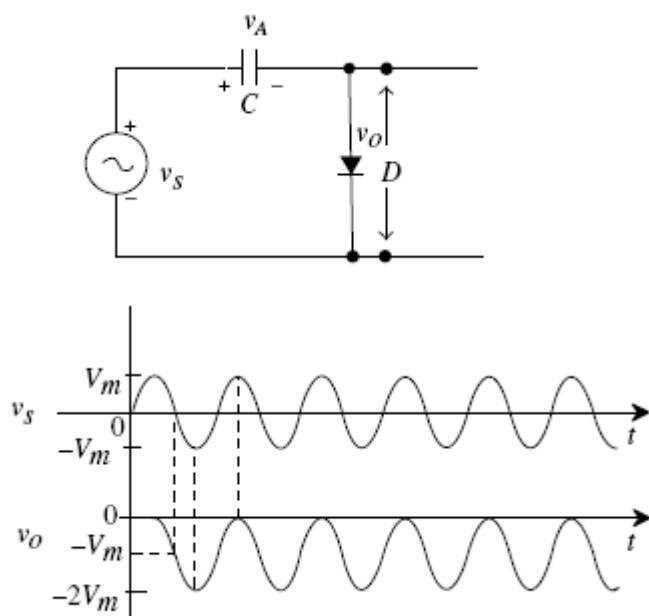
FIGURE 5.3(a) The circuit, input and output waveforms of a negative clamp
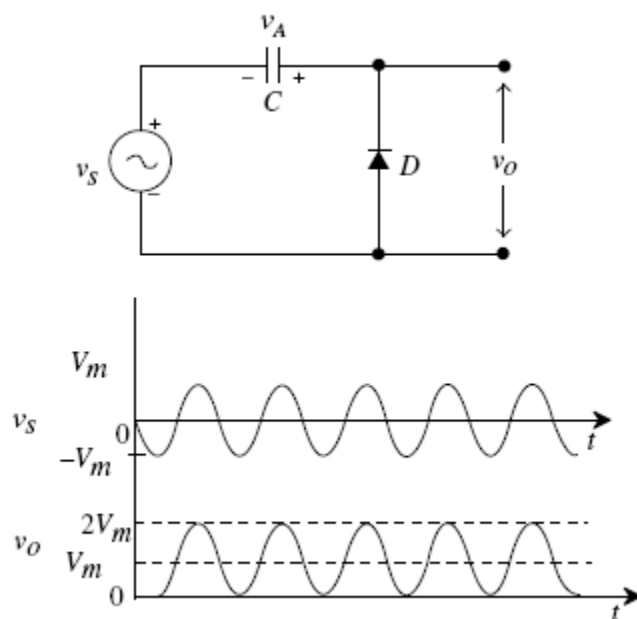
FIGURE 5.3(b) The circuit, input and output waveforms of a positive clamp

The Clamping Circuit for Varying Input Amplitude

In our description of the clamping circuit in the previous section, a steady input signal was assumed; which is always not the case. The amplitude of the input signal may either increase or decrease for various reasons. So, what is the effect of this variation on the output? To answer this

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question, let us analyse the behaviour of the circuit under the two possible conditions—increase in amplitude and decrease in amplitude.

If the amplitude of the input increases at $t = t_1$ [see Fig. 5.4(a)], once again the diode D conducts for a quarter cycle. The output is zero for this period. Subsequently, the positive peak of the output remains clamped to zero, as shown in Fig. 5.4(b). Obviously, this simple clamping circuit can clamp the output to zero, even if the input increases. However, the output is distorted for a quarter of a cycle.
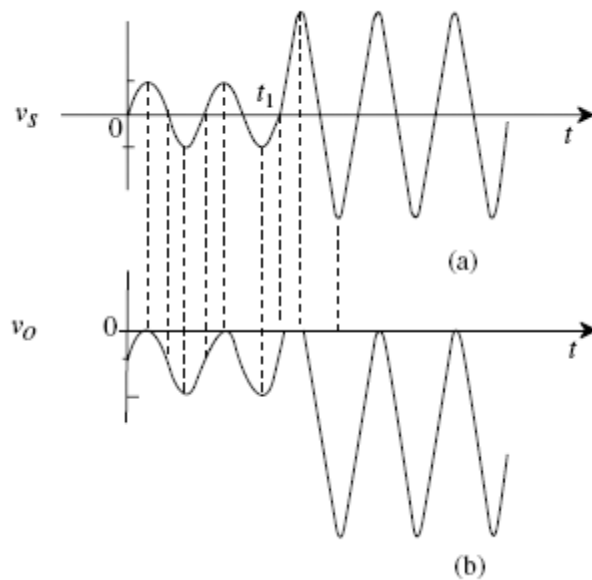
FIGURE 5.4(a) The amplitude of the input increases at t_1; (b) the output is once again clamped to zero in a quarter cycle

However, this clamping circuit cannot handle an input signal with decreasing amplitude. When the amplitude of the input signal decreases, the voltage across the capacitor should change to the peak amplitude of the new input so as to clamp the positive peak to the zero level. In this circuit, there is no path for the charge on the capacitor to discharge. To facilitate the discharge of the condenser, a resistance R is introduced in shunt with the diode D, as shown in Fig. 5.5(a).

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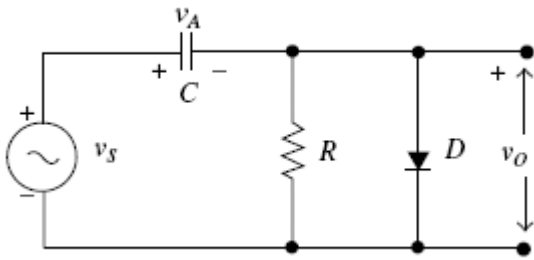
FIGURE 5.5(a) The clamping circuit with a resistance shunted across the diode

It is seen from <u>Figs. 5.5(b)(i) and (b)(ii)</u>, at $t = t_1$, if the input amplitude is abruptly reduced, as the voltage across the capacitor cannot change instantaneously, the positive peaks will not reach the zero level. However, as the capacitor discharges, the voltage across the capacitor varies exponentially with a time constant, $\tau = RC$. The output reaches the zero level at $t = t_2$, and the positive peak is again clamped to zero after a few cycles [see <u>Fig. 5.5(b)</u>(iii)]. Let us examine the situation in detail, when the positive peak is clamped to zero as shown in <u>Fig. 5.6</u>.

In the proximity of a positive peak, D conducts and at $t = \quad$, $v_o = 0$. In the absence of the diode, the output should have followed the dashed line with the peak at $t = t_2$. However, because of the diode, the output is zero from $\quad$ to t_2; and in the subsequent cycles the positive peaks of the sinusoidal waveform are clamped to zero. Although, for a small duration between $\quad$ and t_2, the output is different from the variation of a sinusoidal signal, i.e., there is a distortion. If the distortion is to be minimized, the capacitor must not lose an appreciable charge in one cycle. For this, the time constant has to be very large as compared to the time period of the input signal.

The Practical Clamping Circuit

In our discussion so far, we have assumed an ideal voltage source with $R_S = 0$. However, a practical voltage source has a finite R_S and the influence of R_S on the output will have to be taken into account. In this section, we examine the influence of the internal resistance of the voltage source on the output of the clamping circuit. If the internal resistance of the source R_S is introduced into the clamping circuit, the modified circuit is as depicted in <u>Fig. 5.7</u>.

(i) Input falls abruptly

(ii) Positive peak not clamped to zero

$t = t_1$

$t = t_2$

(iii) Exponential decay of voltage across C
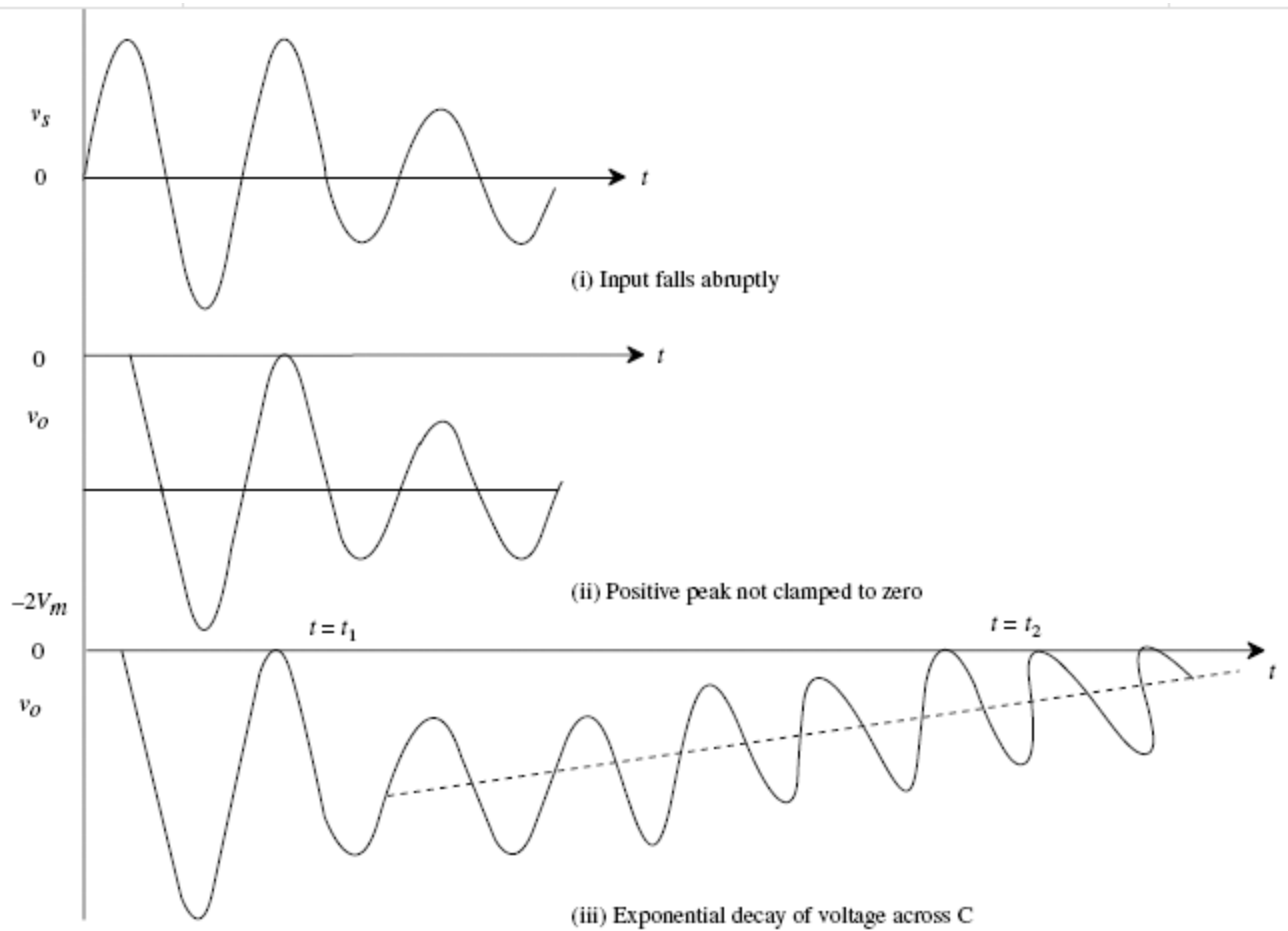
FIGURE 5.5(b) (i) The input when the amplitude decreases at $t = t_1$; (ii) the output when $R = \infty$; and (iii) the output with finite R

When the input is applied to this modified circuit, the output reaches the steady-state value after a few cycles and the positive peaks are clamped to zero. To understand how the output reaches the steady-state, let us examine the equivalent circuits for both the ON and the OFF states of the diode.

When the diode is ON, the circuit is as represented in Fig. 5.8(a). As $R_f << R$, this circuit reduces to that shown Fig. 5.8(b). For the purpose of computing the output, the circuit in Fig. 5.8(b) may be redrawn as shown in Fig. 5.8(c).

Figure 5.9 (a) depicts the circuit when the diode is OFF. As the reverse resistance $R_r >> R$, the effective resistance is R and this circuit reduces as shown in Fig. 5.9(b). Again, for computing the output, the circuit in Fig. 5.9(b) is redrawn as in Fig. 5.9(c).

v_o in the vicinity of a positive peak
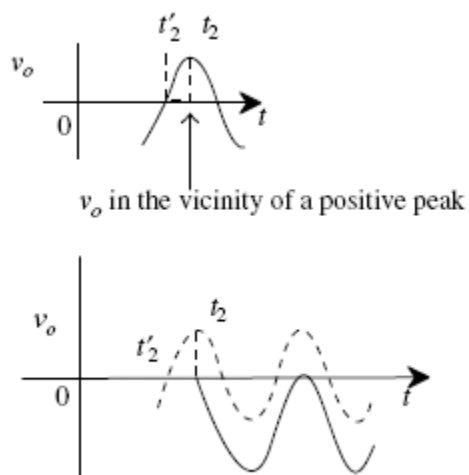
FIGURE 5.6 Output with expanded time scale in the vicinity of a positive peak
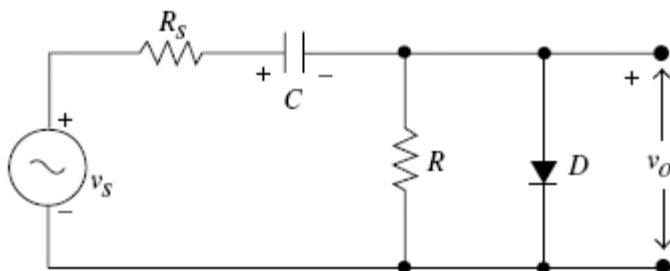
FIGURE 5.7 A clamping circuit where R_S has been taken into account

$R_f =$ Forward resistance of the diode
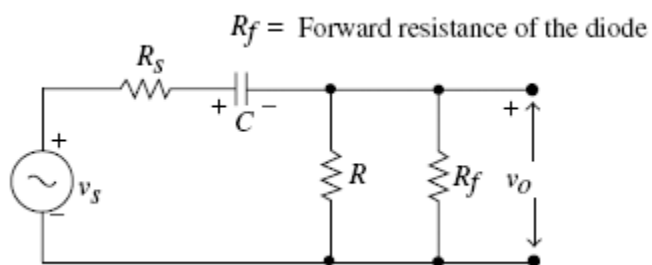
FIGURE 5.8(a) The circuit when the diode is ON
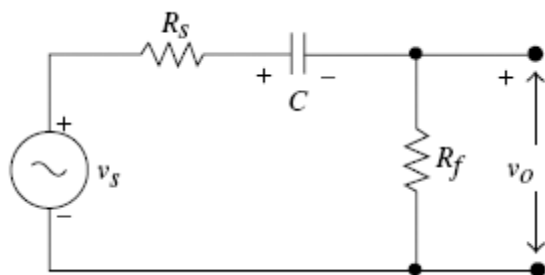
FIGURE 5.8(b) The circuit when D is ON and $R_f << R$
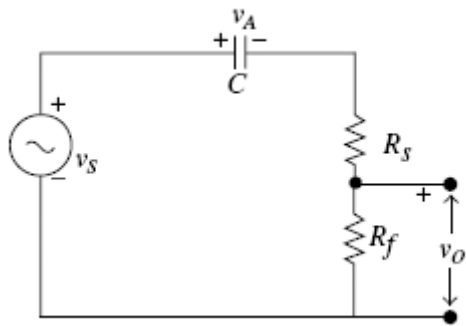
FIGURE 5.8(c) The circuit to calculate the output when the diode is ON
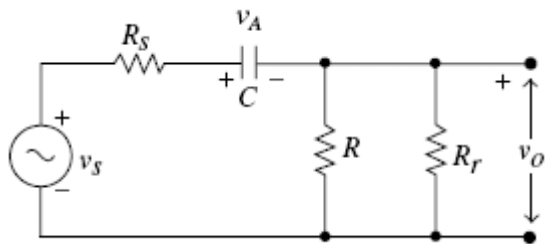
FIGURE 5.9(a) The circuit when D is OFF
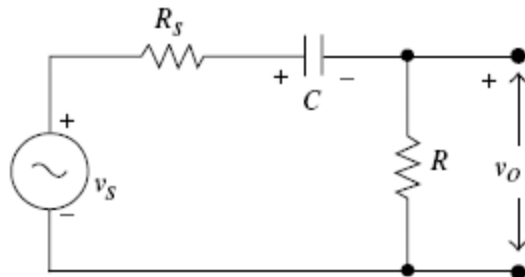
FIGURE 5.9(b) The circuit when $R_r >> R$
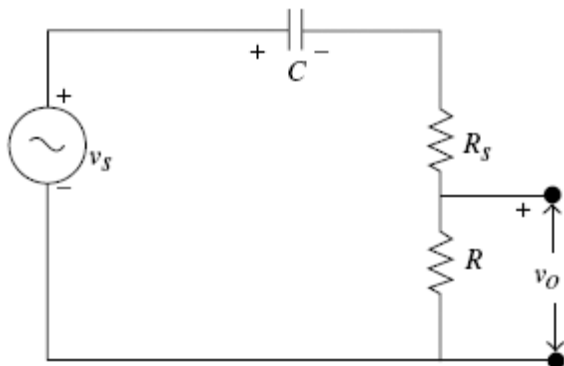
FIGURE 5.9(c) The circuit to calculate the output when the diode is OFF

Transient Response. Let us now consider the square wave v_s, shown in <u>Fig. 5.10(a)</u>, applied as input to the clamping circuit in <u>Fig. 5.7</u>. It is expected that the positive peak of the signal will be clamped to the zero level at the output almost instantaneously, but this does not happen. It takes a few cycles for the positive peak to be clamped to the zero level at the output. When the input is applied, the amplitude of the signal above the zero level goes on decreasing with each successive cycle. The output reaches the steady-state only after a few cycles from the instant the input is applied. The variation of the output with time during this period is called the transient response. At the end of this period when the positive peak is clamped to the zero level, the output is said to have reached the steady state.

We now examine how the output reaches the steady-state value after a few cycles (transient response). The variation of the output for the first few cycles, during the periods when the diode is ON and OFF, is then calculated. The input to the clamping circuit is a square wave with a peak-to-peak amplitude V and a finite frequency $f\,(= 1/T)$ as shown in <u>Fig. 5.10(a)</u>.

At $t = 0+$, the diode is ON. Using the equivalent circuit shown in <u>Fig. 5.8(c)</u>:

$$v_o(0+) = V \times \frac{R_f}{R_S + R_f}$$

If $R_s = R_f$; $v_o(0+) = \frac{V}{2}$
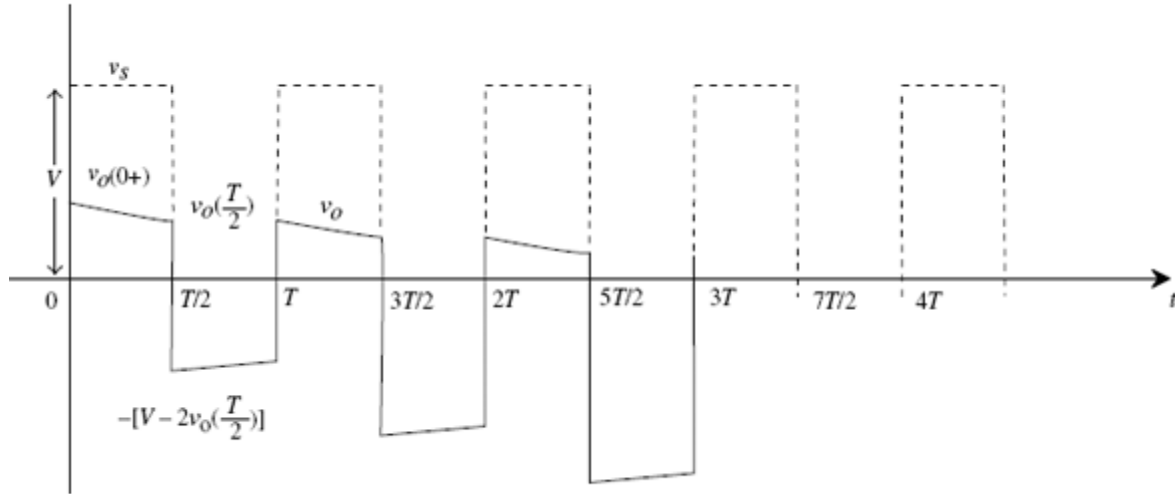
FIGURE 5.10(a) The input and output waveforms of the clamping circuit
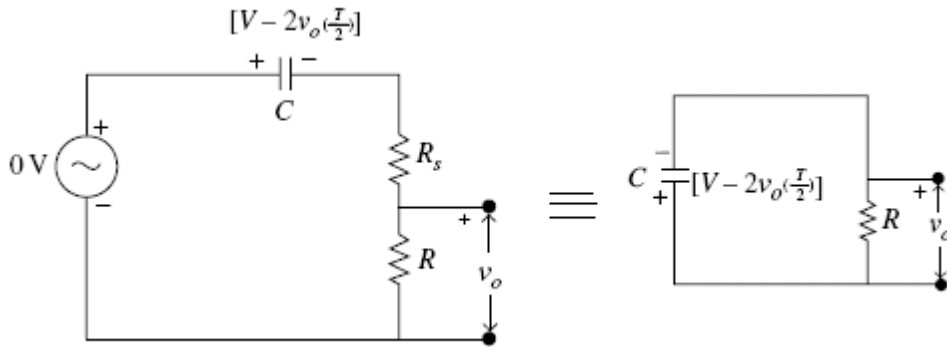
FIGURE 5.10(b) The equivalent circuit to compute the output when D is OFF

During the period 0 to $T/2$, as the input remains constant, the output decays exponentially with the time constant $\tau = C(R_s + R_f)$; and at $t = T/2$; the voltage across R_f is:

$$v_o\left(\frac{T}{2}\right) = v_o(0+)e^{-T/2\tau} = \frac{V}{2}e^{-T/2\tau}$$

Hence, the total voltage across $(R_s + R_f) = 2v_o$ $(T/2)$. The voltage across C is $[V - 2v_o$ $(T/2)]$.

Now at $t = T/2$, the input falls to 0 V, and the diode is OFF. The equivalent circuit shown in Fig. 5.10(b) is the same as the equivalent circuit shown in Fig. 5.9(c), except that the capacitor voltage is indicated here. Since $R_S << R$, the output voltage v_o is almost the same as $[V - 2v_o$ $(T/2)]$ but with a negative sign. Hence the output at $(T/2)+$ abruptly falls to $[V - 2v_o(T/2)]$. During the

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period T/2 to T, the input remains constant, the output decays exponentially with the time constant $\tau = C(R + R_s)$.

$$v_o(T) = -\left[V - 2v_o\left(\frac{T}{2}\right)\right]e^{-T/2\tau}$$

The input once again changes by V. The process is repeated over a few cycles till a steady-state value is reached.

Clamping the Output to a Reference Voltage (V_R)

In the clamping circuit seen in Fig. 5.7, the positive peak of the input signal is clamped to the zero level at the output. However, if the positive peak is to be clamped to a chosen reference voltage V_R for the circuit in Fig. 5.7, a dc voltage V_R is to be included in the output. The circuit in Fig. 5.15 shows a clamping circuit similar to that seen in Fig. 5.7 except for the fact that a reference voltage V_R is included and R_s is zero.

To obtain the steady-state response of the circuit, we assume that V_R is zero. This circuit, then, is the clamping circuit that clamps the positive peak of the input signal to V_γ as shown inFig. 5.7.

The steady-state responses for symmetric and unsymmetric square-wave inputs are plotted in Fig. 5.16(a) and Fig. 5.16(b), respectively.

Solving the four equations [Eqs. (5.6), (5.9), (5.10) and (5.11)], the values of V_1, , V_2 and   can be evaluated. To find these steady state output voltages with V_R included, add the value of V_R to each of these values. If, on the other hand, the polarity of V_R is reversed, add $-V_R$ to each of the values computed. The result is that the positive peak in the output is clamped to $-V_R$, as shown in Fig. 5.17.
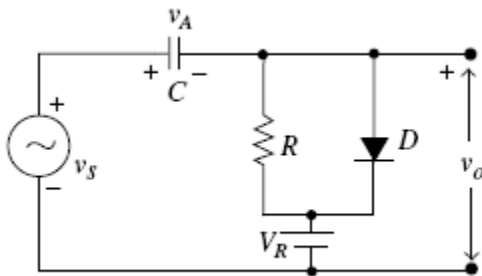
FIGURE 5.15 The circuit that clamps the positive peak of the input to V_R
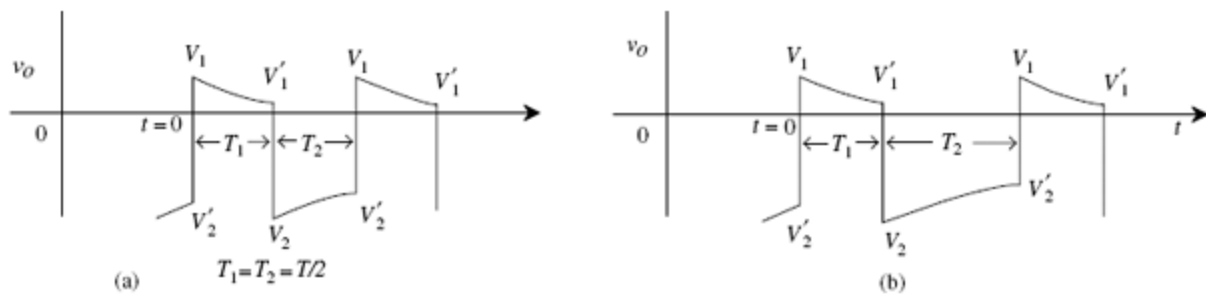
FIGURE 5.16 The steady-state response for (a) symmetric square-wave input; and (b) unsymmetric square-wave input
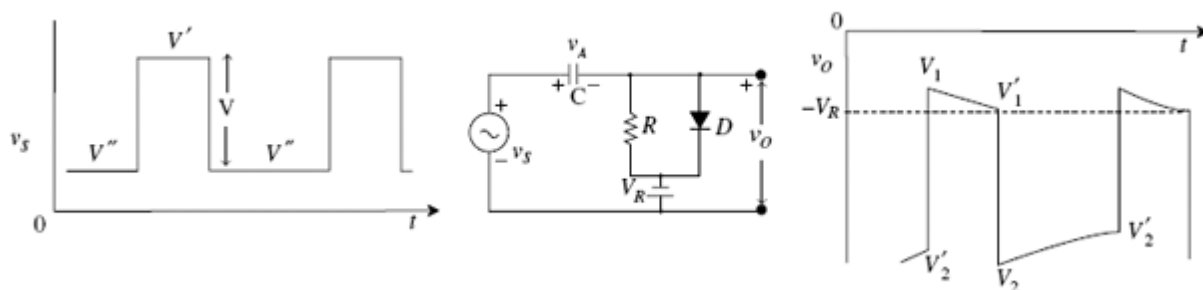
FIGURE 5.17 The positive peak of the input clamped to $-V_R$
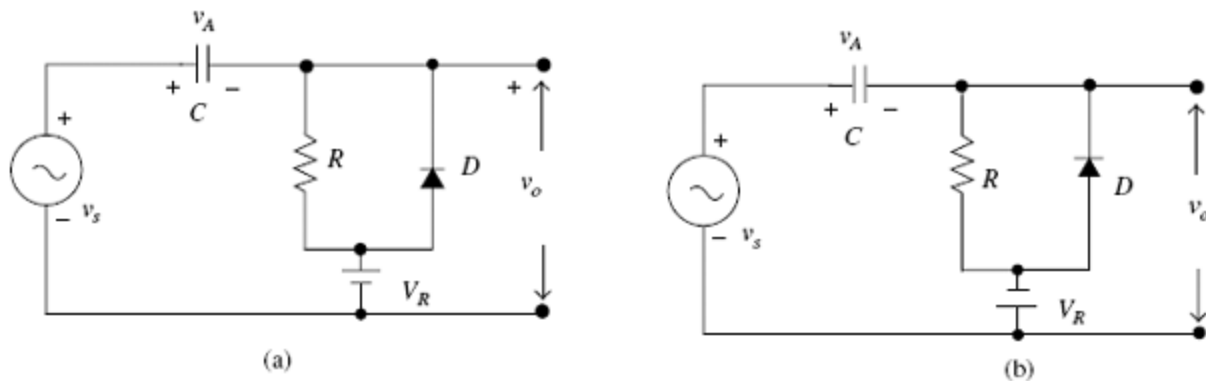
FIGURE 5.18 (a) The negative peak of the input clamped to $+V_R$; and (b) the negative peak of the input clamped to $-V_R$

Similarly, look at the circuits in <u>Fig. 5.18(a)</u> and (b). The circuits here clamp the negative peak of the input to $+V_R$ and $-V_R$ respectively. To simplify the analysis of the clamping circuits let us assume:

1.   The forward resistance of the diode D when ON is negligible. We assume that there is no distortion in the output when D is ON.
2.   The time constant $\tau\ (= RC)$ is so large when compared to the time period of the signal under consideration that practically there is no change in the voltage on the condenser C, when D is OFF.
3.   The internal resistance of the source v_s, $R_S = 0$.

Based on these assumptions, a simple and straight forward method to analyse clamping circuits is as follows:

Step 1: Start the analysis from the time duration during which D is ON. If the starting time duration keeps D OFF, skip that time interval.
Step 2: Consider the relevant circuit, taking care of the polarities of the voltages. Calculate v_o.
Step 3: Find v_A, the voltage on C.
Step 4: Consider the next time interval. Draw the circuit, taking care of the polarities of the input and v_A. Calculate v_o.

If the input is periodic you can plot the steady-state output. To understand the procedure let us consider an example.

THE EFFECT OF DIODE CHARACTERISTICS ON THE CLAMPING VOLTAGE

For the clamping circuit shown in <u>Fig. 5.7</u>, to obtain the steady-state response, the diode is replaced by R_f when ON and $R_r = \infty$ when OFF. Though the positive peak of the signal in the output is ideally required to be clamped to the zero level, in practice it is clamped to a voltage $V_{cl} = V_\gamma$, where V_γ is the cut-in voltage of the diode. In a practical diode, the current variation is non-linear in nature. Hence, we consider the influence of the diode characteristics on the clamping voltage, V_{cl} and show that the clamping voltage (V_{cl}) changes with a change in the amplitude of the input signal. Let us consider the clamping circuit described in <u>Fig. 5.7</u> and let its input be a symmetric square wave as shown in <u>Fig. 5.24(a)</u>.
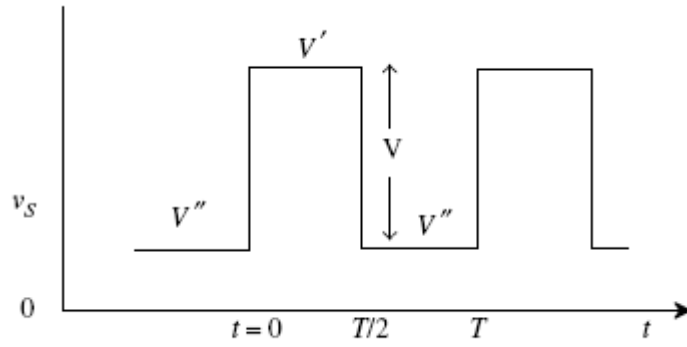
FIGURE 5.24(a) A symmetric square-wave input with peak-to-peak amplitude V

If C is large, irrespective of whether the diode is ON or OFF, the time constants are large so that the output is also a square wave. The steady-state output has a general form as shown in Fig. 5.24(b).
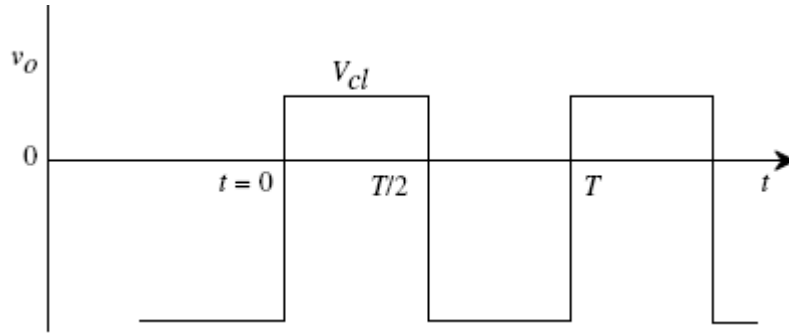
FIGURE 5.24(b) The steady-state output with a large C

In obtaining the steady-state response, we assumed that the diode is ideal with a small R_f. In practice, however, an idealized diode, when ON, is represented as a switch in series with a battery voltage of V_γ, a resistance R_f [see Figure 5.24(c)]; and biased by V' as shown in Fig. 5.24(a).

We now consider the V–I characteristic of the practical diode to understand the influence of the diode characteristics on the clamping voltage. The diode current is given by the relation:

$$I = I_0 e^{V/\eta V_T}$$

When the diode is ON, the positive peak of the signal is clamped to V_{cl} and the current in the diode is I_{cl}. V_{cl} is the voltage to which the positive peak is clamped.

$$I_{cl} = I_0 e^{V_{cl}/\eta V_T}$$
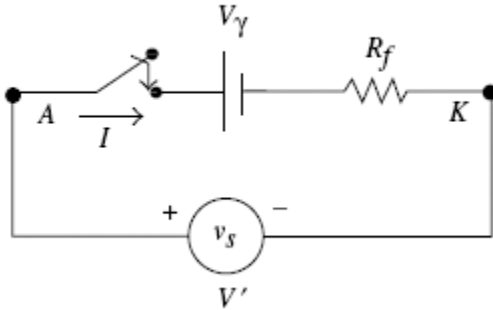
FIGURE 5.24(c) The equivalent circuit of the forward-biased diode

The equivalent circuit when the diode is ON, when $v_s = V'$ with $R_s = 0$ is shown in <u>Fig. 5.24(d)</u>. From <u>Fig. 5.24(d)</u>:

$$v_A = V' - V_{cl}$$

During the negative half-cycle of the square-wave input, $v_s = V''$ and the diode is OFF. The equivalent circuit is given in <u>Fig. 5.24(e)</u>.

From <u>Fig. 5.24(e)</u>:

$$v_A = V'' + v_o$$

And

$$v_o \simeq V - V_{cl}$$

Using <u>Eqs. (5.24)</u> and <u>(5.25)</u>:

$$v_A - V'' = V - V_{cl}$$

In practice, $V_{cl} \approx V_\gamma$ and V can be typically of the order of a few tens of volts. Thus, $V >> V_{cl}$. From <u>Eq. (5.26)</u>:

$$v_A - V'' = V$$
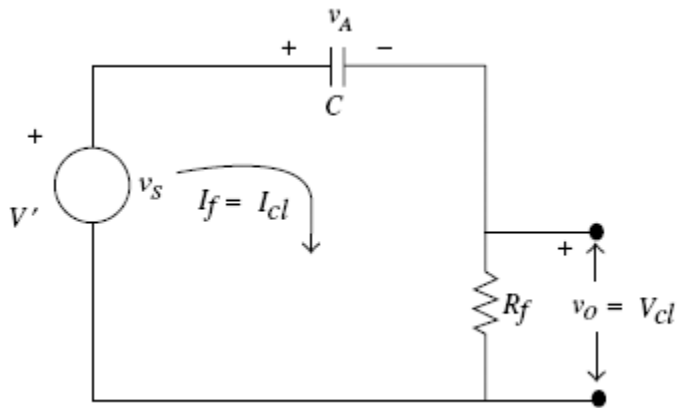
FIGURE 5.24(d) The equivalent circuit when the diode is ON
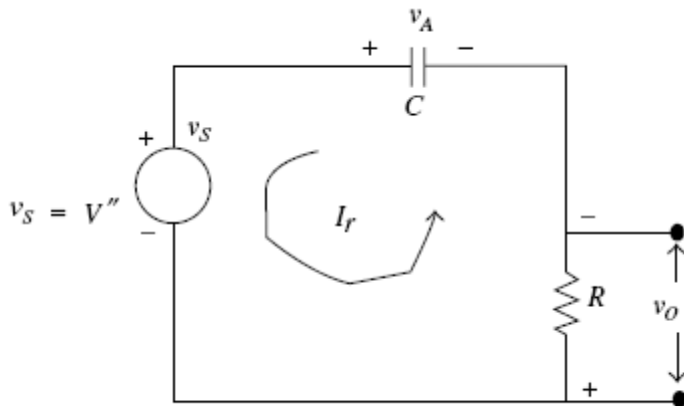
FIGURE 5.24(e) The equivalent circuit when the diode is OFF

As the net voltage across R is V, I_r the discharging current of C is given by the relation:

$$I_r = \frac{V}{R}$$

As the input is a symmetric square wave, under steady-state, the charge gained by C when the diode is ON should be equal to the charge lost by C when the diode is OFF.

Therefore,

$$I_{cl} = I_r$$

From Eqs. (5.22) and (5.28):

$$\frac{V}{R} = I_o e^{V_{cl}/\eta V_T}$$

$$e^{V_{cl}/\eta V_T} = \frac{V}{I_o R}$$

Taking logarithms to the natural base:

$$\frac{V_{cl}}{\eta V_T} = \ln \frac{V}{I_o R}$$

$$V_{cl} = \eta V_T \ln \frac{V}{I_o R}$$

$$\frac{dV_{cl}}{dV} = \eta V_T \times \frac{I_o R}{V} \times \frac{1}{I_o R} = \frac{\eta V_T}{V}$$

$$dV_{cl} = \eta V_T \times \frac{dV}{V}$$

Equation (5.31) gives the steady-state clamping voltage and Eq. (5.32) describes the variation in the clamping voltage with a change in the amplitude of the input signal. For a silicon diode used in a clamping circuit for which $V_{cl} = V_\gamma = 0.5$ V, $\eta = 2$, $V = 10$ V and $dV = 1$ V:

$$dV_{cl} = 2 \times 26\,\text{mV} \times \frac{1}{10} = 5.2\,\text{mV}$$

Equation (5.32) suggests that as V increases, the change in the clamping voltage, dV_{cl}, becomes smaller. Also, when the diode is ON, V is the forward-bias. Hence, to ensure that the clamping voltage remains unaltered, the diode must be forward-biased by a larger voltage. The circuit for this is represented in Fig. 5.25(a).

Let us now try to calculate dV_{cl} for this circuit to verify whether this arrangement really ensures negligible change in V_{cl} or not. Redrawing the circuit in Fig. 5.25(a) gives Fig. 5.25(b). The equivalent circuit when the diode is ON, i.e., when $v_s = V$, is shown in Fig. 5.25(c).
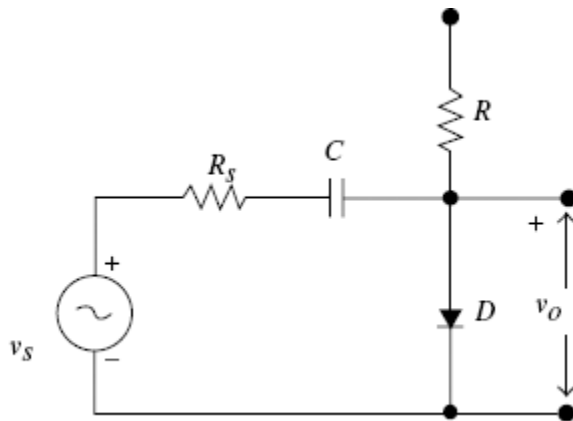
FIGURE 5.25(a) A clamping circuit in which the diode is forward-biased by a large voltage V_{YY}
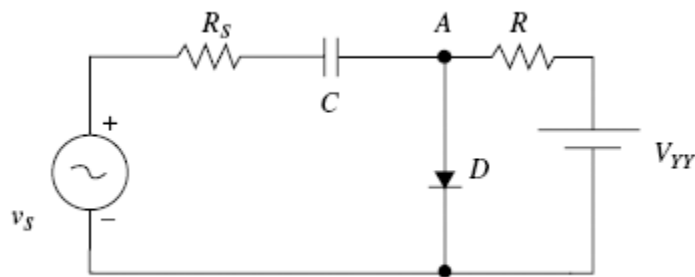
FIGURE 5.25(b) The modified circuit of Fig. 5.25(a)

From Eq. (5.22):

$$I_{cl} = I_o e^{V_{cl}/\eta V_T}$$

From Fig. 5.25(c):

$$I_R = \frac{V_{YY} - V_{cl}}{R} \approx \frac{V_{YY}}{R}$$

as $V_{cl} << V_{YY}$.

Writing the KCL equation at node A:

$$I_f + I_R - I_{cl} = 0$$

$$I_f = I_{cl} - I_R = I_{cl} - \frac{V_{YY}}{R}$$

Also,

$$v_A = V' - V_{cl} - I_f R_s = V' - V_{cl} - \left(I_{cl} - \frac{V_{YY}}{R}\right) R_s \qquad (5.36)$$

When the input goes to V'', the diode is OFF and the equivalent circuit is as shown in Fig. 5.25(d).

The discharging current I_r is:
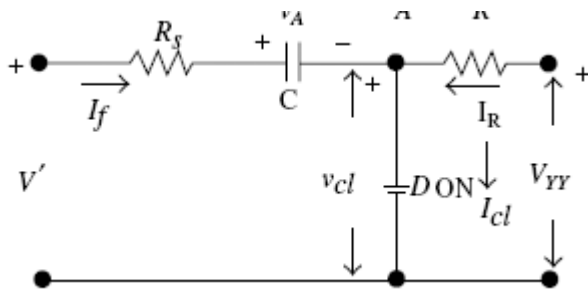
FIGURE 5.25(c) The equivalent circuit of Fig. 5.25(b) when the diode is forward-biased
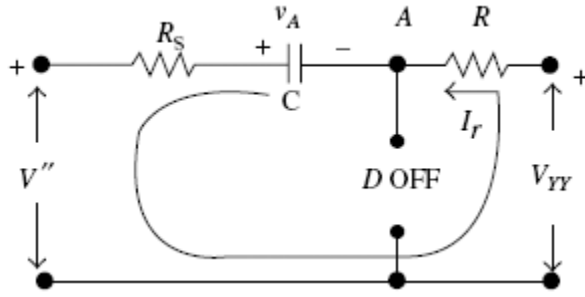
FIGURE 5.25(d) The equivalent circuit of Fig. 5.25(b) when the diode is OFF

$$I_r = \frac{V_{YY} - V'' + v_A}{R + R_S} = \frac{V_{YY} - V'' + v_A}{R} \tag{5.37}$$

since $R >> R_S$. Put Eq. (5.36) in (5.37):

$$I_r = \frac{1}{R}\left[V_{YY} - V'' + V' - V_{cl} - \left(I_{cl} - \frac{V_{YY}}{R}\right)R_S\right] = \frac{1}{R}\left[V_{YY}\left(1 + \frac{R_S}{R}\right) - V'' + V' - V_{cl} - I_{cl}R_S\right]$$

But $V' - V'' = V$. Therefore:

$$I_r = \frac{1}{R}\left[V_{YY}\left(1 + \frac{R_S}{R}\right) + V - V_{cl} - I_{cl}R_S\right]$$

We know that $V >> V_{cl}$ and $R_S << R$. Therefore:

$$I_r = \frac{1}{R}\left[V_{YY} + V - I_{cl}R_S\right] \tag{5.38}$$

As the input is a symmetric square wave, $I_f = I_r$. Therefore, from Eqs. (5.35) and (5.38):

$$I_{cl} - \frac{V_{YY}}{R} = \frac{1}{R}\left[V_{YY} + V - I_{cl}R_S\right]$$

$$I_{cl}\left(1 + \frac{R_S}{R}\right) = \frac{1}{R}\left[V_{YY} + V_{YY} + V\right] = \frac{2V_{YY} + V}{R}$$

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As $R_S << R$:

$$I_{cl} = \frac{2V_{YY} + V}{R} \tag{5.39}$$

From Eq. (5.22):

$$I_{cl} = I_0 e^{V_{cl}/\eta V_T} \qquad \frac{2V_{YY} + V}{R} = I_0 e^{V_{cl}/\eta V_T}$$

Taking logarithms to the natural base:

$$V_{cl} = \eta V_T \ln\left(\frac{2V_{YY} + V}{I_0 R}\right) \tag{5.40}$$

$$\frac{d}{dV} V_{cl} = \eta V_T \frac{I_0 R}{2V_{YY} + V} \times \frac{1}{I_0 R} = \frac{\eta V_T}{2V_{YY} + V}$$

$$dV_{cl} = \eta V_T \frac{dV}{2V_{YY} + V} \tag{5.41}$$

SYNCHRONIZED CLAMPING

In the clamping circuits examined in this chapter, the duration for which clamping is effective is controlled by the signal alone—the signal remains clamped as long as its amplitude remains unaltered. However, in some applications it may become necessary that the time of clamping be determined by the control or gating signal that occurs synchronously with the signal. Two or more signals are said to be synchronized if they arrive at a particular reference point in their cycles at the same time. The simultaneous presence of the gating signal during the period of constant amplitude input enables the two waveforms to be synchronized and the output to be referenced to V_R. One typical application could be in a CRO, where, for the spot to move vertically, the signal

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applied to the X-deflecting plates of the CRT varies in both directions but returns to a reference level V_R, as shown in Fig. 5.26(a).
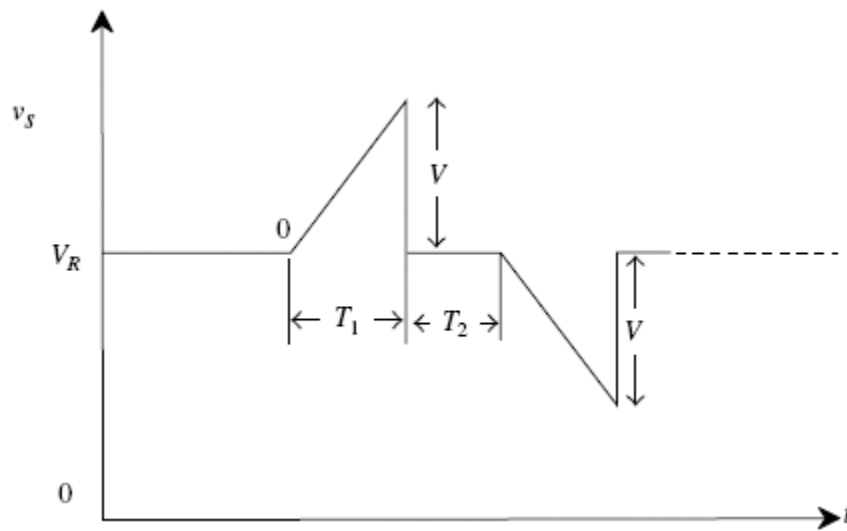
FIGURE 5.26(a) The signal that varies in both directions but is referenced to V_R

Let the signal then be transmitted through a capacitive coupled network like a high-pass network shown in Fig. 5.26(b).

For the duration 0 to T_1, when the input is a ramp, the output varies exponentially from point A with a time constant τ. At $t = T_1$, both the input and the output fall by V, giving rise to an undershoot. During the interval T_1 to T_2, as the input remains constant, the output decays exponentially to zero (point B). A similar variation takes place during the period the signal is negative. The resultant output waveform v_o is shown in Fig. 5.26(c).
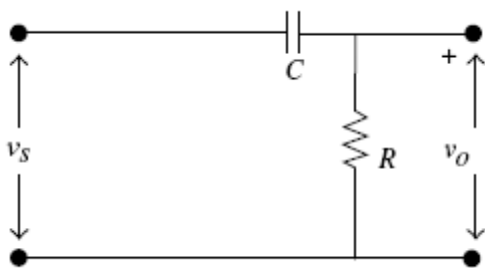
FIGURE 5.26(b) A high-pass RC circuit
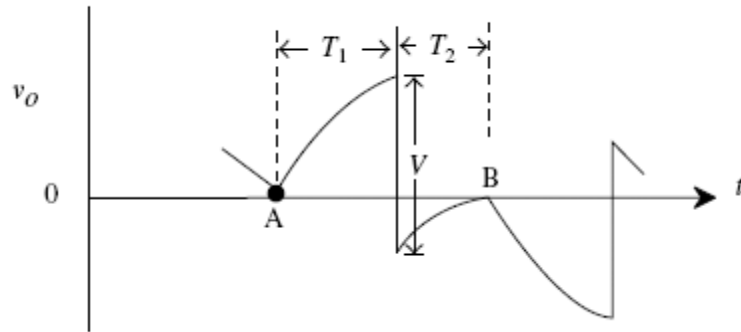
FIGURE 5.26(c) The output of a capacitive coupling network (high-pass circuit)

This output is devoid of a dc component. To reintroduce the dc component, we apply a signal referenced to the zero level [see Fig. 5.27(a)] as input to the circuit, as shown in Fig. 5.27(b). The output waveform of this circuit is shown in Fig. 5.28.
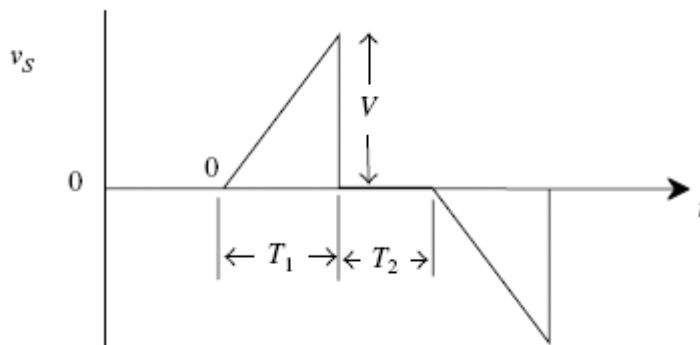
FIGURE 5.27(a) The input signal;
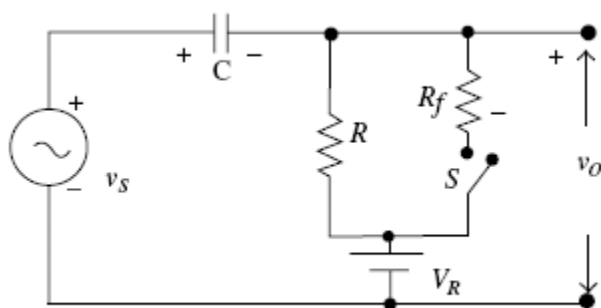
(b) The switch S operates in sync with the signal to clamp the output to V_R
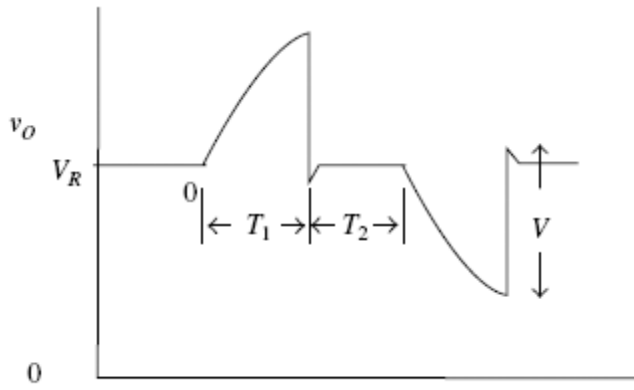
FIGURE 5.28 The output of the circuit in Fig. 5.27(b)
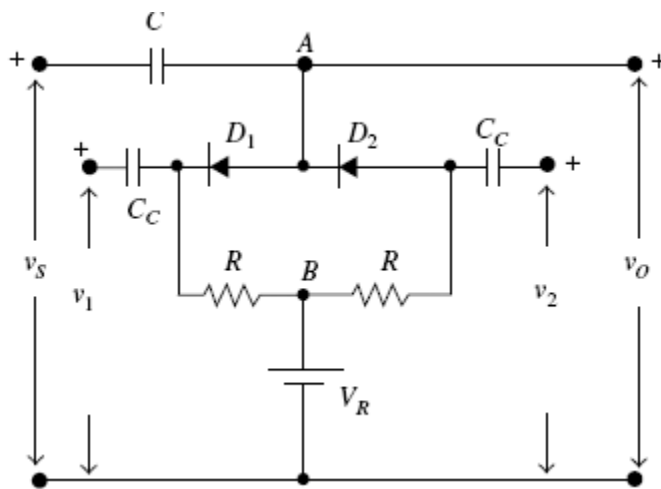
FIGURE 5.29(a) A synchronized clamping circuit

When the switch S closes, during the interval T_2, $v_o = V_R$. When the switch S opens during the interval T_1, C charges resulting in the waveform shown in Fig. 5.28. The small spikes can be reduced to negligible values if the switch has a zero resistance in the ON position.

The circuit in Fig. 5.27(b) can be implemented practically using diodes D_1 and D_2, and two control signals v_1 and v_2, with a 180° phase shift, as shown in Figs. 5.29(a), 5.30(a) and 5.30(b). If the signal in Fig. 5.30(c) is referenced to the zero level; the output in Fig. 5.30(d) is referenced to V_R.
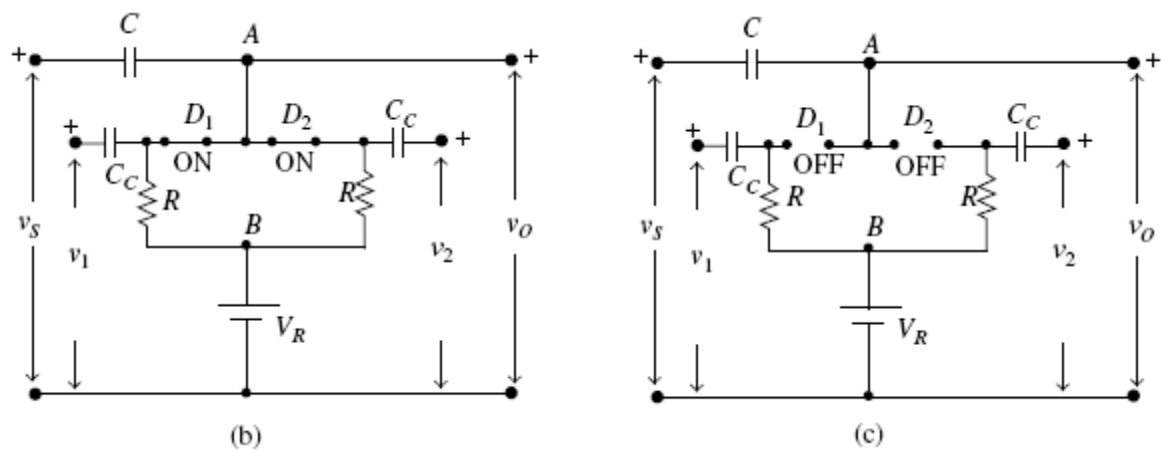
FIGURE 5.29(b) The circuit when D_1 and D_2 are ON; and (c) the circuit when D_1 and D_2 are OFF
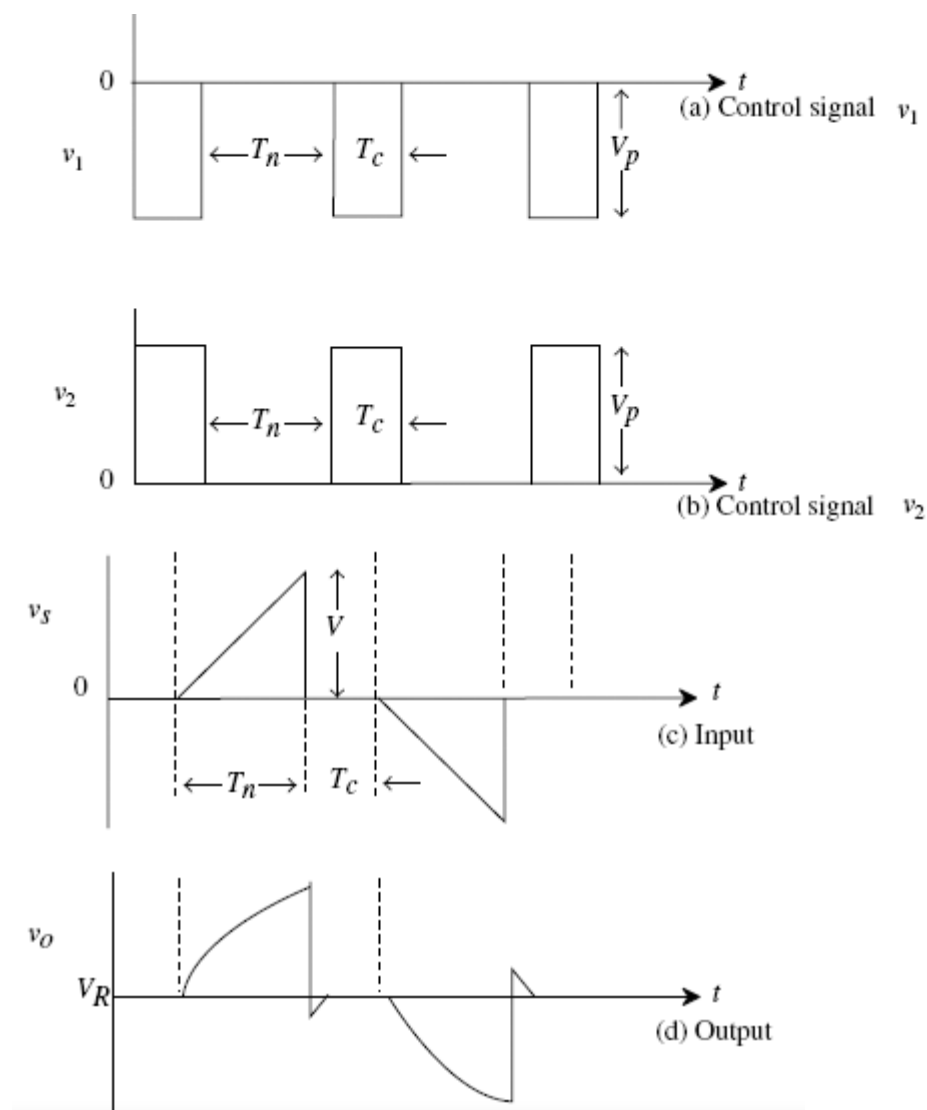
FIGURE 5.30 The waveforms of a synchronized clamping circuit

T_c is the time duration of the control signals and T_n is the time period during which the control signals are zero. The input to the clamping circuit is synchronized with the control signals v_1 and v_2. Since the input v_s is referenced to the zero level, the purpose of this circuit is to introduce a dc voltage (V_R) so that the output v_o is now referenced to V_R instead of the zero level. From the circuit in Fig. 5.29(a), it is evident, for the given polarities of the control signals that the diodes D_1 and D_2 conduct during the period T_c, resulting in the circuit of Fig. 5.29(b). As v_1 and v_2 are of equal magnitudes but of the opposite polarity, their net effect is zero at the output. The result is the output V_R.

However, when the control signals are zero, diodes D_1 and D_2 are OFF, resulting in the circuit of Fig. 5.29(c). The input is transmitted to the output terminals with a slight distortion in amplitude, as the capacitor charges exponentially. The output of this circuit is now referenced to V_R, meaning that a dc voltage V_R is introduced by the clamping circuit.

THE CLAMPING CIRCUIT THEOREM

This theorem enables us to calculate the voltage level to which the output is clamped by considering the areas above and below the reference level, when the values of R_f and R are known.

The clamping circuit theorem states that under steady-state conditions, for any input waveform, the ratio of the area under the output voltage curve in the forward direction to that in the reverse direction is equal to the ratio R_f/R. To prove the clamping circuit theorem, consider a typical steady-state output for the clamping circuit, represented in Fig. 5.31.

In the time interval t_1 to t_2, D is ON. Hence, during this period, the charge builds up on the capacitor C. If i_f is the diode current, the charge gained by the capacitor during the interval t_1 to t_2 is:

$$q_1 = \int_{t_1}^{t_2} i_f \, dt \tag{5.43}$$

However, $i_f = V_f/R_f$, where V_f is the diode forward voltage:

$$q_1 = \frac{1}{R_f} \int_{t_1}^{t_2} V_f \, dt \tag{5.44}$$

During the interval t_2 to t_3, D is OFF. Hence, the capacitor discharges and the charge lost by C is:

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$$q_2 = \int_{t_2}^{t_3} i_r \, dt \qquad\qquad (5.45)$$
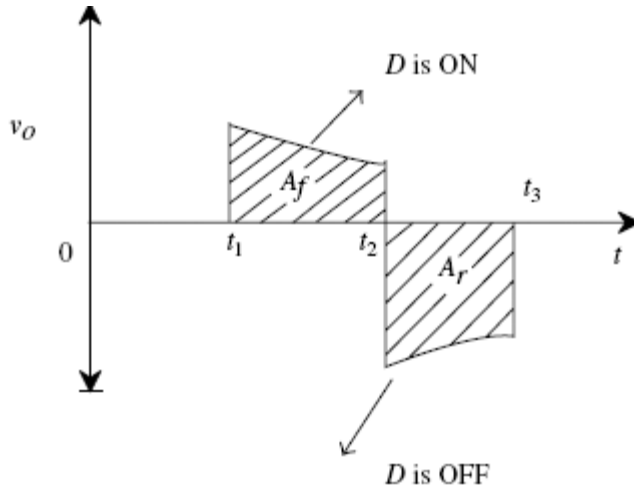
FIGURE 5.31 Typical steady-state output of the clamping circuit

Put $i_r = V_r/R$, where V_r is the diode reverse voltage:

$$q_2 = \frac{1}{R} \int_{t_2}^{t_3} V_r \, dt \qquad\qquad (5.46)$$

At steady state, the charge gained is equal to the charge lost. In other words, $q_1 = q_2$.

Therefore,

$$\frac{1}{R_f} \int_{t_1}^{t_2} V_f \, dt = \frac{1}{R} \int_{t_2}^{t_3} V_r \, dt \qquad\qquad (5.47)$$

However,

$$A_f = \int_{t_1}^{t_2} V_f \, dt \quad \text{and} \quad A_r = \int_{t_2}^{t_3} V_r \, dt \qquad (5.48)$$
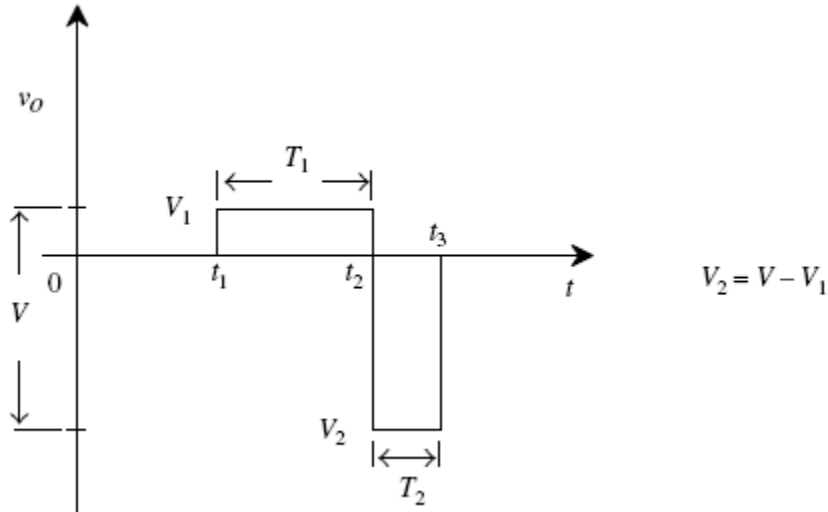
FIGURE 5.32 The output of the clamping circuit when C is large

Here, A_f is the area with D in the ON state and A_r is the area under the output curve with D in the OFF state.

From Eqs. (5.47) and (5.48):

$$\frac{A_f}{R_f} = \frac{A_r}{R} \quad \text{or} \quad \frac{A_f}{A_r} = \frac{R_f}{R} \qquad (5.49)$$

This relation is known as the clamping circuit theorem.

Consider Fig. 5.32 in which the output of the clamping circuit is assumed to remain almost constant during the periods T_1 and T_2 when the diode D is ON and OFF by choosing large values of C.

If V_1 and T_1 are the voltage and time duration above the reference level and V_2 and T_2 are the voltage and time duration below the reference level under steady-state, then as per this theorem:

$$\frac{A_f}{A_r} = \frac{V_1 T_1}{V_2 T_2} = \frac{V_1 T_1}{(V - V_1) T_2} = \frac{R_f}{R}$$

Assuming that T_1, T_2, R_f, R and the amplitude of the signal V are known, it is possible to compute the voltage level V_1 to which the signal is clamped at the output.

UNIT-3
Switching characteristics of Devices:

LEARNING OBJECTIVES

After studying this chapter, you will be able to:

- Use diodes and transistors as switches
- Describe the effect of inter-electrode capacitances on switching times
- Describe the switching times of devices and derive the necessary relations
- Describe the temperature dependence of the transistor on various parameters
- Understand the use of transistor switch as a latch
- Realize the use of transistor switches with inductive and capacitive loads

INTRODUCTION

Active devices such as semiconductor and diodes, transistors and FETs can be used as static switches. To use these switches for high-speed applications, it is necessary to know the influence of inter-electrode capacitors on the switching speed of these devices. For transistors, the switching speed can be improved with the use of speed-up capacitors and expressions for the switching times of a transistor are derived to calculate the turn-on and turn-off times of a transistor. Further, the choice of the supply voltage depends on the breakdown voltages of the transistor and the saturation parameters of the transistor are temperature dependent. The influence of temperature on these parameters is discussed in this chapter. Finally, a transistor switch with inductive or capacitive loads is considered and also the application of a transistor switch as a latch. In most applications, the ON transistor is driven into saturation. This in turn increases the storage time that results in a longer turn-off time, thereby reducing the switching speed. To overcome this problem, a non-saturating switch is discussed.

A *p-n* junction diode can be used as a switch. When the diode is forward-biased, the switch is said to be in the ON state and when it is reverse-biased, the switch is in the OFF state.

DIODES AS SWITCHES

A physical switch either makes or breaks a contact between two nodes, meaning the resistance between the nodes is either 0 or ∞. When electronic devices are used as switches, no physical contact is either made or broken; the resistance between the nodes is made either too small (ideally 0) or too large (ideally ∞). Diodes can be used as switches. We shall discuss the application of semiconductor and Zener diodes as switches in this section.

The Semiconductor Diode as a Switch

A semiconductor diode, used as a switch, is ON when forward-biased and OFF when reverse-biased. As such, this device may be used as a static switch. The voltage between the anode (A) and the cathode (K) is ideally zero; and hence, the resistance is zero when the switch is closed. In practice, however, there is a finite forward resistance (R_F), typically of a few ohms, as shown in Fig. 4.1(a). When the switch is open, ideally the current should be zero and the resistance infinity. However, in actuality, a diode will have a finite reverse resistance, R_r which is typically few mega ohms, as shown in Fig. 4.1(b).

Figure 4.2 shows the typical V–I characteristic of a semiconductor diode. Let the reverse saturation current be typically 50 μA. When compared to this, the forward current is as large as 100 mA. Hence, the reverse current is negligible when compared to the forward current. This diode can, thus, be used as a one-way device, i.e., as a switch. Let the diode be an ideal diode. The V–I characteristic of an ideal diode is represented in Fig. 4.3.

However, a diode has a barrier potential, and the idealized characteristic of silicon and germanium diodes are represented in Figs. 4.4(a) and (b), respectively.

Consider the diode circuit in Fig. 4.5(a). Now let the input (v_i) to such a diode switch be as shown in Fig. 4.5(b). The currents in the switch are represented in Fig. 4.5(c).

$R_F = 0$

$\leftarrow V_F = 0 \rightarrow$

$i = \infty$

i

R_F

A

K

(a)

$R_r = \infty$

$i = 0$

R_r

A

K
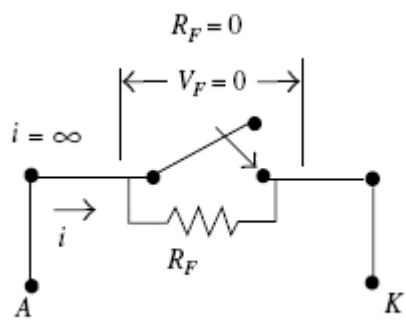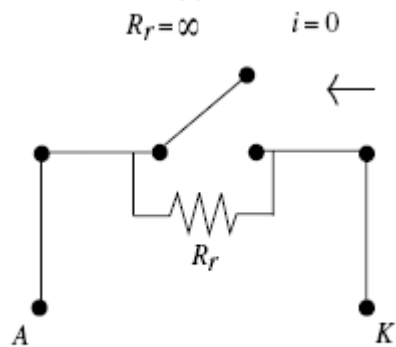
(b)

FIGURE 4.1 (a) Diode as a closed switch (b) Diode as an open switch

I_F mA

100 — — — — — — Forward characteristic

V_R

50 μA

V_F Volts

← Breakdown

I_R
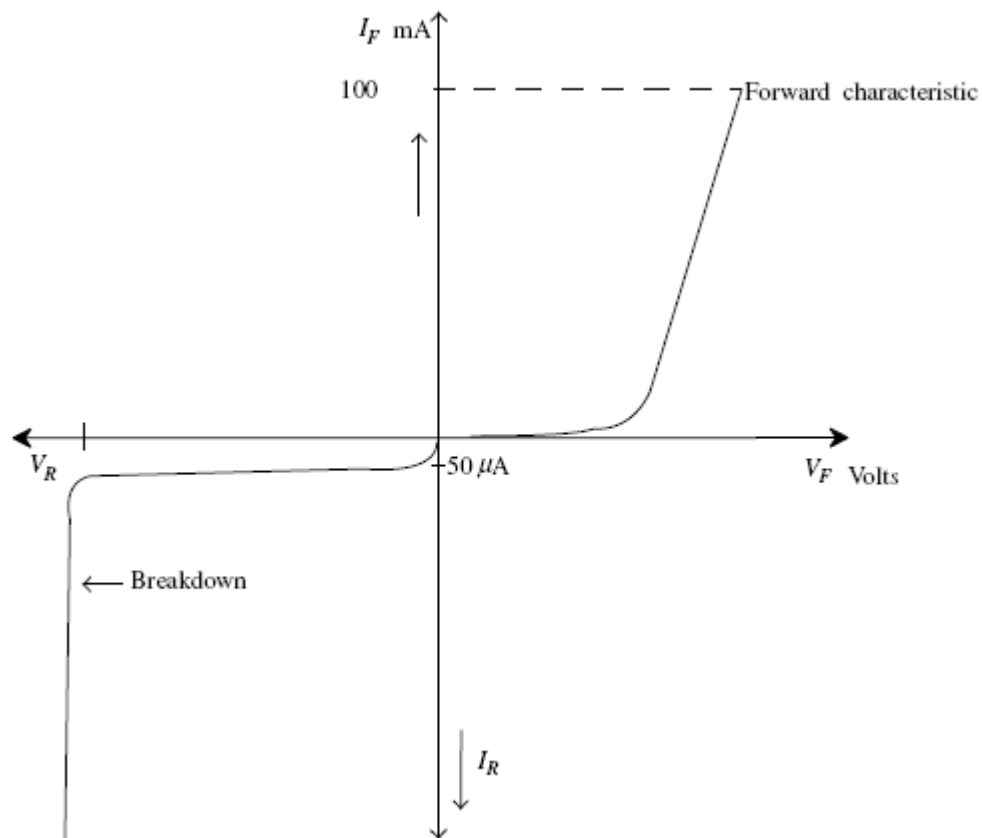
FIGURE 4.2 The V–I characteristic of a practical diode
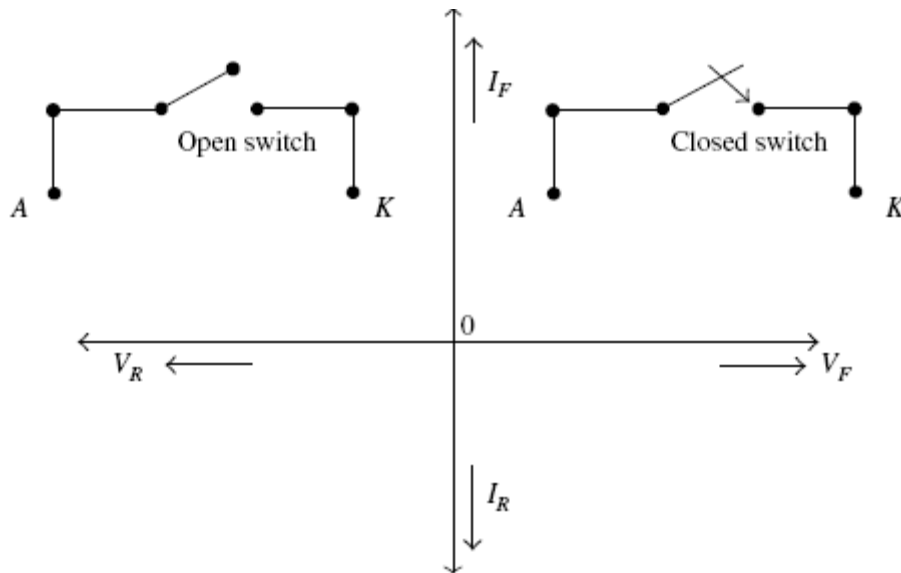
FIGURE 4.3 The V–I characteristic of an ideal diode
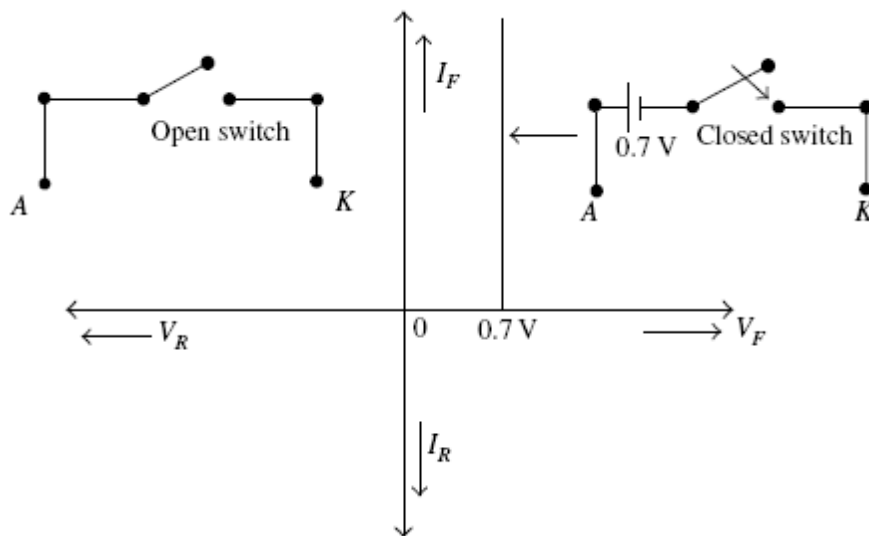
FIGURE 4.4(a) The idealized V–I characteristic of a silicon diode
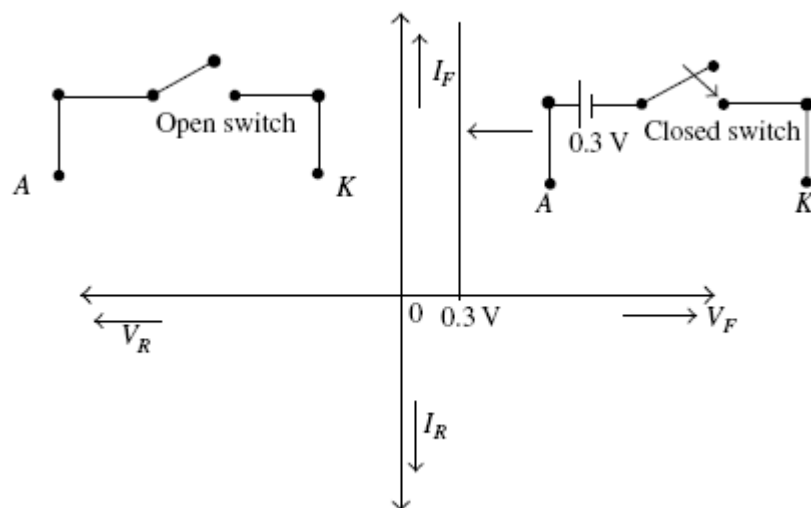
FIGURE 4.4(b) The idealized V–I characteristic of a germanium diode
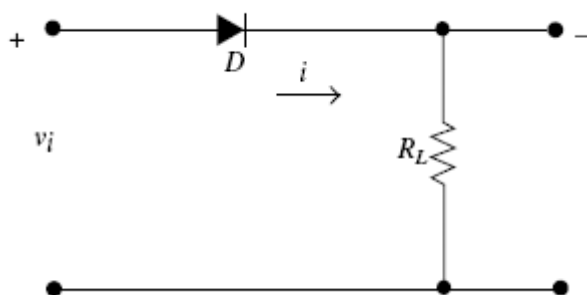
FIGURE 4.5(a) A simple diode circuit
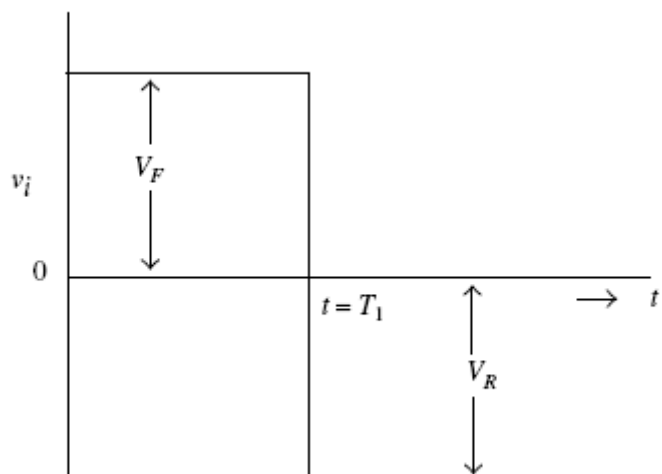
FIGURE 4.5(b) Suddenly changing input
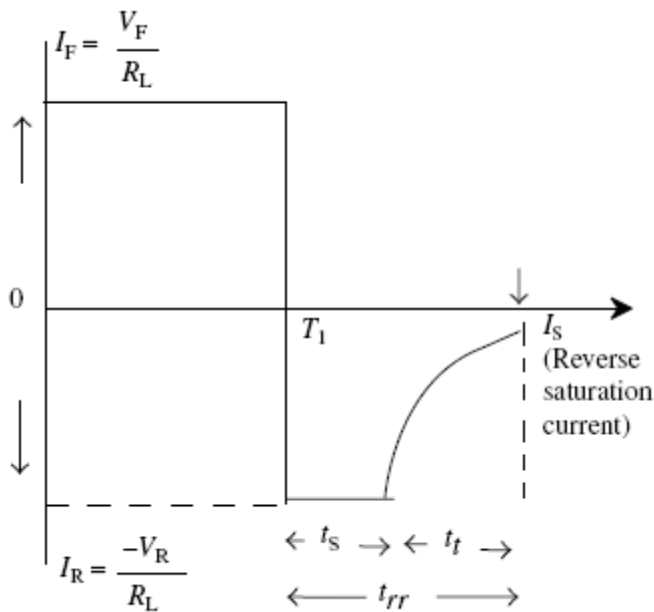
FIGURE 4.5(c) Diode currents

During the period 0 to T_1, the input forward-biases the diode. If the forward resistance of D is very small when compared to R_L, then $I_F = V_F/R_L$.

At T_1, the polarity of the input reverses and the reverse voltage is V_R. Thus, I_R ($= -V_R/R_L$) remains large for a time duration called the storage time t_s, though the diode is expected to go into the OFF state at T_1. This is because of the presence of a large number of stored charges on either side of the junction in the forward-biased diode. After this time interval, charges get cleaned up, gradually reducing the current to a value I_s after a time interval t_t called the transition time. At this instant, the diode is said to be switched from the ON state into the OFF state. It can be seen from Fig. 4.5(c) that a finite time elapses before the current is the reverse saturation current. This indicates that a diode is switched from the ON state into OFF state not exactly at T_1, when the input reverse-biases the diode but only after a time interval when the reverse current reaches I_s. The time interval ($t_s + t_t$) is called the reverse recovery time of the diode, t_{rr}.

This is the time interval for which the switch is still ON. The reverse recovery time, t_{rr}, may thus be defined as the time taken for the diode reverse current to fall to 10 per cent of its forward-current value when the diode is suddenly switched from the ON to the OFF state. If the forward current I_F, when the diode is ON, is 10 mA, then the time taken for this current to fall to 1 mA is the reverse recovery time. This can also be termed as the "turn-off" time of the diode. Similarly, when the device switches from the OFF state to the ON state, there is a small turn-on time, which is small when compared with the turn-off time. These time intervals tell us how fast we can switch the

diode from one state to the other. Further, a reverse-biased diode has a transition capacitance C_T between the anode and the cathode. At low frequencies, this capacitance has no appreciable influence. However, at high frequencies, this offers low reactance, which will have to be taken into consideration when we consider diode series and shunt clippers.

What is an ideal diode? How does an actual diode differ from an ideal diode?

Ans. Ideal diode: It is two terminal device and permits only unidirectional conduct. It conducts well in the forward direction poorly in reverse direction. It would have ideal if it acted as a conductor with zero resistance or zero voltage drop across it, when reverse bised. The volt ampere characteristics of such an ideal diode have been as shown in Fig.1 (b). An ideal diode acts like an automatic switch. The switch is closed when diode is forward biased and is opened when reverse baised.
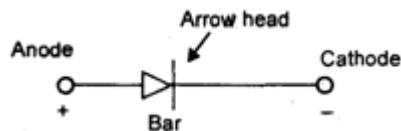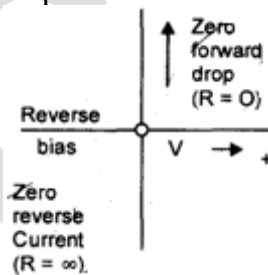
Fig. 1 :(a) Ideal diode   **Fig. 1(b) ideal diode Characteristics**

Closed
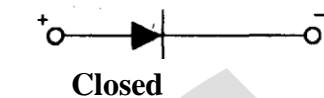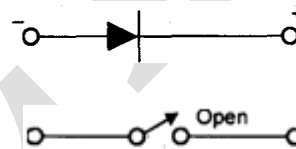
IN Forward Bias   **In Reverse bias**

Fig. 1. (c) Switch Analogy

Ideal diode is different from actual diode because, no diode can act as ideal diode. An actual diode does not behave as a perfect conductor when forward biased and as perfect insulator when reverse biased. Neither it offers zero resistance when forward biased nor infinite resistance when reverse biased.

However, there are many applications in which diodes can be assumed to be nearly ideal devices, if the voltage drop across the diode when it is forward biased i.e. v is taken into account. In cases when the circuit supply voltage V is much larger than the forward voltage drop v, v can be assumed constant without introducing any serious error. Also, the diode forward current 'I' is usually so much larger than the reverse saturation current I_0 so that the I_0 can just be ignored.Thease e assumptions lead to a nearly ideal or approximate characteristics for germanium silicon diodes as illustrated in fig. 1
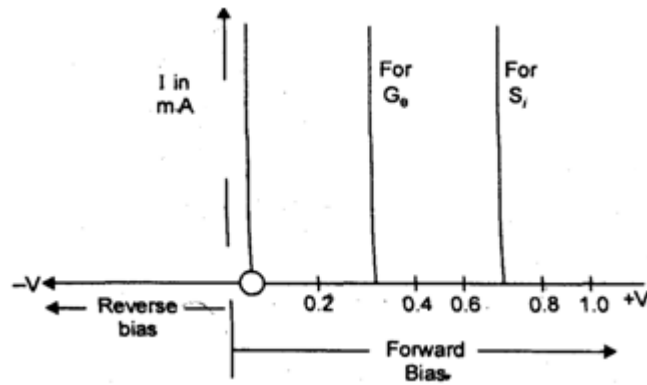
Explain various transistor switching times.

Ans.1. The time interval between the instant of application input pulse and output (collector) currant to attain 10 percent of its maximum value is termed as the delay time t_d .

2. Rise time, t_r is defined as the time required for the output currant I_C to go from 10% to 90% of its maximum value.

3. The sum of delay time, t_d and rise time, t_r is called the turn-ON time, t_{ON}.

   i.e. $t_{ON} = t_d + t_r$

4. TURN- OFF time t_{OFF} is made up of a storage time, t_s and a fall time t_F.

   i.e. $\left(t_{OFF} = t_s + t_F \right)$

5. Storage time, t_s is defined as the time interval between the end of the input pulse (trailing edge) and when the collector current falls to 90% of its maximum value.

                         OR

Storage time, t_s is equal to the sum of time taken in removing excess charge stored and the time taken by collector transition capacitance to discharge to 90% of its maximum but major portion of the time is taken in removing excess charge storage.

       The time duration of the output pulse measured between two 50% levels of rising and falling waveform is known as the **pulse width**.

For a fast-switching transistor, turn-on time t_{ON} and turn-off time t_{OFF} must be of the order of nano seconds.

(a) Pulse waveform
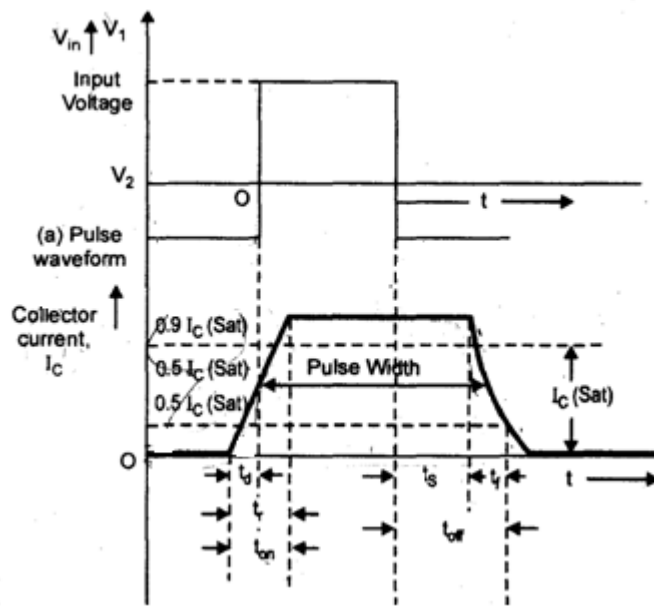
Fall time: The time required for the collector to drop from 90% to 10% of the saturation current is defined as a fall time t_F.

How is a transistor used as a switch.

Ans. A transistor can be employed as an electronic switch. Operating a transistor as a switch means it at either saturation or cut-off nowhere else along the load line. When a transistor is saturated it is like a closed switch from collector to emitter. When a transistor is cut off it is like an open switch.
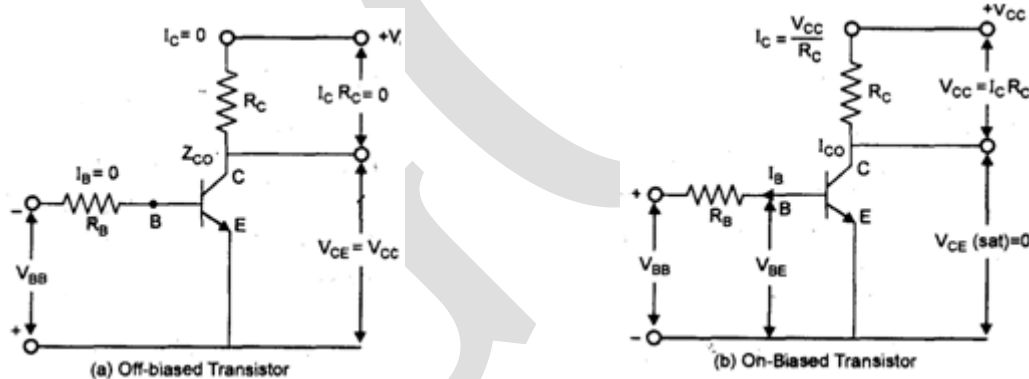
(a) Off-biased Transistor   (b) On-Biased Transistor

Fig. Operation of a Transistor as a switch

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Instead of a step, if a pulse is applied to the transistor switch, how does the device respond? To understand this, we consider the switching times of a transistor (see Fig. 6.24).

Let the input to the transistor switch be a pulse of duration T. When a pulse is applied, because of stray capacitances, collector current will not reach the steady-state value instantaneously. To know exactly when the device switches into the ON state and also into the OFF state, we define the following switching times of the transistor.
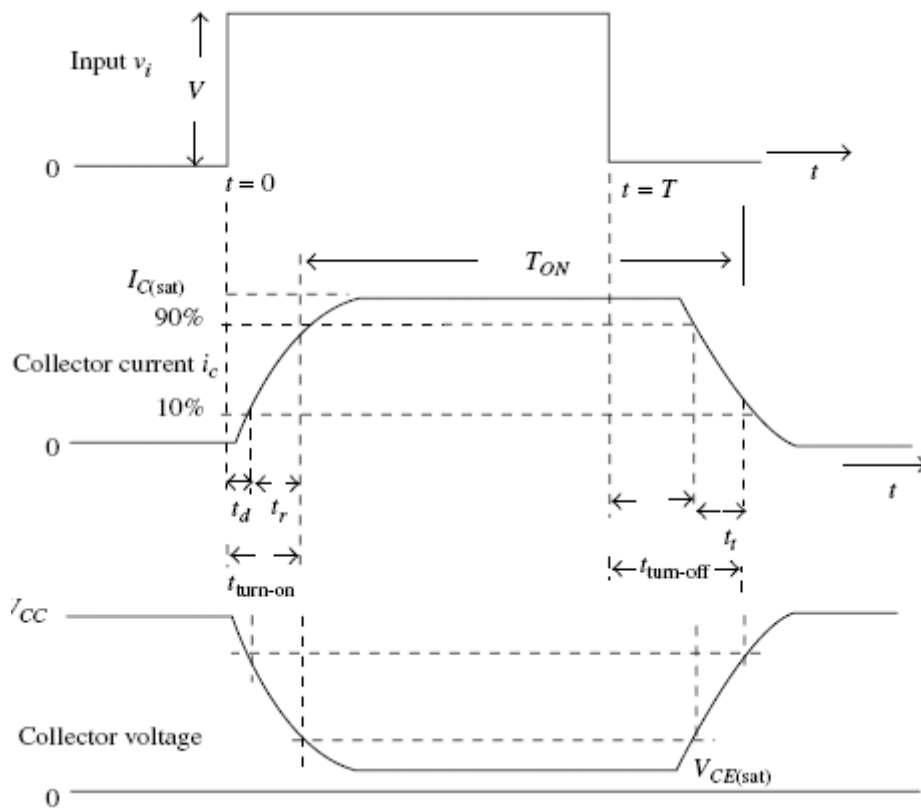
FIGURE 6.24 Switching times of the transistor

The Turn-on Time of a Transistor

Turn-on time of the transistor is the time taken by the transistor from the instant the pulse is applied to the instant the transistor switches into the ON state and is the sum of the delay time and rise time. To find out the turn-on time of the transistor, the delay time and rise time have to be calculated.

Delay Time (t_d). It is the time taken for the collector current to reach from its initial value to 10 per cent of its final value.

If the rise of the collector current is linear, the time required to rise to 10 per cent $I_{C(sat)}$ is 1/8 the time required for the current to rise from 10 per cent to 90 per cent $I_{C(sat)}$.

It is given as:

$$t_d = \frac{1}{8} t_r$$

where, t_r is the rise time.

Rise Time. Rise time, t_r is the time taken for the collector current to reach from 10 per cent of its final value to 90 per cent of its final value. From Fig. 6.24 it is seen that the moment input pulse is zero, the collector current is expected to fall to zero. However, because of the stored charges, the current remains unaltered for sometime interval t_{s1} and then begin to fall. The time taken for this current to fall from its initial value at t_{s1} to 90 per cent of its initial value is t_{s2}. The sum of these t_{s1} and t_{s2} is approximately $t_{s1} = t_s$ and is called the storage time.

BREAKDOWN VOLTAGES

We have seen that by the application of a signal of proper polarity and magnitude, a transistor switch can be driven into saturation. As a result, the voltage at the collector of the device is $V_{CE(sat)}$ (typically 0.1 V for Ge and 0.2 V for Si). Now, when a signal of opposite polarity is applied as input to the switch, ideally the voltage at the collector rises to V_{CC}. Thus, we see that the change in voltage at the collector is $V_{CC} - V_{CE(sat)} \approx V_{CC}$. This output is connected to operate some other circuits. For proper operation, it is desirable that V_{CC} be made reasonably large. However, by increasing the value of V_{CC}, the reverse-bias voltage on the collector base diode could become so large that an avalanche breakdown may occur in the collector diode. The leakage current I_{CO} will then become $M_n I_{CO}$ where, M_n is the avalanche multiplication factor. M_n depends on V_{CB}. An empirical relation for M_n, applicable for many transistor types is given as:

$$M_n = \frac{1}{1 - \left(\dfrac{V_{CB}}{V_{CBO(max)}} \right)^n} \tag{6.48}$$

Here, $V_{CBO(\max)}$ is a maximum reverse-bias voltage that can be applied between the collector and base terminals of the transistor when the emitter lead is open-circuited and n is typically in the range of 2 to 10 which controls the sharpness of onset of a breakdown. Calculation of M_n is illustrated in the Example 6.12.

The Breakdown Voltage with Base Not Open Circuited

Consider the figure shown in Fig. 6.31. $V_{CEO(\max)}$ is the breakdown voltage between the collector and emitter terminals with the base lead open. Now, if the base lead is not open circuited, but a resistance R_B is connected between the base and emitter terminals, the new breakdown voltage may be termed as $V_{CER(\max)}$. The expectation is that $V_{CER(\max)}$ lies somewhere between $V_{CEO(\max)}$ and $V_{CBO(\max)}$. Let us try to calculate the value of $V_{CER(\max)}$.
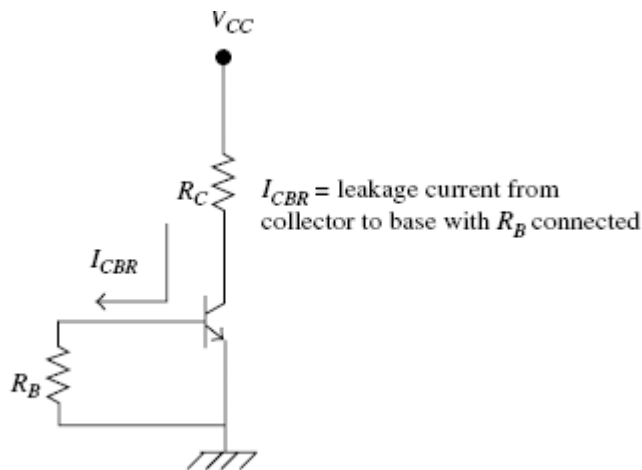
FIGURE 6.31 R_B is connected between base and emitter terminals

It is known that unless a voltage of V_γ exists between base and emitter terminals, the diode forward current is small and the collector to base leakage current will now flow through R_B. Once the forward-bias voltage of the base emitter diode is more than V_γ, a large current flows through the collector and the corresponding breakdown voltage is $V_{CEO(\max)}$. Breakdown occurs when V_{CE} is greater than $V_{CEO(\max)}$. When the threshold voltage V_γ is reached, at that instant the collector current is $M_n I_{CO}$. Thus, at breakdown the current through R_B is $M_n I_{CO}$.
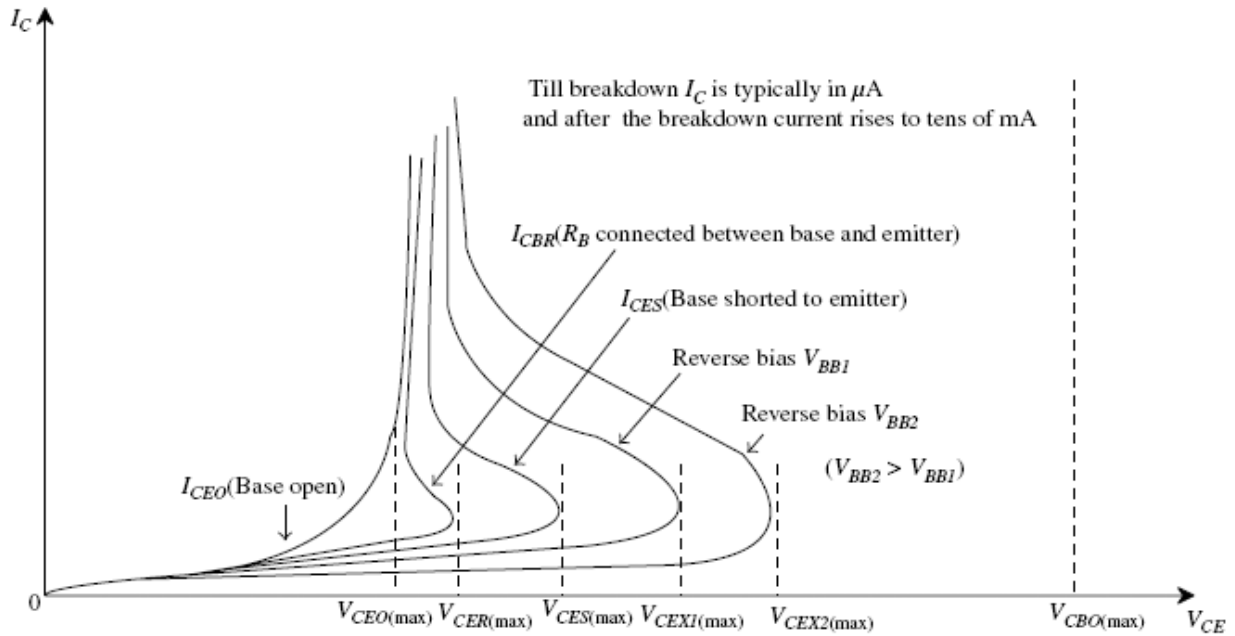
FIGURE 6.34 $I_C vs. V_{CE}$ extended into breakdown region for different conditions

1.   When the base is open circuited ($I_C = I_{CEO}$)
2.   When R_B is connected between the base and emitter
3.   When R_B is connected with a reverse-bias voltage V_{BB}.

From Fig. 6.34, it is apparent that breakdown occurs at $V_{CEO(max)}$ with base lead open at the point, the current rises abruptly. $V_{CEO(max)}$ is called the sustaining voltage. When R_B is connected between the base and emitter, the breakdown occurs at a larger voltage $V_{CER(max)}$. After breakdown the voltage returns to the sustaining voltage. If $R_B = 0$, breakdown occurs at a slightly larger voltage. Further, we also see from the characteristics that if the emitter diode is reverse-biased, the breakdown occurs at a still larger voltage. The larger is the reverse-bias voltage, the larger is the breakdown voltage. These characteristics explain the possible breakdown voltages for different conditions on the emitter diode, so that at these prohibited voltages the transistor is not operated. The currents for all the possible connections (except for I_{CEO}) give two values for the same voltage. Also, once the breakdown occurs current in the transistor increases with decreasing voltage, which means that the transistor exhibits negative resistance characteristic. The transistor when used in the breakdown region is called an avalanche transistor.

From Eq. (6.59) we see that $V_{CEO(max)}$ is dependent on h_{FE} which in turn depends on the collector current I_C. DC current gain is the ratio of I_C/I_B at an operating point and is designated as h_{FE} or β_{dc}.

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The parameter h_{FE} is useful in determining whether a transistor is in saturation or not and it varies with collector current I_C (see Fig. 6.30). Typically h_{FE} varies as shown in Fig. 6.35 which is called current gain characteristic.

THE SATURATION PARAMETERS OF A TRANSISTOR AND THEIR VARIATION WITH TEMPERATURE

The output characteristics of n–p–n transistor having P_T = 250 mW at room temperature in the CE configuration are given in Fig. 6.36. The dc load line for R_L = 400 Ω is superimposed on the characteristics. However, from the characteristics in Fig. 6.36 the saturation voltage $V_{CE(sat)}$ can not be found as its value is typically a fraction of a volt (0.1 V for Ge and 0.2 V for Si). A transistor is said to be in saturation when the emitter and collector diodes are forward-biased.

R_L = 400 Ω, V_{CC} = 10 V

To draw the dc load line:

$$I_{C(sat)} = \frac{10V}{400\,\Omega} = 25\,mA$$

$V_{CE(cut\text{-}off)} = V_{CC} = 10$ V

To be able to read $V_{CE(sat)}$, the characteristics in the voltage range 0 to 0.5 V are expanded and the dc load line for R_L = 400 Ω is again superimposed, as shown in Fig. 6.37(a). The region [see Fig. 6.37(b)] around I_B = 0.175 mA is expanded to see the variation in I_C for larger values of I_B as shown as the dotted region in Fig. 6.37(a). It is seen for I_B > 0.175 mA, that there is no appreciable change in the collector current for a change in the base current as shown in Fig. 6.37(b), which indicates that the transistor is driven into saturation. Again from these characteristics we see that for I_B = 0.175 mA, $V_{CE(sat)}$ = 250 mV and for I_B = 0.35 mA, $V_{CE(sat)}$= 125 mV. This variation explains that, the larger is the value of I_B, the smaller is the value of $V_{CE(sat)}$. At a given operating point, the ratio of $V_{CE(sat)}/I_C$ is called the saturation resistance R_{CS}. R_{CS} at the point Q is
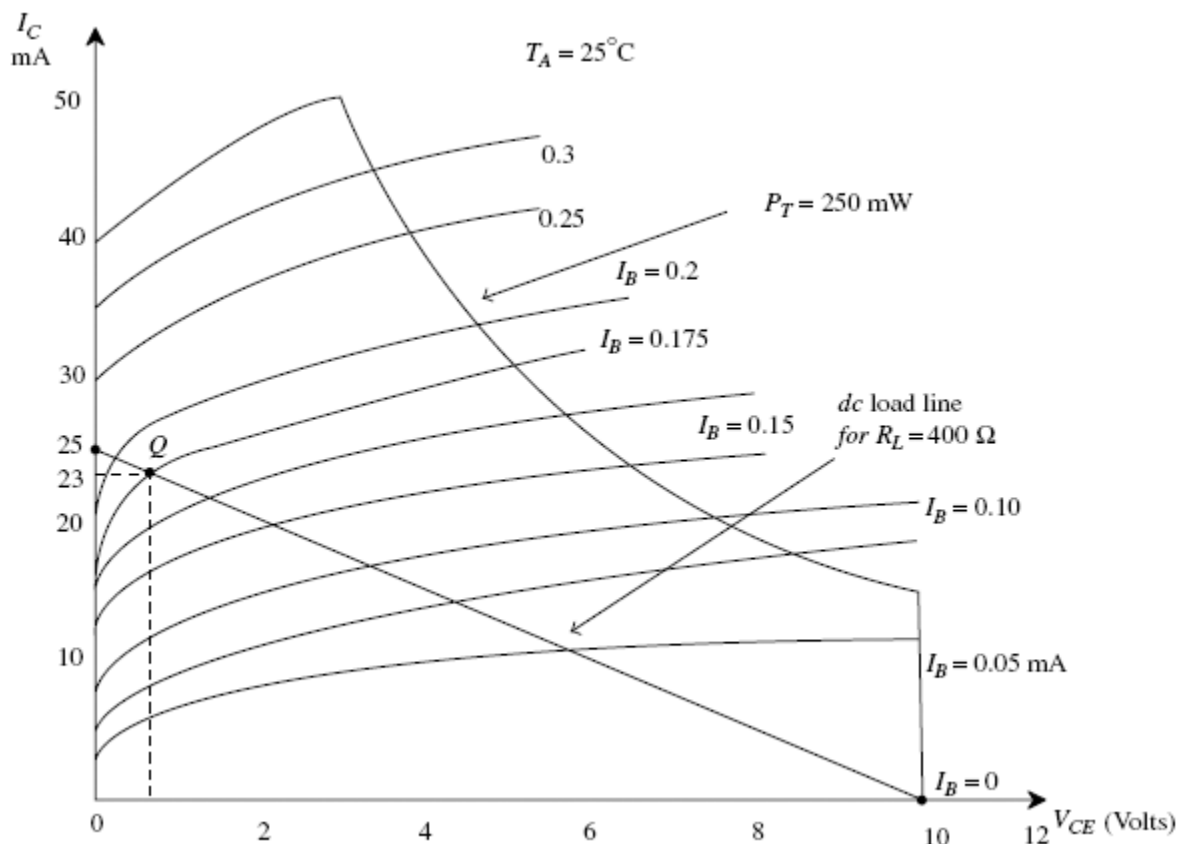
FIGURE 6.36 Typical output characteristics of an $n–p–n$ transistor in the CE mode

UNIT-IV - b

Sampling gates

INTRODUCTION

A sampling gate is a transmission circuit that faithfully transmits an input signal to the output for a finite time duration which is decided by an external signal, called a gating signal (normally rectangular in shape), as shown in <u>Fig. 11.1</u>.

The input appears without a distortion at the output, but is available for a time duration T and afterwards the signal is zero. They can transmit more number of signals. The main applications of

the sampling gates are: (i) multiplexers; (ii) choppers; (iii) D/A converter; (iv) sample and hold circuits, etc. Sampling gates can be of two types:

1. Unidirectional gates: These gates transmit the signals of only one polarity.
2. Bidirectional gates: These gates transmit bidirectional signals (i.e., positive and negative signals).

Earlier, we had seen logic gates in which the output, depending on the input conditions, is either a 1 level or a 0 level. That is, the inputs and outputs are discrete in nature. In a sampling gate, however, the output is a faithful replica of the input. Hence, sampling gates are also called linear gates, transmission gates or time selection circuits. Linear gates can use either a series switch, as shown in <u>Fig. 11.2(a)</u> or a shunt switch, as shown in <u>Fig. 11.2(b)</u>. In<u>Fig. 11.2(a)</u>, only when the switch closes, the input signal is transmitted to the output. In <u>Fig. 11.2(b)</u>, only when the switch is open the input is transmitted to the output.
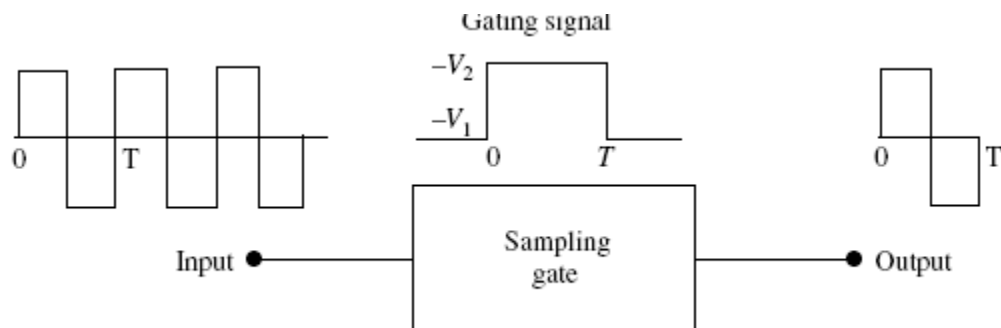
FIGURE 11.1 A sampling gate
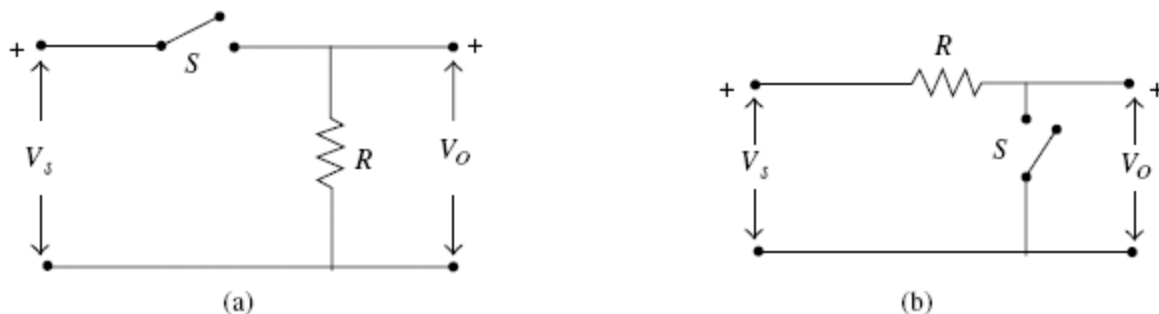
FIGURE 11.2 A linear gate (a) using a series switch; and (b) using a shunt switch

UNIDIRECTIONAL DIODE GATES

A unidirectional gate can transmit either positive or negative pulses (or signals) to the output. It means that this gate transmits pulses of only one polarity to the output. The signal to be

transmitted to the output is the input signal. This input signal is transmitted to the output only when the control signal enables the gate circuit. Therefore, we discuss two types of unidirectional diode gates, namely, unidirectional diode gates that transmit positive pulses and unidirectional diode gates that transmit negative pulses.

Unidirectional Diode Gates to Transmit Positive Pulses

In order to transmit positive pulses, the unidirectional gate shown in Fig. 11.3 can be used. The gating signal is also known as a control pulse, selector pulse or an enabling pulse. It is a negative signal, whose magnitude changes abruptly between $-V_2$ and $-V_1$.

Consider the instant at which the gating signal is $-V_1$, which is a reasonably large negative voltage. As a result, D is OFF. Even if a positive input pulse is present when the gating signal with value $-V_1$ is present, the diode D remains OFF since the input may not be sufficiently large to forward-bias it. Hence, the output is zero.

Now consider the duration when the gate signal has a value $-V_2$ (smaller negative value) and when the input is also present (coincidence occurs). Assume that the control signal has peak-to-peak swing of 25 V and the signal has peak-to-peak swing of 15 V.

1.   Let, for example, $-V_1 = -40$ V, $- V_2 = -15$ V and the signal amplitude be 15 V, as shown in Fig. 11.4(a). The net voltage at the anode of the diode, when the input is present for the duration of the gating signal, is 0. The diode is OFF and the output in this case is zero.
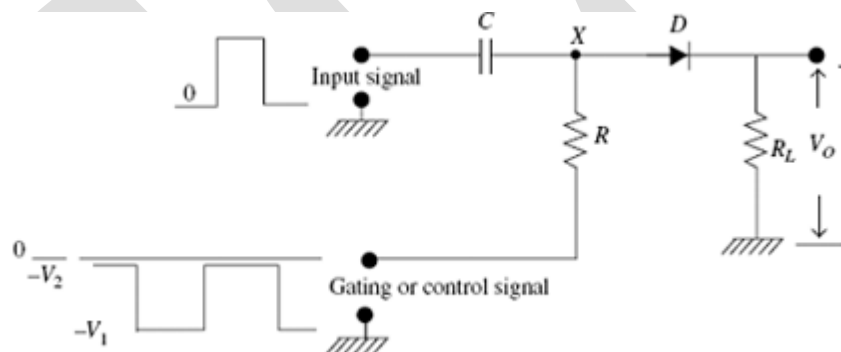
FIGURE 11.3 The unidirectional gate to transmit positive pulses
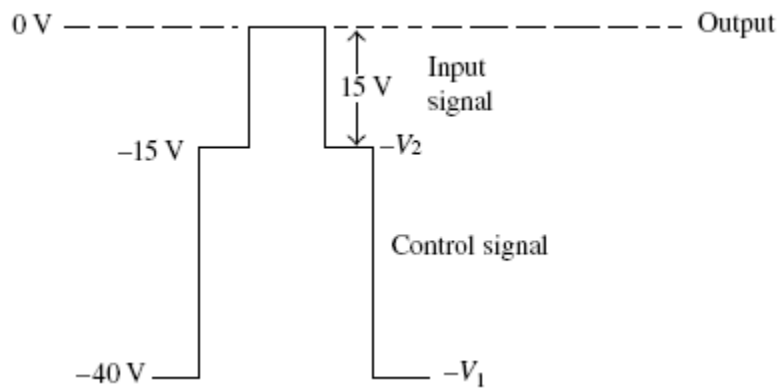
FIGURE 11.4(a) The control signal with $-V_1 = -40$ V, $-V_2 = -15$ V and the input amplitude 15 V

2. Now, change the levels to $-V_1 = -35$ V, $-V_2 = -10$ V and the signal amplitude remains constant at 15 V, as shown in Fig. 11.4(b). Only when the input forward-biases the diode, there is an output. The output in this case is a pulse of amplitude 5 V (assuming an ideal diode). The duration of the output is the same as the duration of the input signal.

3. Now let $-V_1 = -30$ V, $-V_2 = -5$ V and the signal amplitude be 15 V, as shown in Fig. 11.4(c). As the signal above the zero level is 10 V, the output is a pulse of amplitude 10 V and has the same duration as the input.

4. Let $-V_1 = -25$ V, $-V_2 = 0$ V and the signal amplitude be 15 V, as shown in Fig. 11.4(d). The output in this case is 15 V and has the same duration as the input.

5. Let $-V_2 = +5$ V and $-V_1 = -20$ V, as shown in Fig. 11.4(e). In this case, the output not only contains the input but also a portion of the control signal. The desired signal at the output is seen to be riding over a pedestal. We see that the output of the gate changes by adjusting $-V_2$ and in the last case it is seen that the output is superimposed on a pedestal of 5 V. Thus, the output is influenced by the control signal.
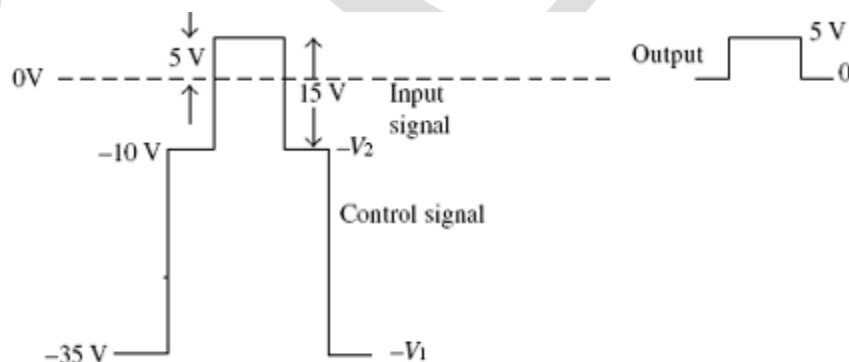
FIGURE 11.4(b) The control signal with $V_1 = -35$ V, $-V_2 = -10$ V and the input amplitude 15 V
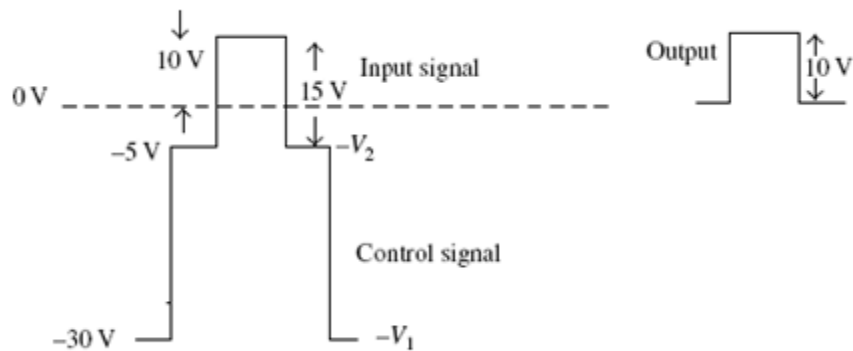
FIGURE 11.4(c) The control signal with $V_1 = -30$ V, $-V_2 = -5$ V and the input amplitude 15 V
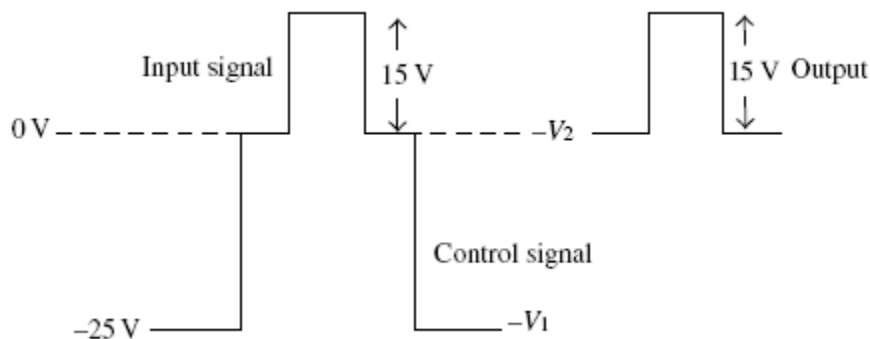
FIGURE 11.4(d) The control signal with $V_1 = -25$ V, $-V_2 = 0$ V and the input amplitude 15 V
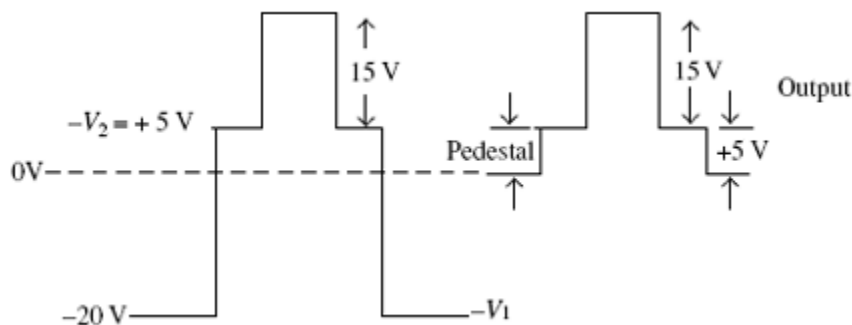
FIGURE 11.4(e) The control signal with $V_1 = -20$ V, $-V_2 = 5$ V and the input amplitude 15 V

For a gating signal, the RC network behaves as an integrator. Hence, the gate signal is not necessarily a rectangular pulse but rises and falls with a time constant RC. As a result, there is a distortion in the gate signal. However, if the duration of the input signal (a pulse) is much smaller than the duration of the gate, this distortion associated with the gating signal is not necessarily

transmitted to the output; and the output is a sharp pulse as desired, provided the pedestal is eliminated, as shown in Fig. 11.4(f). On the contrary, if there is a pedestal, there is a corresponding distortion in the output, as shown in Fig. 11.4(g).

The advantages of unidirectional diode gates are: (i) they are simple to implement; (ii) have a negligible transmission delay; (iii) the gate draws no current in the quiescent condition; and (iv) by the proper modification of the circuit, more than one input signal can be transmitted through the gate circuit. However, there are two disadvantages of this arrangement. As the control signal and the input signal are directly connected at X (see Fig. 11.3), there could be an interaction between these two sources. The time constant RC, if properly not chosen, can cause the distortion of the gate signal. A two-input unidirectional diode gate is shown in Fig. 11.5(a).
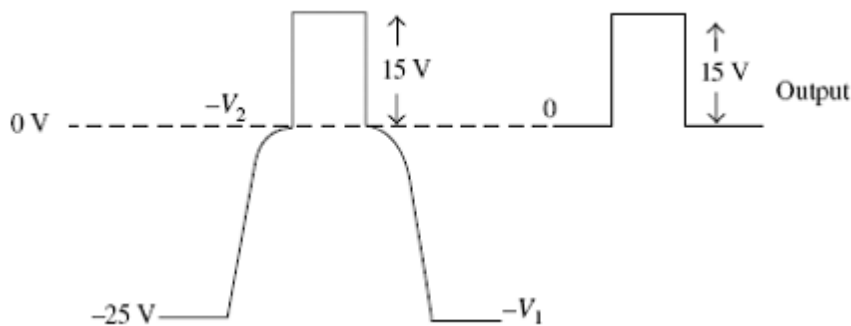
FIGURE 11.4(f) There is no distortion in the output though the control signal is distorted
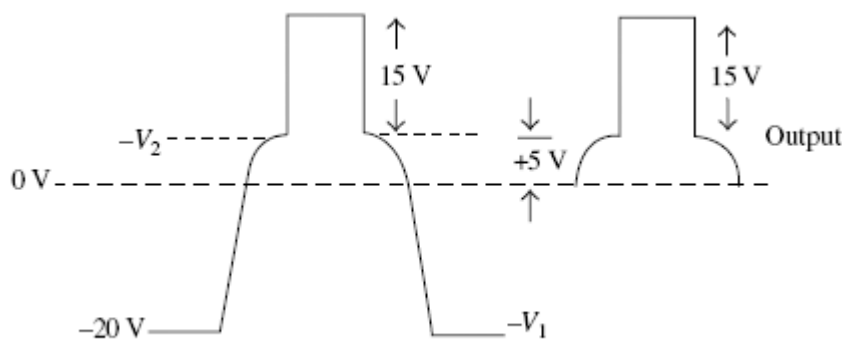
FIGURE 11.4(g) The distorted gate signal giving rise to a distorted pedestal

Let V_{s1} and V_{s2} be the pulses of amplitude 5 V. When both these signals appear at the input simultaneously, having the same duration, the output is shown in Fig. 11.5(b), when $-V_1 = -25$ V and $-V_2 = 0$.

When the control signal is at $-V_2$ (= 0 V), and if both the inputs are 0 the output is zero. When the inputs are above 0, the output is 5 V. However, when the control input is at $-V_1$ (−25 V), no output is available. This negative control signal inhibits the gate. Hence, this circuit is a two-input OR gate with $-V_1$ (−25 V) and inhibiting the gate operation. The waveforms shown in Fig. 11.5(b) suggest that time division multiplexing can be employed to simultaneously transmit a number of signals. The limitation of this arrangement is that signal sources may load the control input. To overcome this disadvantage, an arrangement in which the signal sources avoid loading the control input is suggested in Fig. 11.6. Here, the input signals are connected to point X through diodes D_1 and D_2 whereas the control source is connected at X directly to avoid interference and loading.
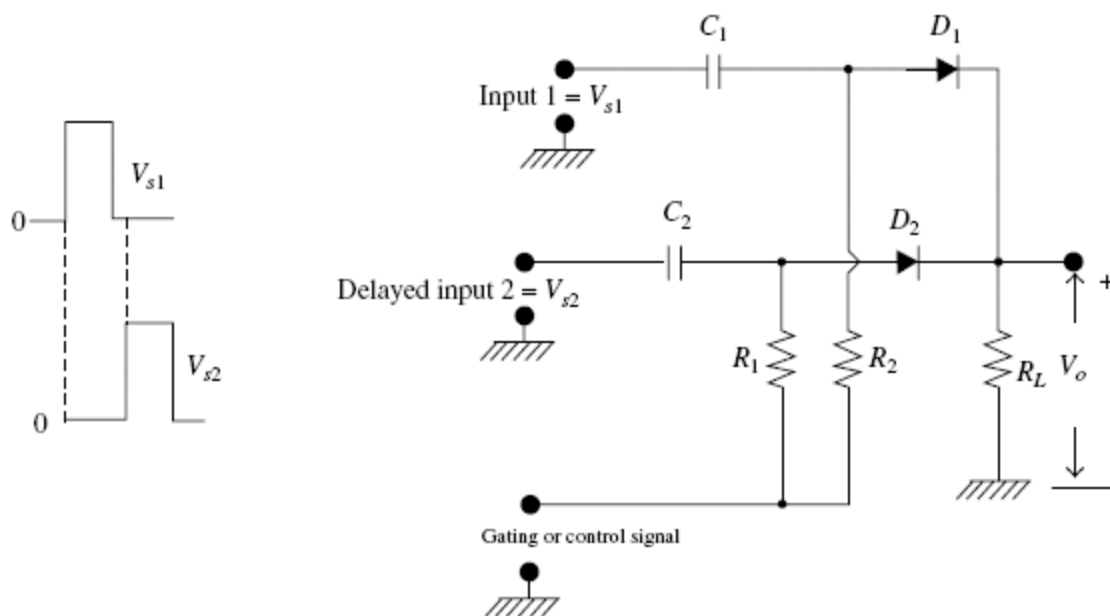
FIGURE 11.5(a) A unidirectional two-input diode gate
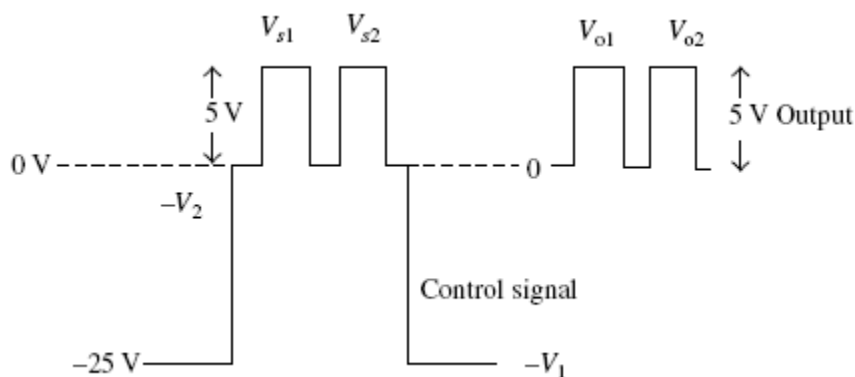
FIGURE 11.5(b) The waveforms of a two-input unidirectional gate
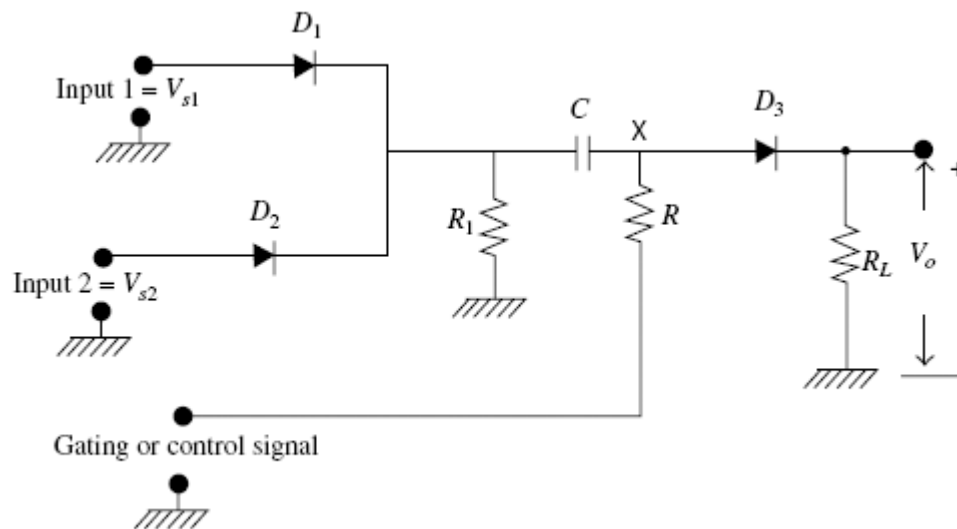
FIGURE 11.6 A two-input diode gate that avoids loading on the control signal

Unidirectional Diode Gates

1.   **A unidirectional diode coincidence gate (AND gate)**: In certain applications, it may become necessary that the input be transmitted to the output only when a set of conditions are simultaneously satisfied. In such cases, a coincidence gate is employed. A unidirectional diode coincidence (AND) gate is shown in Fig. 11.7(a).

When any of the control voltages is at $-V_1(-25\text{ V})$, point X is at a larger negative voltage, even if the input pulse V_s (15 V) is present. D_o is reverse-biased. Hence, there is no signal at the output.
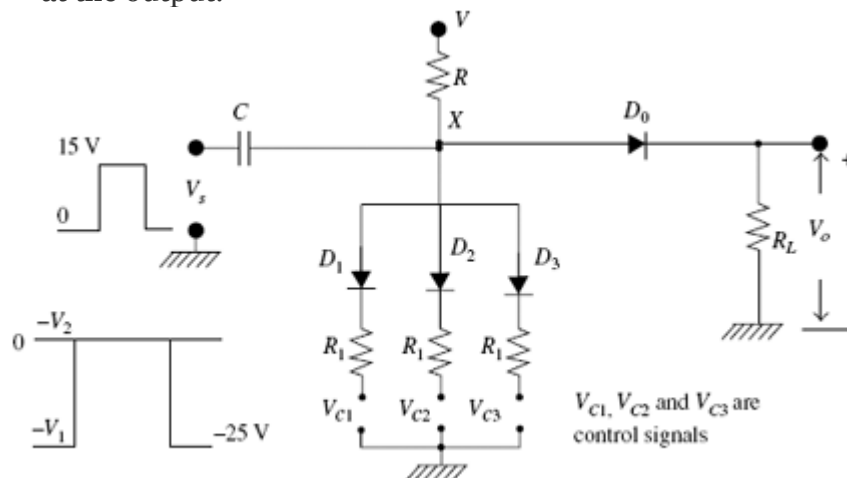
FIGURE 11.7(a) A unidirectional diode AND gate with multiple control signals

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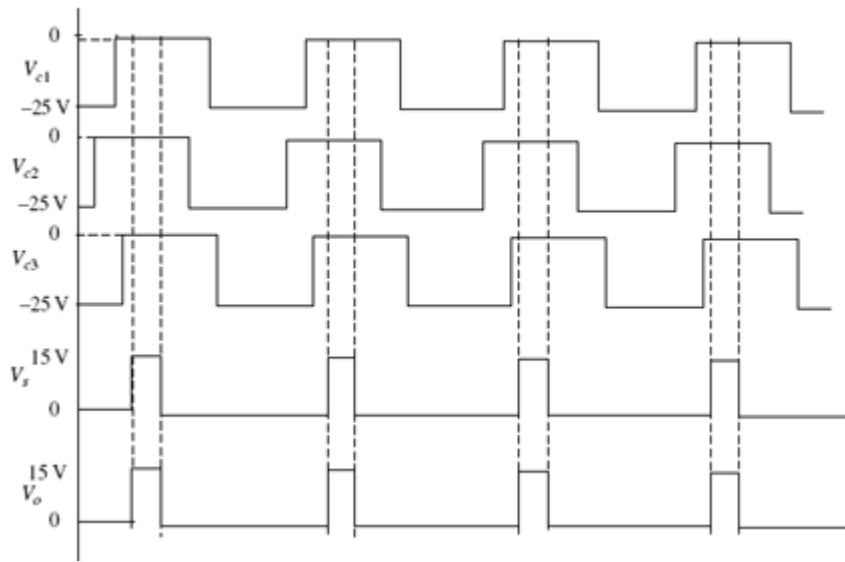
FIGURE 11.7(b) The waveforms of the coincidence (AND) gate

When all the control voltages, on the other hand, are at $-V_2$ (0 V), if an input signal V_s(15 V) is present, D_0 is forward-biased and the output is a pulse of 15 V. Thus, only when all the control signals are at 0 V (1 level) and if an input signal is present, then it is transmitted to the output. Hence, this circuit is a coincidence circuit or AND circuit, as shown in Fig. 11.7(b).

2. **A unidirectional diode OR gate:** Consider the gate circuit shown in Fig. 11.8(a). Let the control voltages vary from −50 V to 0 V. If any control signal V_C (say V_{C1}) is at 0 V, D_1 conducts and behaves as a short circuit. Then the resultant circuit is shown in Fig. 11.8(b). If R_s is 1 kΩ and if I is specified as 1 mA then R = 149 kΩ. The voltage at X is now at −1 V.

Hence, D_0 is reverse-biased and is an open circuit; and so the output is zero. Now, if a pulse V_s (= 10 V) is applied at the input, D_0 is forward-biased and D_1 and D_2 are reverse-biased. The output is 10 V.
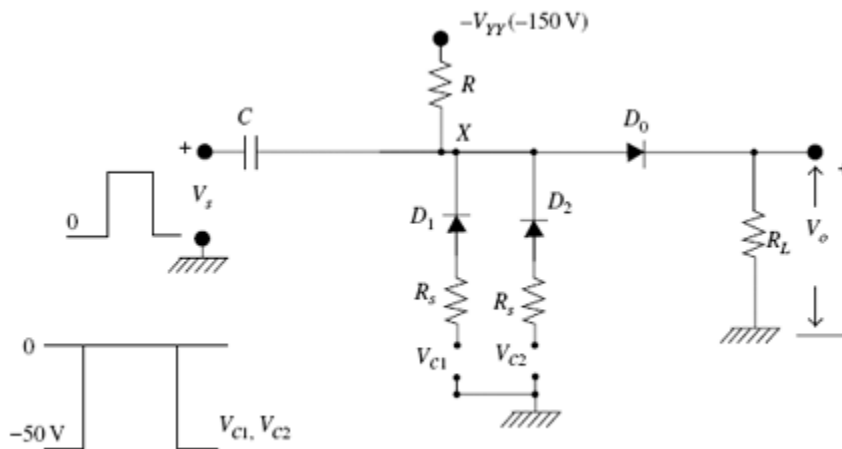
FIGURE 11.8(a) An OR sampling gate
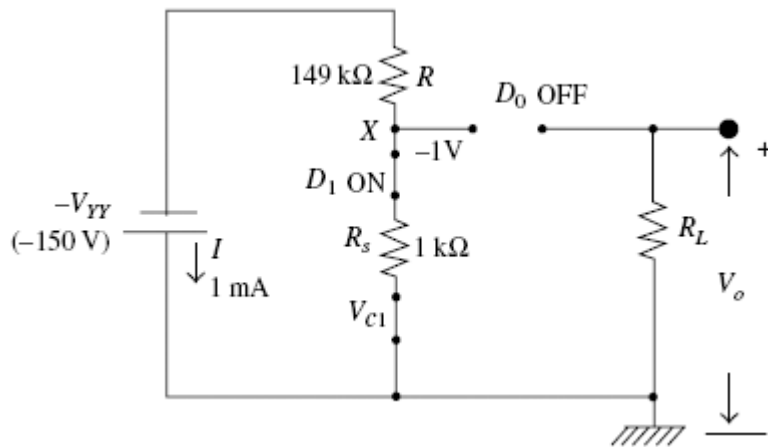
FIGURE 11.8(b) The circuit of Fig. 11.8(a) when any of the control signals and inputs is zero

Thus, the circuit shown in Fig. 11.8(a) is a gate that transmits the input signals to the output when any one of the control inputs is 0 V (1 level). This circuit is an OR circuit. The waveforms are shown in Fig. 11.8(c). The truth table, given in Table. 11.1 with control signals as logical inputs, verifies the OR operation. We see from the waveforms shown in Fig. 11.8(c) and Table.11.1 that the output is 0 V (0 level) for input pulses 4 and 8, for which both the control signals are −50 V (0 level).

3.   **Unidirectional diode gate that eliminates pedestal**: In the unidirectional gates discussed till now, if the upper level of the gating signal $(-V_2)$ is exactly zero volts, the gate is enabled and an input is faithfully transmitted to the gate output terminals. The output can also be derived if $−V_2$ is a positive voltage (say 5 V). In this case, the output will have a pedestal and the signal is superimposed on it. To ensure that the output is a faithful replica of the input even if the upper level of the control signal is positive (i.e., to eliminate pedestal), the circuit shown in Fig. 11.9(a) is employed.

1.   If the input V_s is zero and if the enabling control signal is not present, D_1 conducts and the negative voltage at X reverse-biases D_0 and $V_0 = 0$, shown in Fig. 11.9(b).

TABLE 11.1 The truth table of the OR gate with control signals as logical inputs

Input pulse number	State of V_{C1}	State of V_{C2}	Output V_o
1	0 V (1 level)	0 V (1 level)	10 V (1 level)
2	−50 V (0)	0 V (1)	10 V (1)
3	0 V (1)	−50 V (0)	10 V (1)
4	−50 V (0)	−50 V (0)	0 V (0)
5	0 V (1)	0 V (1)	10 V (1)
6	−50 V (0)	0 V (1)	10 V (1)
7	0 V (1)	−50 V (0)	10 V (1)
8	−50 V (0)	−50 V (0)	0 V (0)
9	0 V (1)	0 V (1)	10 V (1)
10	−50 V (0)	0 V (1)	10 V (1)
11	0 V (1)	−50 V (0)	10 V (1)
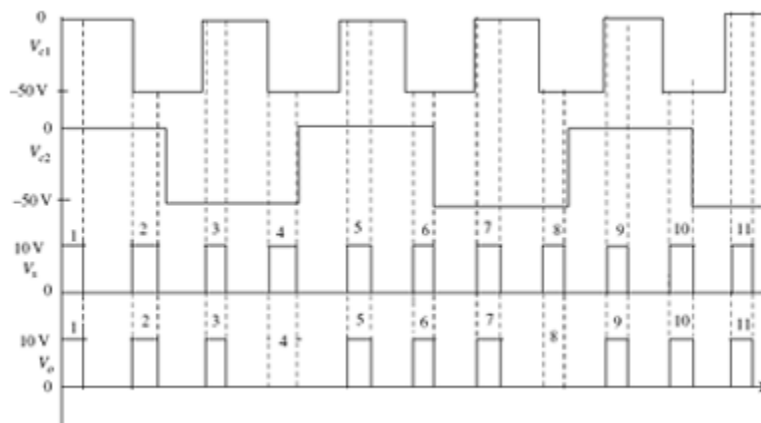
FIGURE 11.8(c) The waveforms of the OR gate shown in <u>Fig. 11.8(a)</u>.
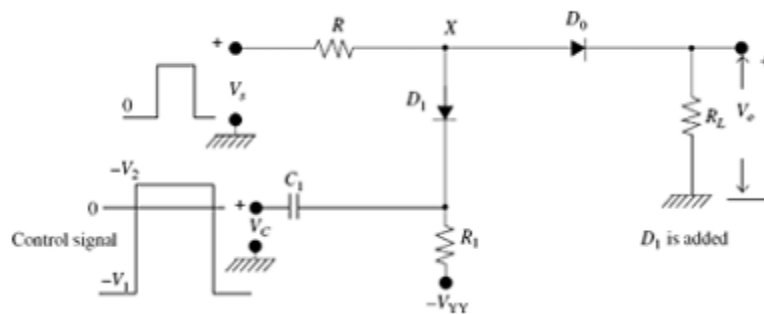
FIGURE 11.9(a) A sampling gate that is insensitive to the upper level $(-V_2)$ of the control signal
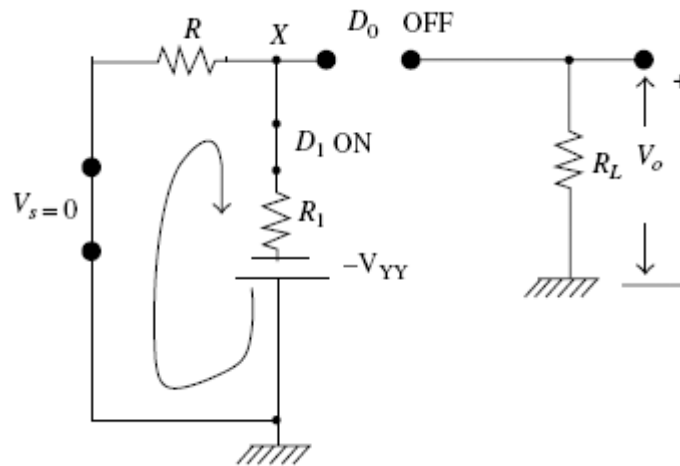
FIGURE 11.9(b) The circuit of Fig. 11.9(a) when $V_s = 0$ and the control signal is absent
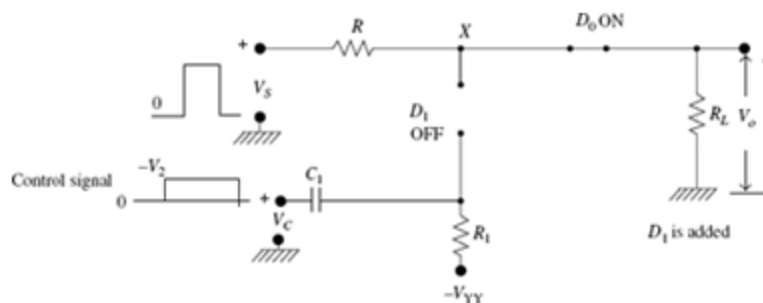
FIGURE 11.9(c) The circuit when the control signal is positive and the input is present

2.   If the control voltage is now positive, D_1 is reverse-biased and is OFF, as shown in Fig. 11.9(c). An input signal V_s (a positive pulse) ensures conduction of D_o and hence, the input signal is present at the output for the duration of the control signal. There is no pedestal in the output even though the control signal has a positive voltage as its upper level.

A Unidirectional Diode Gate to Transmit Negative Pulses

A unidirectional diode gate is shown in Fig. 11.3, to transmit the positive pulses when the gating signal is present. Similarly, a unidirectional diode gate to transmit negative pulses can be constructed as shown in Fig. 11.10. The difference between these two gates is that the input signals are negative pulses and the gating signal varies between V_1 and V_2 as shown in Fig. 11.10 and the diode is connected in the opposite direction.

When the gating signal is at V_1, the voltage at X is a large positive voltage as a result D is reverse-biased. If an input signal is now present until the magnitude of the input is more negative than the

positive voltage at X, the diode will not conduct, i.e., for the diode to conduct and thus transmit the signal to the output, the input is required to have a large negative value. Even if the diode conducts only the peak of the input will be transmitted to the output, but not the entire input signal. On the other hand, when the amplitude of the gating signal is V_2, a small positive voltage, if a negative pulse is present at the input it can make the diode conduct. As such the output is present when the gating signal is at V_2.

BIDIRECTIONAL SAMPLING GATES

Till now we have considered gates that pass only unidirectional signals. Bidirectional sampling gates transmit both positive and negative signals. These gates can be derived using diodes, BJTs, FETs, etc. We are going to consider some variations of the bidirectional gates.
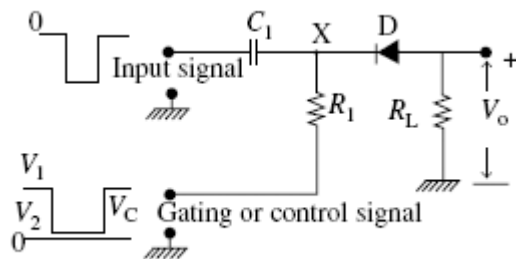
FIGURE 11.10 The unidirectional diode gate to transmit negative pulses

SINGLE-TRANSISTOR BIDIRECTIONAL SAMPLING GATES

A bidirectional sampling gate using a single transistor is shown in Fig. 11.11. The control signal and the input are applied to the base of Q. The control signal is a pulse whose amplitude varies between V_1 and V_2 and has a duration t_p sufficient enough for a signal transmission. As long as V_C is at the lower level V_1, Q is OFF and at the output we only have a dc voltage V_{CC}. However, when V_C is at its upper level V_2, Q is ON for the duration t_p and if the input signal is present during this period, it is amplified and transmitted to the output with phase inversion but referenced to a dc voltage V_{dc}. At the end of t_p, Q is again OFF and the dc voltage at its collector jumps to V_{CC}. Thus, the signal is transmitted when the gating signal is at V_2. However, the output contains a pedestal.
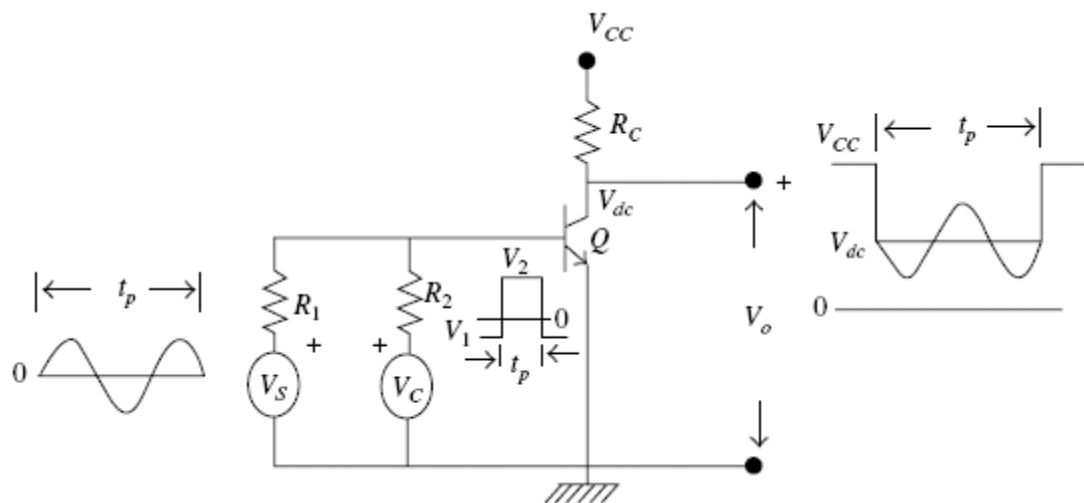
FIGURE 11.11 A bidirectional transistor gate

Two-transistor Bidirectional Sampling Gates

The <u>Fig. 11.12(a)</u> shows another bidirectional transistor gate where two devices Q_1 and Q_2 are used and the control signal and the input signal are connected to the two separate bases.

There is no external dc voltage connected to the base of Q_1, only the gating signal V_C is connected. Let the control voltage be at its upper level, V_2. Then, Q_1 is ON and there is sufficient emitter current I_{E1} which results in V_{EN1} across R_E. Q_2 is biased to operate in the active region using R_1 and R_2. The voltage at the base of Q_2 with respect to its emitter (V_{BE2}) is ($V_{BN2} - V_{EN1}$). If this voltage is sufficient enough to reverse-bias the base emitter diode of Q_2, then Q_2 is OFF. There is no output signal, but only a dc voltage V_{CC} is available. However, when the gating signal is at its lower level V_1, Q_1 is OFF and Q_2 operates in the active region and can also operate as an amplifier. If an input signal is present, there is an amplified output V_o. The presence of R_E increases the input resistance R_i and thus, the signal source is not loaded.

From the waveforms shown in <u>Fig. 11.12(b)</u> it is seen that the output is V_{CC} when Q_2 is OFF. When the gating signal drives Q_1 OFF and Q_2 ON, the dc voltage at the collector of Q_2 falls to V_{dc} (a voltage much smaller than V_{CC}). During the period of the gating signal, the input signal is amplified and phase inverted by Q_2 and is available at the output. Again at the end of the gating signal Q_2 goes OFF and V_o jumps to V_{CC}. Hence, the signal is superimposed on a pedestal.
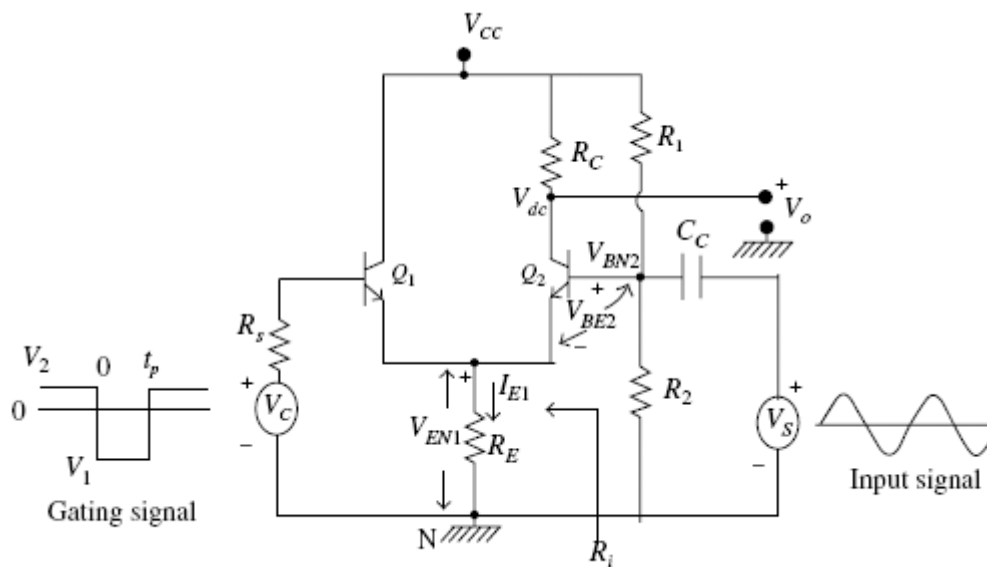
FIGURE 11.12(a) A bidirectional transistor gate
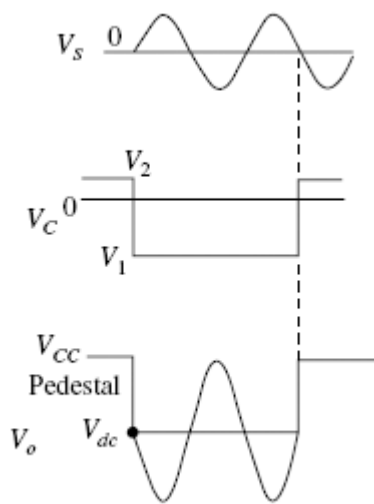
FIGURE 11.12(b) The waveforms

11.3.3 A Two-transistor Bidirectional Sampling Gate that Reduces the Pedestal

A circuit arrangement that reduces the pedestal is shown in <u>Fig. 11.13</u>. The control signals applied to the bases of Q_1 and Q_2 may have the same amplitude but are of a opposite polarity. When the gating signal is connected to Q_1 at $T = 0-$, it is negative (at level V_1). The net voltage at the base of Q_1 is $- (V_{BB_1} + V_1)$. Therefore, Q_1 is OFF. At the same time the gating signal connected to Q_2 is positive and is   . The net voltage at the base of Q_2 is ($- V_{BB_2}$) and is positive and therefore, drives Q_2 ON. Q_2 draws a collector current I_C. As a result, there is a dc voltage V_{dc} at its collector and $V_o = V_{dc}$. However, when the gating voltage at the base of Q_1 drives Q_1 ON and into the active

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region, at $t = 0+$, Q_2 goes OFF as the gating signal is   . During this period when Q_1 is ON, if the input signal is present, it is amplified and is available at the output, with phase inversion. The bias voltages V_{BB1} and V_{BB2} are adjusted such that the quiescent current in Q_1 and Q_2 when ON is the same ($= I_C$) and consequently the quiescent dc voltage at the output is V_{dc}. Therefore, the dc reference level practically is V_{dc}. At the end of the time period t_p, Q_1 once again goes into the OFF state and Q_2 into the ON state and the dc voltage at the output is V_{dc}. As such the pedestal can be eliminated. However, our assumption is that the gating signals are ideal pulses (with zero rise time). In this case, the instant Q_1 switches ON, Q_2 switches OFF, as shown in <u>Fig. 11.14(a)</u>. However, in practice the gating signals may not be ideal pulses but have a finite rise time and fall time; these may then give rise to spikes in the output shown in <u>Fig. 11.14(b)</u>.

Let V_{BE} be the voltage between the base and emitter terminals of a transistor when the device is in the active region. If the gating pulse is at its lower level (, negative), the net voltage as we have seen at the base of Q_2 is far below the cut-off. As a result, Q_2 goes OFF at $t = t_2$. At the same instant, Q_1 is required to go into the ON state, as the gating signal at its base is positive. However, because of the finite rise time associated with the gating signal at the base of Q_1, it may not necessarily go into the ON state at the instant Q_2 has gone into the OFF state(t_2) and may go into the ON state at $t = t_1$. The result is that the output is nearly V_{CC} during the interval t_2 to t_1. This voltage, however, falls to V_{dc} when eventually Q_1 is ON. A spike is developed at the output. Similarly, at the end of the gating signal Q_1 goes OFF (at $t = t_4$) before Q_2 goes ON (at $t = t_3$). Another spike develops at the output. It is seen that the gating signals themselves give rise to spikes in the output. If the rise time of the gating signal is large, these spikes are of larger duration as shown in <u>Fig. 11.14(b)</u>, where as if the rise time of the gating signal is small, these output spikes are of smaller duration as shown in <u>Fig. 11.15</u>. If the rise time of the gating signal is small when compared to the duration of the gating signal, even though the spikes may occur in the output, as the duration of the signal is smaller than the spacing between the spikes, these spikes will not cause any distortion of the signal and hence, are not objectionable, as shown in <u>Fig. 11.15</u>.
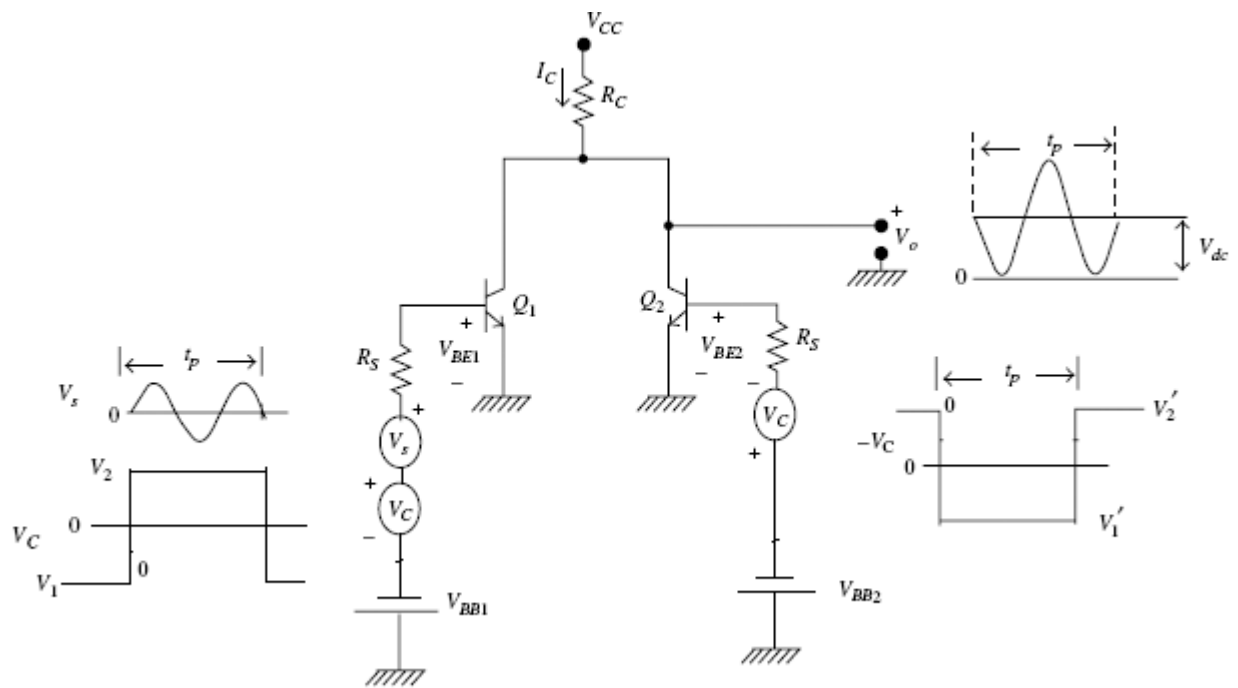
FIGURE 11.13 Circuit that reduces the pedestal
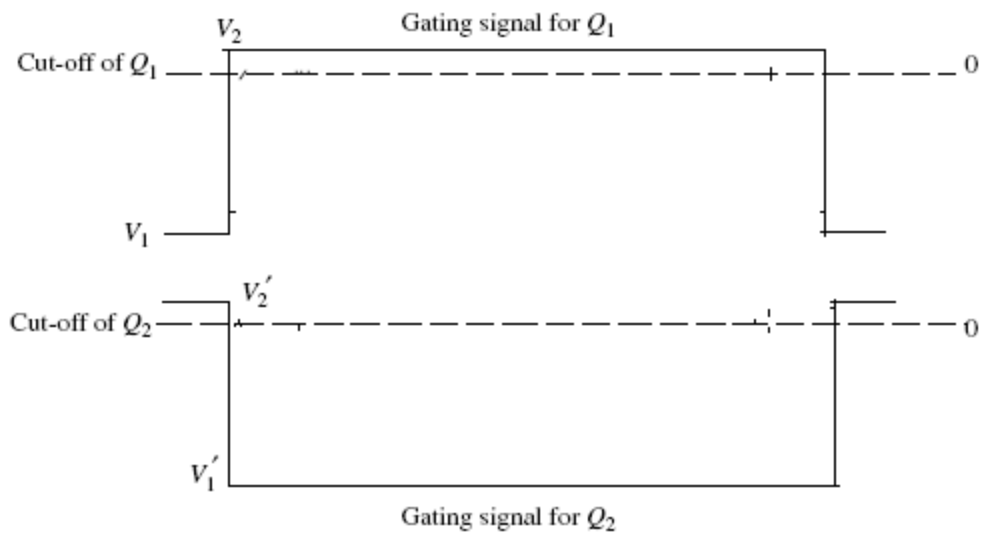
FIGURE 11.14(a) There are no spikes in the output when the gating signals are ideal
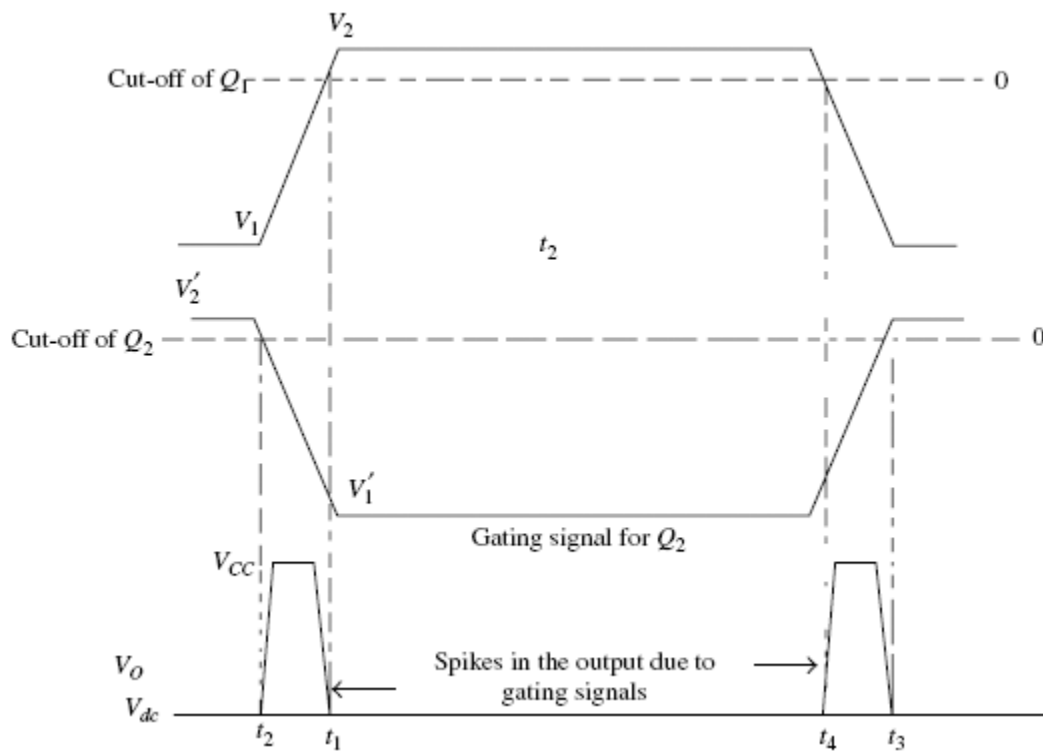
FIGURE 11.14(b) The spikes of a longer duration if the rise time of the gating signal is large

A Two-diode Bridge Type Bidirectional Sampling Gate that Eliminates the Pedestal

A bidirectional diode gate that eliminates the pedestal is shown in <u>Fig. 11.16(a)</u>. R_1, R_1, D_1 and D_2 form the four arms of the bridge. When the control signals are at V_1, D_1 and D_2 are OFF and no input signal is transmitted to the output. However, when the control signals are at V_2, diode D_1 conducts if the input (= V_s) are positive pulses and diode D_2 conducts if the input are negative pulses. Hence, these bidirectional inputs are transmitted to the output. This arrangement because of the circuit symmetry eliminates a pedestal. Consider one half of the circuit that transmits the positive pulses to the output when D_1 conducts (because of symmetry), as shown in <u>Fig. 11.16(b)</u>.
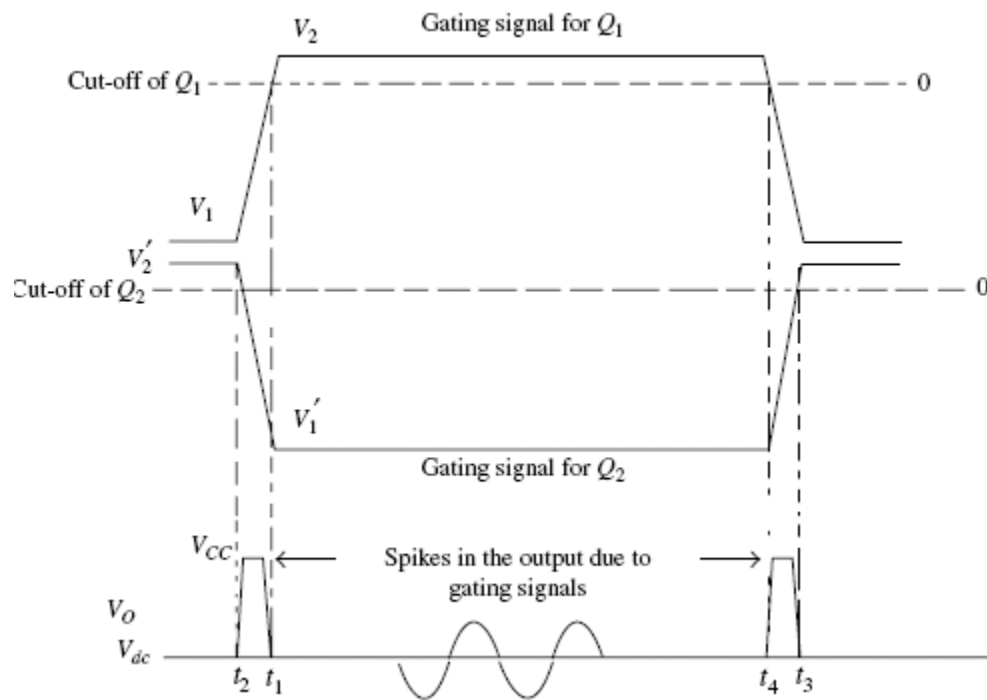
FIGURE 11.15 The spikes of relatively smaller duration when the rise time of the gating signals is small

Thévinizing the circuit shown in Fig. 11.16(b) at node A, the Thévenin voltage source magnitude due to V_s (shorting V_C source, considering one source at a time) and its internal resistance are calculated using the circuit shown in Fig. 11.16(c).
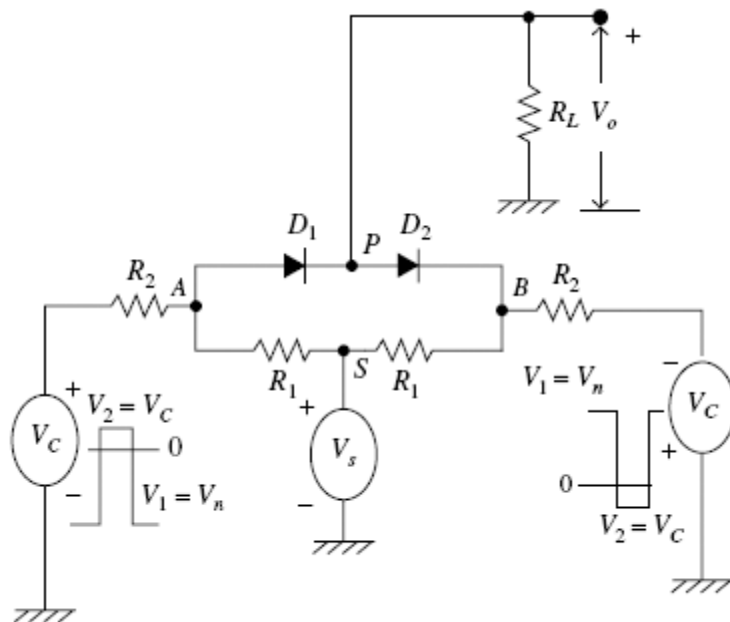
FIGURE 11.16(a) A bidirectional gate in the form of a bridge circuit

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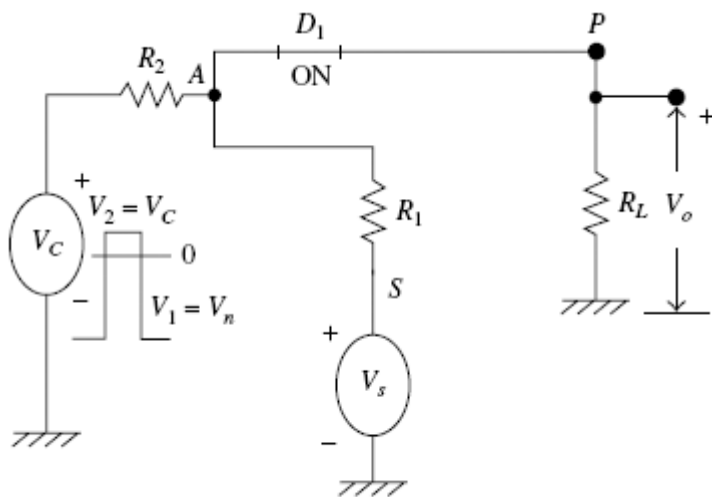
FIGURE 11.16(b) The circuit that transmits the positive pulses to the output
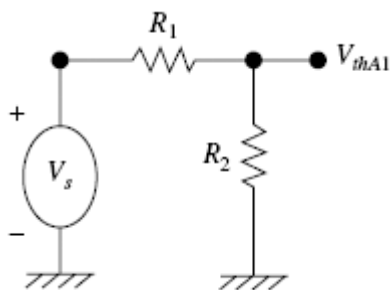
FIGURE 11.16(c) The equivalent circuit to calculate voltage at node A due to V_s source
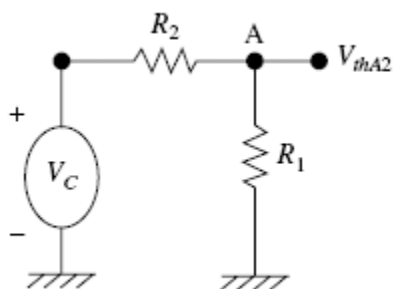
FIGURE 11.16(d) The equivalent circuit to calculate voltage at node A due V_C source

$$V_{thA1} = \frac{R_2}{R_1 + R_2} V_s = \alpha V_s$$

where $\alpha = \dfrac{R_2}{R_1 + R_2}$ and $R_{th1} = R_1 \parallel R_2 = \dfrac{R_1 R_2}{R_1 + R_2}$

Similarly, Thevenizing the circuit shown in Fig. 11.16(b) at node A, the Thévenin source due to V_C is (shorting V_s), shown in Fig. 11.16(d).

$$V_{thA2} = \frac{R_1}{R_1 + R_2} V_C \quad R_{th2} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{thA2} = \frac{R_1}{R_1 + R_2} V_C \quad = \left(1 - \frac{R_2}{R_1 + R_2}\right) V_C = (1 - \alpha) V_C$$

We have $R_{th1} = R_{th2}$.

Redrawing the circuit shown in Fig. 11.16(b) and replacing the diode by its linear model (a battery of value V_γ in series with R_f, the forward resistance of the diode), results in the circuit shown in Fig. 11.16(e).

Similarly, considering the circuit when a negative signal is transmitted to the output when D_2 is ON and combining the equivalent circuits of the two halves, we finally have the circuit shown in Fig. 11.16(f).

$$R_3 = R + R_f, \text{ where } R = R_{th1} = R_{th2}$$
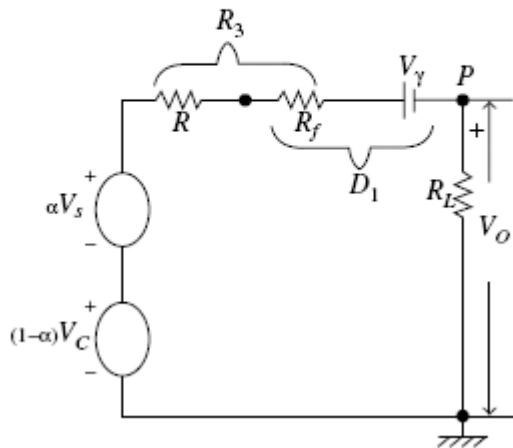
FIGURE 11.16(e) The equivalent circuit of the circuit shown in Fig. 11.16(b)

R_f is the diode forward resistance
V_γ is its cut-in voltage

We shall now define the gain of the transmission gate A (strictly speaking this is attenuation) as the ratio of V_o/V_s during transmission period. The control and small diode voltages do not contribute to any current in R_L, the resultant simplified circuit is shown in Fig. 11.16(g). The open circuit voltage between P and the ground is αV_s and the Thévenin resistance is $R_3/2$, as shown in Fig. 11.16(h).

$$V_o = \alpha V_s \frac{R_L}{R_L + \dfrac{R_3}{2}} \qquad A = \frac{V_o}{V_s} = \alpha \frac{R_L}{R_L + \dfrac{R_3}{2}}$$

But

$$\alpha = \frac{R_2}{R_1 + R_2}$$
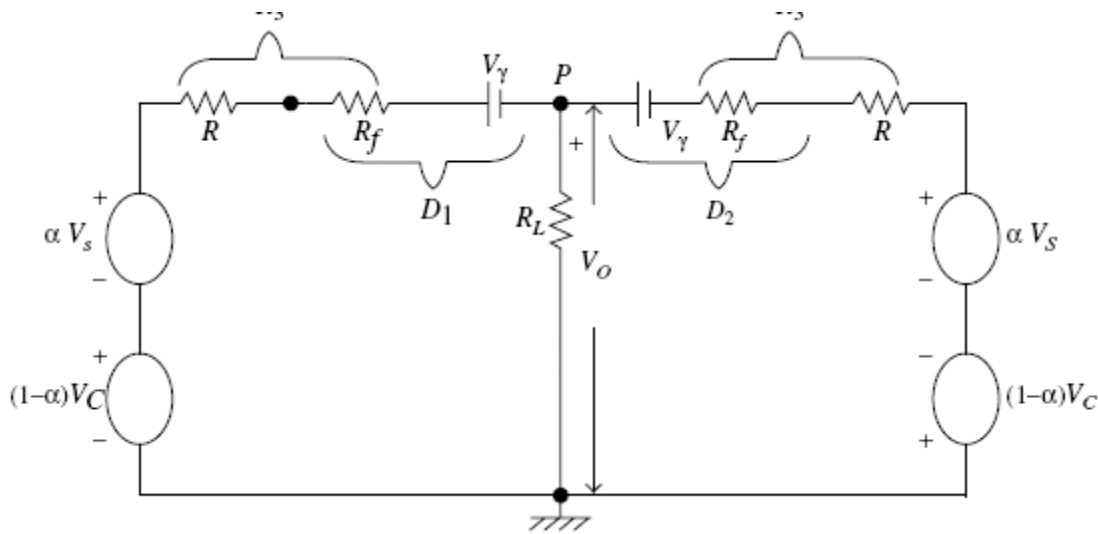
FIGURE 11.16(f) The equivalent circuit of Fig. 11.16(a)

R_f is the diode forward resistance
V_γ is its cut-in voltage
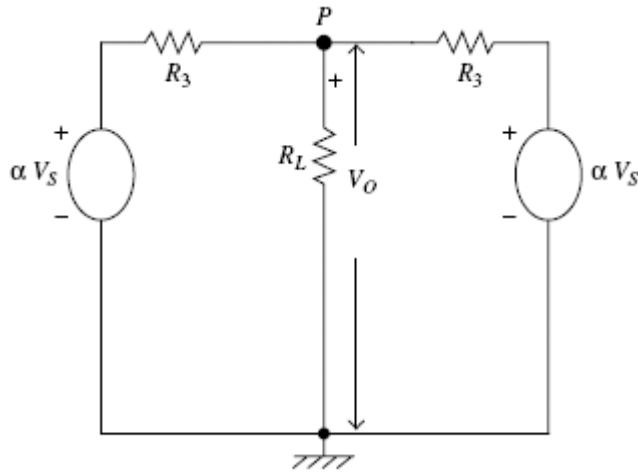
FIGURE 11.16(g) The simplified circuit of Fig. 11.16(f)
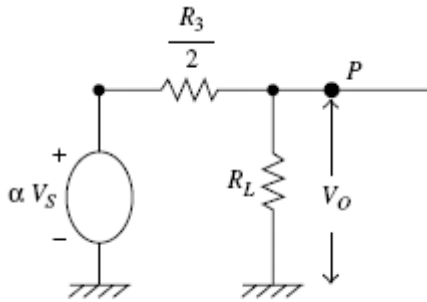
FIGURE 11.16(h) The circuit that enables the calculation of gain A

Therefore,

$$A = \frac{R_2}{R_1 + R_2} \times \frac{R_L}{R_L + \dfrac{R_3}{2}} \tag{11.1}$$

a) **Minimum control voltage V_C(min) required to keep both the diodes D_1 and D_2 ON:** Let only the gating signals be present. The amplitude and polarity of the gating signals are such that both the diodes D_1 and D_2 conduct, and equal currents flow in these two diodes. When these equal and opposite currents flow in R_L, the net voltage drop is zero and there is no pedestal.

Let V_s be a positive signal. As the amplitude of the signal goes on increasing, the current in D_1 goes on increasing and that in D_2 goes on decreasing. As V_s increases further, the current in D_2 becomes zero (i.e., D_2 is OFF). Thus, there is a minimum control voltage V_C that will keep both the diodes

ON. To calculate this $V_{C(\min)}$, let it be assumed that D_2 has just stopped conducting i.e., the diode current has become zero; the drop across R_3 is zero. Therefore, the output voltage across R_L is the open circuit voltage, as shown in Fig. 11.17(a).
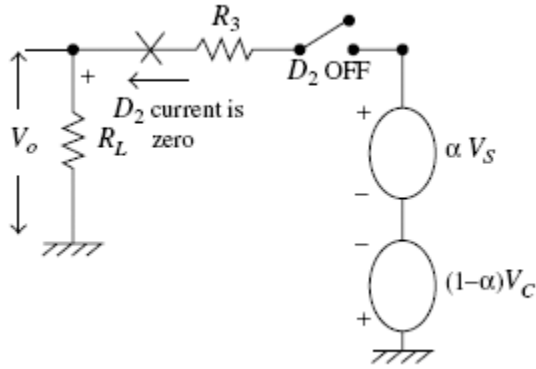
FIGURE 11.17(a) The voltage V_o when D_2 is OFF
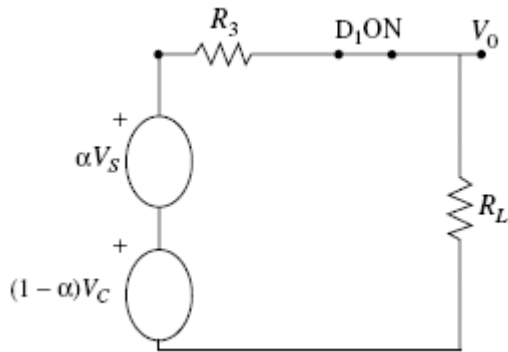
FIGURE 11.17(b) The voltage V_o when D_1 is ON

Now, calculating the output due to the left hand side signal source V_s and control signal $(1 - \alpha)V_C$, with the assumption that $V_\gamma \ll V_s$ (i.e., $V_r \approx 0$), as shown Fig. 11.17(b).

$$V_o = [\alpha V_s + (1 - \alpha)V_C]\frac{R_L}{R_L + R_3} \qquad (11.3)$$

Eqs. (11.2) and (11.3) represent V_o hence,

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$$[\alpha V_s + (1-\alpha)V_C]\frac{R_L}{R_L + R_3} = \alpha V_s - (1-\alpha)V_C$$

$$\alpha V_s\left(1 - \frac{R_L}{R_L + R_3}\right) = (1-\alpha)V_C\left(\frac{R_L}{R_L + R_3} + 1\right) \qquad \alpha V_s\left(\frac{R_3}{R_L + R_3}\right) = (1-\alpha)V_C\left(\frac{R_3 + 2R_L}{R_L + R_3}\right)$$

$$\alpha V_s R_3 = (1-\alpha)V_C(R_3 + 2R_L)$$

$$\alpha = \frac{R_2}{R_1 + R_2} \text{ and } 1 - \alpha = 1 - \frac{R_2}{R_1 + R_2} = \frac{R_1}{R_1 + R_2}$$

$$\frac{R_2 R_3}{R_1 + R_2}V_s = \frac{R_1}{R_1 + R_2}(R_3 + 2R_L)V_C$$

$$V_{C(min)} = \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L}V_s \qquad\qquad\qquad (11.4)$$

$V_{C(min)}$ decreases with increasing R_L.

b) **Minimum control voltage V$_n$(min) to ensure that D$_1$ and D$_2$ are reverse-biased:** We have calculated the minimum control voltage $V_{C(min)}$ i.e., needed to keep both the diodes, D_1 and D_2 ON. Similarly we calculate the minimum control voltage $V_{n(min)}$ i.e., required to keep D_1 and D_2 OFF when no transmission takes place. If both the diodes are reverse-biased, the output voltage at point P is zero and P is at the ground potential, shown in <u>Fig. 11.18(a)</u>. As D_1 is reverse-biased, it behaves as an open circuit. As a result, the input appears at the output.
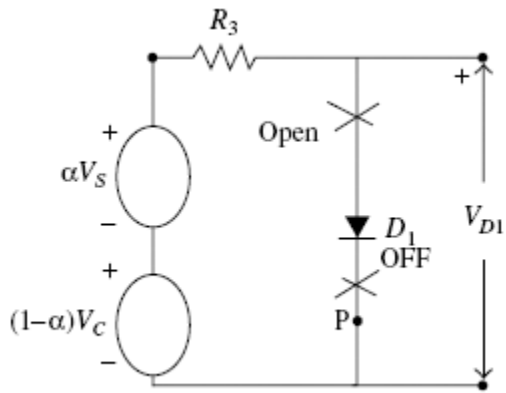
FIGURE 11.18(a) The gate circuit when D_1 and D_2 are reverse-biased
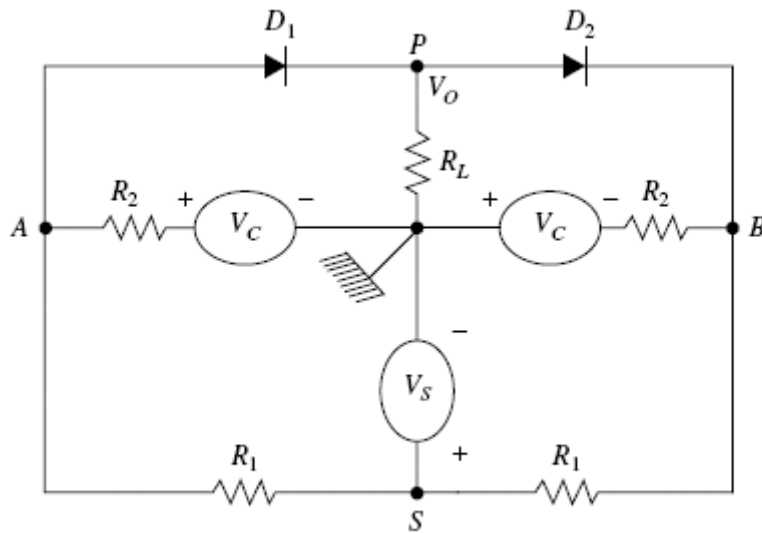
FIGURE 11.19(a) The bidirectional gate redrawn in the form of a bridge

V_{D1} = Voltage across D_1 = $[\alpha V_s + (1 - \alpha)V_C]$

If V_n is the magnitude of V_C at the lower level,

$V_{D1} = [\alpha V_s + (1 - \alpha)V_n]$

For D_1 to be OFF, V_{D1} must be either zero or negative. If V_{D1} is zero,

$$[\alpha V_s + (1 - \alpha)V_n] = 0 \qquad V_n = V_{n(min)} = \frac{-\alpha V_s}{1 - \alpha} \qquad \frac{\alpha}{1 - \alpha} = \frac{R_2}{R_1}$$

Therefore,

$$V_{n(min)} = \frac{-R_2}{R_1} V_s \qquad (11.5)$$

In practice $V_{C(min)}$ and $V_{n(min)}$ are larger by 25 per cent. The bidirectional diode gate shown in Fig. 11.16(a) is redrawn as shown in Fig. 11.19(a). If the two control voltages are equal in magnitude but opposite in polarity the pedestal is not present in the output.

c) **Input resistance**: The purpose of the control signal is to enable the gate and the current drawn from the signal source does not depend on the control voltage. This current depends on the state of the diodes, whether they are ON or OFF. Here we assume that D_1 and D_2 as ideal diodes.

When the diodes D_1 and D_2 are OFF from Fig. 11.19(a) the equivalent circuit is as shown in Fig. 11.19(b) (obtained by open circuiting the diodes D_1 and D_2 and short circuiting V_C sources). The input resistance is calculated using the circuit shown in Fig. 11.19(b).

(i) When D_1 and D_2 are OFF

$$R_i = (R_1 + R_2)||(R_1 + R_2) \qquad (11.6)$$

$$R_i = \frac{(R_1 + R_2)}{2}$$
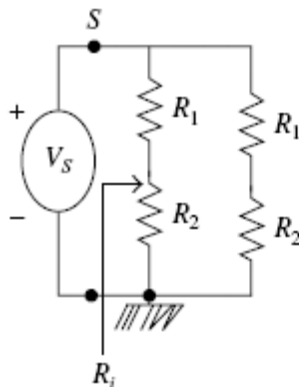
FIGURE 11.19(b) The circuit of Fig. 11.19(a) when D_1 and D_2 are OFF
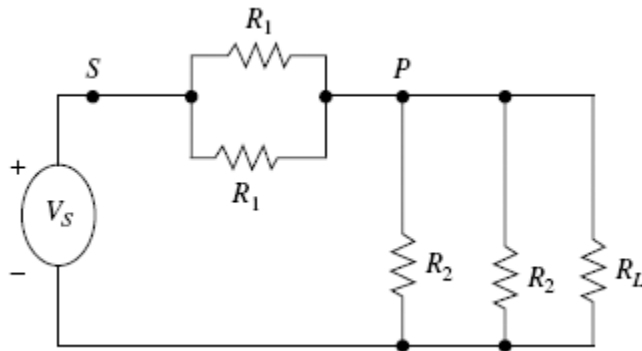
FIGURE 11.19(c) The circuit of Fig. 11.19(a) when D_1 and D_2 are ON
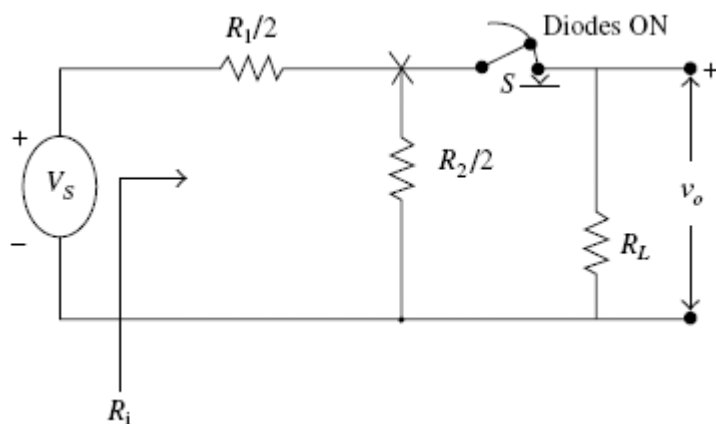
FIGURE 11.19(d) The simplified circuit of Fig. 11.19(c)

When the diodes are ON, the equivalent circuit is as shown in Fig. 11.19(c). The circuit of Fig. 11.19(c) after simplification is redrawn as shown in Fig. 11.19(d).

From the circuit in Fig. 11.19(d), input resistance R_i when the diodes are conducting is,

$$R_i = \frac{R_1}{2} + \frac{\frac{R_2}{2}R_L}{\frac{R_2}{2} + R_L}$$

$$R_i{}^1 = \frac{R_1}{2} + \frac{R_2 R_L}{R_2 + 2R_L} \qquad\qquad (11.7)$$

Now to calculate the gain of the transmission gate, A, let us calculate the Thévenin voltage source magnitude and its internal resistance. The circuit in Fig. 11.19(d) now reduces to that shown in Fig. 11.19(e).

$$V_{th} = V_s \times \frac{\dfrac{R_2}{2}}{\dfrac{R_1}{2} + \dfrac{R_2}{2}} = V_s \times \frac{R_2}{(R_1 + R_2)} = \alpha V_s$$

$$R_{th} = \frac{R_1}{2} \| \frac{R_2}{2} = \frac{R_1 R_2}{2(R_1 + R_2)} = \alpha \frac{R_1}{2}$$
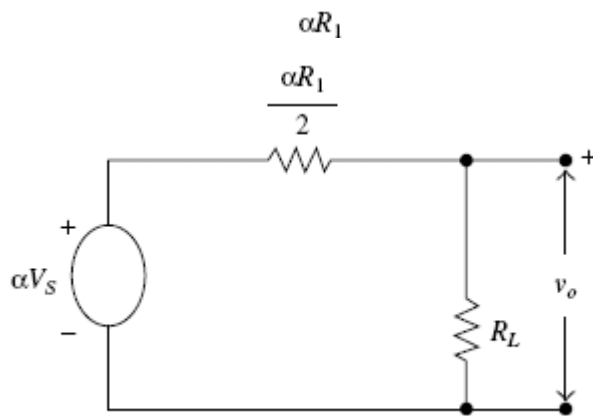
FIGURE 11.19(e) The simplified circuit of Fig. 11.19(d)

$$V_o = \frac{\alpha V_s R_L}{R_L + \alpha \dfrac{R_1}{2}}$$

$$A = \frac{V_o}{V_s} = \frac{\alpha R_L}{R_L + \alpha \dfrac{R_1}{2}} = \frac{\alpha}{1 + \alpha \dfrac{R_1}{2R_L}} \qquad (11.8)$$

Eq. (11.8) gives the expression for the transmission gain.

Four-diode Gates

The main disadvantages with two-diode gates are (i) although A is called the gain, the circuit actually offers a large attenuation to the signal since A is small (much less than 1); (ii) the two control voltages V_C and $-V_C$ should be equal in magnitude and opposite in polarity, failing which, there could be a pedestal in the output and (iii) $V_{n(min)}$ can be appreciably large, as seen in Example 11.1. These limitations can be overcome in a four diode gate shown in Fig. 11.20(a). The differences seen in the four diode gate as compared to a two diode gate shown in Fig. 11.16(a) are (i) instead of connecting control signals at points A and B, sources $+V$ and $-V$ are connected at these points and (ii) the control signals are connected through the two additional diodes D_3 and D_4 to points P_1 and P_2.
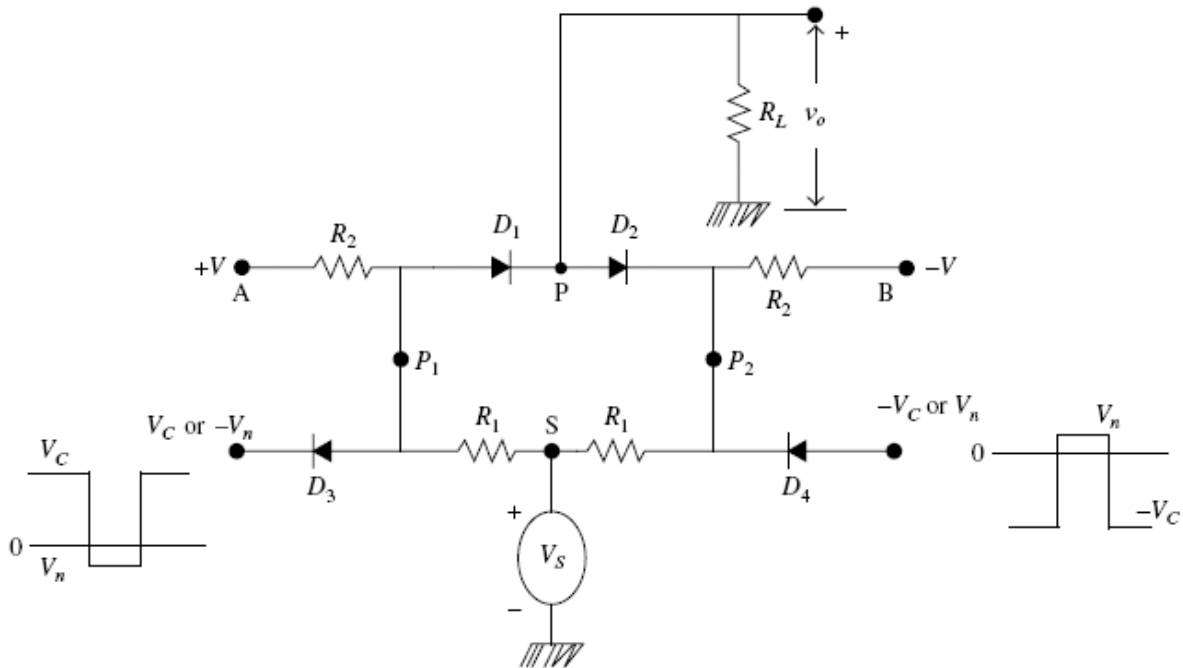
FIGURE 11.20(a) A four-diode gate

When the control voltages are V_C and $-V_C$, D_3 and D_4 are reverse-biased and are OFF. However, D_1 and D_2 are ON because of $+V$ and $-V$. The signal is connected to the load through R_1 and the conducting diodes, as shown in Fig. 11.20(b).

When the signal is transmitted, as D_3 and D_4 are OFF, even if there is a slight imbalance in the two control voltages $+V_C$ and $-V_C$, there is no pedestal at the output. Alternately, if the control voltages are at $-V_n$ and V_n respectively, D_3 and D_4 conduct. As a result, D_1 and D_2 are OFF and now the output is zero. When D_3 and D_4 are OFF, the circuit is similar to a two diode gate and A is the

same as given in <u>Eq. (11.1)</u> except for the fact that V_C and $-V_C$ are replaced by V and $-V$. Also, the minimum value of voltage $V_{(\min)}$ is the same as $V_{C(\min)}$ in <u>Eq. (11.4)</u>.

Therefore,

$$V_{\min} = \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L} \times V_s \qquad (11.9)$$

Let us now compute $V_{C(\min)}$. If $R_f \ll R_L$, for a positive V_s the voltage at P_1 is AV_s. If D_3 is to be OFF, V_C must at least be equal to AV_s.

ie., $V_{C(\min)} \approx AV_s \qquad (11.10)$

$V_{n(\min)}$ is calculated to satisfy the condition that D_2 is OFF and D_4 is ON. Then we calculate the voltage at the cathode of D_4 (K_2) due to sources $-V$ and V_s using the superposition theorem, as shown in <u>Fig. 11.20(c)</u>. The minimum voltage $V_{n(\min)}$ should at least be equal to V_{K2}.

Therefore,

$$V_{n(\min)} = V_s \times \frac{R_2}{R_1 + R_2} - V \times \frac{R_1}{R_1 + R_2} \qquad (11.11)$$
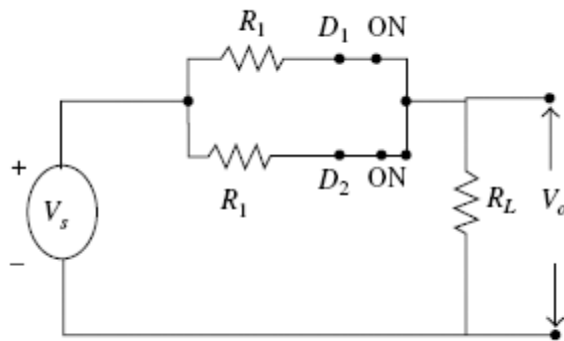
FIGURE 11.20(b) The circuit of <u>Fig. 11.20(a)</u> when D_1 and D_2 are ON and D_3 and D_4 are OFF
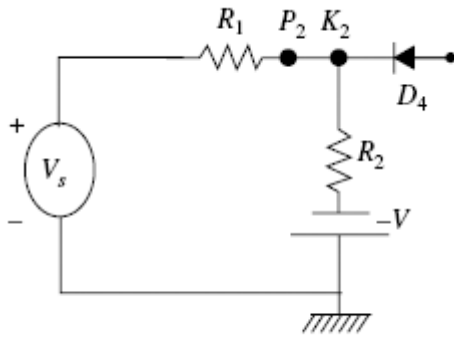
FIGURE 11.20(c) The circuit to calculate the voltage at the cathode of D_4

Six-diode Gates

For the four-diode gate shown in <u>Fig. 11.20(a)</u>, the voltages $+V$ and $-V$ need to be large and have to be balanced to avoid pedestal. This gate circuit is insensitive to slight variations in the control voltages. Also, for the four diode gate [see <u>Fig. 11.21(a)</u>], the control voltages tend to become large and further there is a need for balanced control voltages, which is difficult. However, in the former case it is easy to choose large desired values for $+V$ and $-V$ and also easy to balance these two voltages as these are dc sources. For the circuit shown in <u>Fig. 11.21(a)</u>, R_L is connected through a parallel path with the result the current is shared by these two parallel branches. The transmission gain A in both the cases, however, is approximately unity. A six diode gate is shown in <u>Fig. 11.22</u>, and it combines the features of the gate circuits shown in <u>Figs. 11.20(a)</u> and <u>11.21(a)</u>.

When no signal is transmitted, D_5 and D_6 conduct while D_1 to D_4 remain OFF. During the transmission, D_5 and D_6 are OFF and this six diode gate is equivalent to the four diode gate seen in <u>Fig. 11.21(a)</u>, earlier. If the diodes D_5 and D_6 remain OFF for the signal amplitude V_s, then,

$$V_{C(min)} = V_s \qquad\qquad (11.18)$$

The minimum required value of V_n is $V_{n(min)}$ and is equal to V_s since the transmission diodes D_1 to D_4 will not conduct unless V_s exceeds V_n.

Hence,

$$V_{n(\min)} = V_s \qquad\qquad (11.19)$$

The expression for A is given by Eq. (11.16).
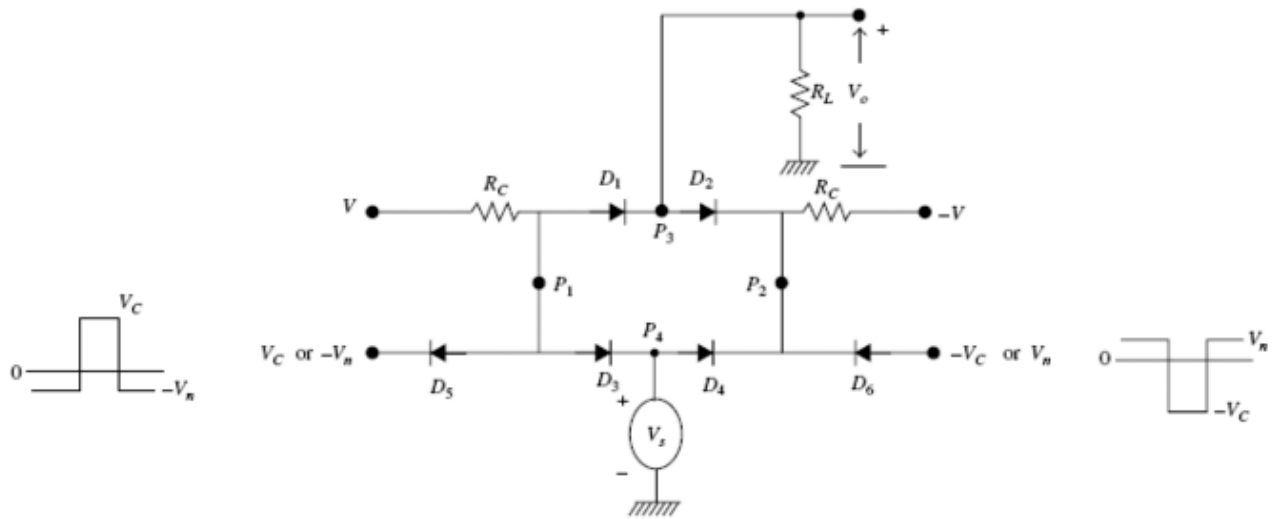
FIGURE 11.22 A six-diode gate

11.5 APPLICATIONS OF SAMPLING GATES

Sampling gates find applications in many circuits. Sampling gates are used in multiplexers, D/A converters, chopper stabilized amplifiers, sampling scopes, etc. Here, the three specific applications of the sampling gates in: chopper stabilized amplifier; sampling scope and time division multiplexer are discussed.

11.5.1 Chopper Stabilized Amplifiers

Sometimes it becomes necessary to amplify a signal v that has a very small dv/dt and that the amplitude of the signal itself is very small, typically of the order of milli-volts. Neither, ac amplifiers using large coupling condensers nor dc amplifiers with the associated drift would be useful for such an application. A chopper stabilized amplifier employing sampling gates can be a useful option in such an application, as shown in Fig. 11.27(a).
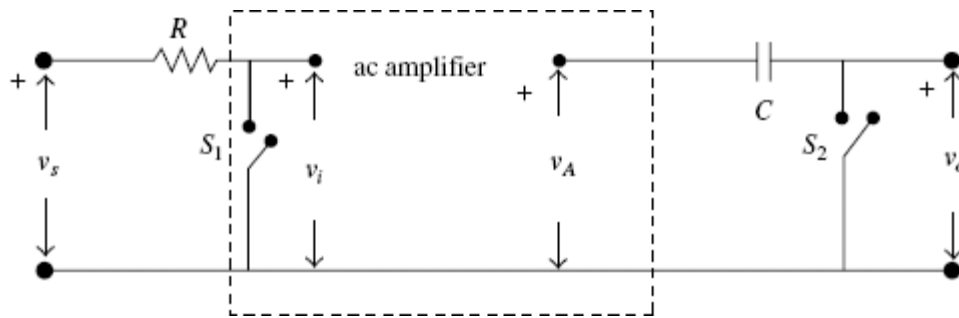
FIGURE 11.27(a) A chopper stabilized amplifier

Let the input v_s to the amplifier be a slowly varying sinusoidal signal. Switch S_1 and S_2 open and close synchronously at a fast rate i.e., the switching frequency is significantly larger than the signal frequency. When S_1 is open, v_i is the same as v_s. When S_1 is closed, v_i = 0. As the switching frequency is large, the samples are taken at smaller time intervals. With the result, the signal v_i contains pulses with almost flat tops and have the same amplitude of the input signal as is available at the instant of sampling. As a result, the input of the amplifier v_i is a chopped signal—R and S_1 constitute the chopper. Hence, v_i can be described as a square wave at the switching frequency (if dv/dt is small), i.e., amplitude modulated by the input signal and superimposed on a signal (dashed line) that is proportional to v_s. The waveform v_A at the amplifier output is an amplitude modulated square wave, as shown in <u>Fig. 11.27(b)</u>. Hence, a chopper is also called a modulator.

Let S_1 and S_2 operate in synchronism. During $t = T_1$, the negative going component of v_A is zero and during $t = T_2$ the positive going component is zero. Also, because of the amplifier, v_o is greater than v_i in amplitude. Except for this change, v_A is similar to v_i, as shown in <u>Fig. 11.27(c)</u>. This signal is passed through a low pass filter which eliminates the squarewave and retrieves the original signal. If S_2 opens when S_1 is closed, the output is shifted in phase by 180°, as shown in <u>Fig. 11.27(d)</u>. C and S_2 constitute a synchronous detector. The chopper eliminates the need for a dc stabilized amplifier. This amplifier is called a chopper stabilized amplifier.

11.5.2 Sampling Scopes

Another application of a sampling gate is in a sampling scope used to display very fast periodic waveforms, having a rise time of the order of nano-seconds. A general purpose CRO may be used for displaying such waveforms. However, a CRO needs a wideband amplifier. A sampling scope eliminates the use of the high gain wideband amplifier. The basic principle of

a sampling scope is explained with the aid of a block diagram shown in <u>Fig. 11.28(a)</u> and the waveforms are shown in<u>Fig. 11.28(b)</u>.

(a) Input signal

(b) Chopped signal

(c) Signal-modulated square wave when S_1 and S_2 operate in synchronism

(d) Signal-modulated square wave when S_1 and S_2 do not operate in synchronism
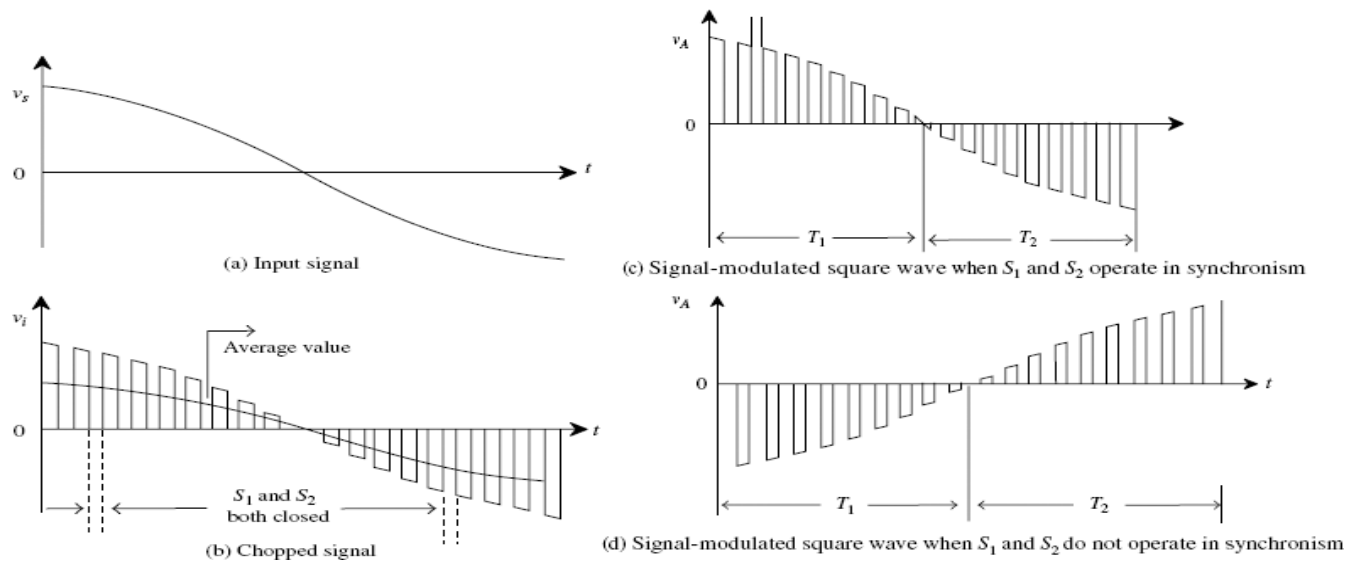
FIGURE 11.27(b) The waveforms of the chopper stabilized amplifier

(a) The trigering signal

(b) Signal to be observed

(c) The ramp and staircase signals
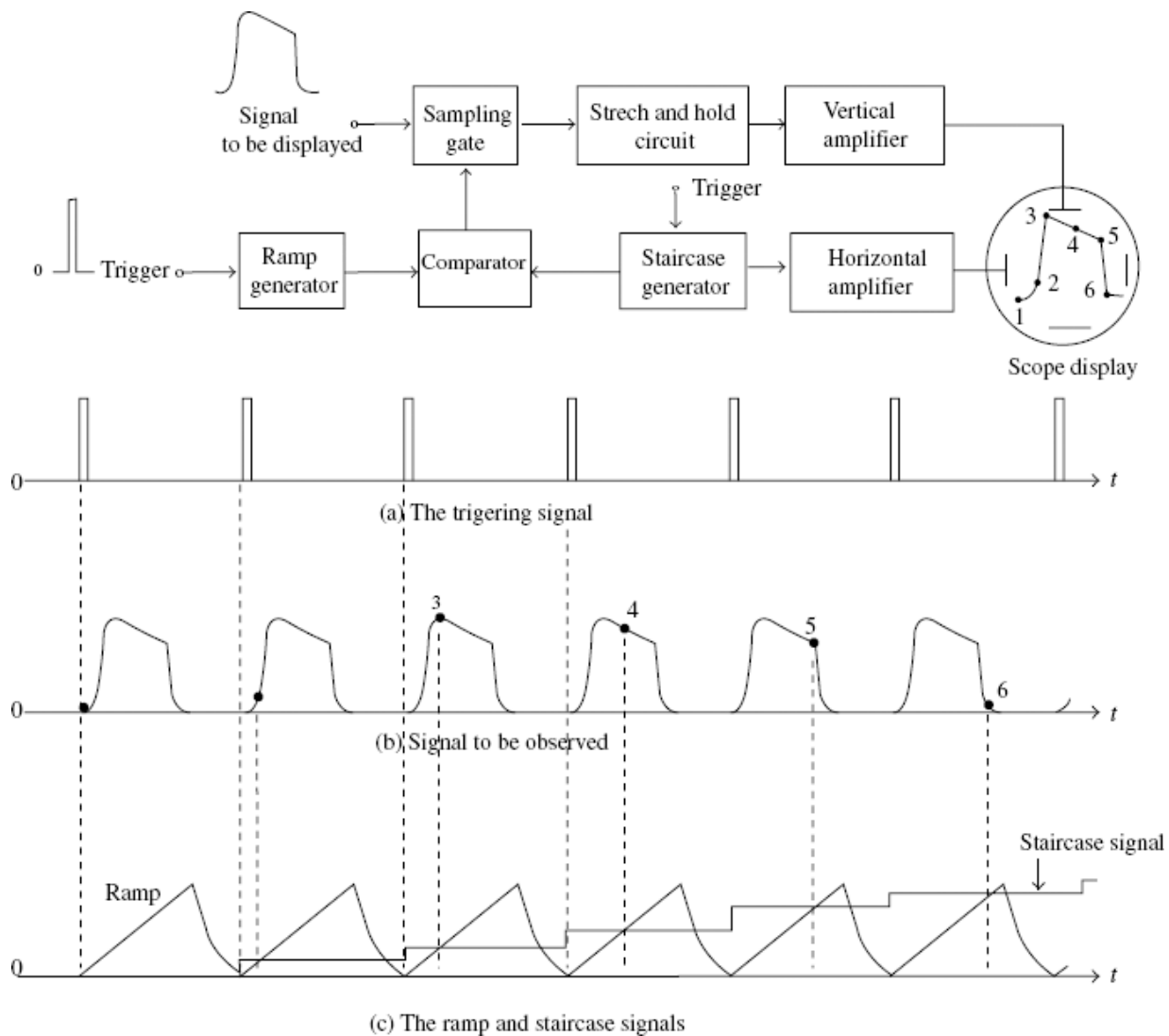
FIGURE 11.28(a) The waveforms that explain the principle of sampling-scope

Let the trigger signals shown in Fig. 11.28(a) occur slightly prior to the occurrence of the pulses that are to be displayed on the screen. These trigger signals trigger ramp and staircase generators. The staircase generator has constant amplitude between the triggers and its amplitude jumps to a higher level at the instant the trigger is present. The amplitude of the staircase generator remains the same till the presence of the next trigger. The inputs to the comparator are the staircase and ramp signals. The instant the ramp reaches the amplitude of the staircase signal; a pulse is produced at the output of the comparator. This pulsed output of the comparator is used as the control signal for the sampling gate. When a control signal is present, the gate transmits a sample of the signal to the vertical amplifier whose amplitude is the same as that of the signal at the instant of sampling and has the same duration as the control signal. Points 1, 2..., 6 are the instants at which the samples are taken. The output of the staircase generator is connected to the horizontal deflecting plates.

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When one sample is taken, say at instant 1, to go to the next sample, i.e., sample 2, the amplitude of sample 1 should be held constant till the next trigger pulse arrives. Therefore, it becomes necessary to hold the amplitude of the input signal between successive triggers and hence, the need for a stretch and hold circuit. The staircase generator moves the spot horizontally across the screen in steps and at each step the spot is deflected vertically proportional to the signal amplitude. The CRT beam is blanked normally and is un-blanked only at the time of display of the sample. Thus, the signal is represented by a series of dots.

11.5.3 Multiplexers

An analog time division multiplexer using a sampling gate is shown in Fig. 11.29(a). In the FET Q_1, Q_2 and Q_3 are ON when the control voltages V_{C1}, V_{C2} and V_{C3} are at 0 V. The voltage V is more negative than the pinch off voltage of the FET. As such the FET is OFF when the gate voltage is V. During the period 0 to T_1, V_{C1} is such that Q_1 is ON. At the same time Q_2 and Q_3 are OFF. Hence, input V_{S1}, which is the sinusoidal signal is present at the output during this period. During the period T_1 to T_2, Q_2 is ON and Q_1 and Q_3 are OFF. Hence, only V_{S2} is present at the output during this period. During the period T_2 to T_3, Q_3 is only ON and hence, V_{S3} is present at the output. The output now contains all the input signals separated by a specific time interval, as shown in Fig. 11.29(b).
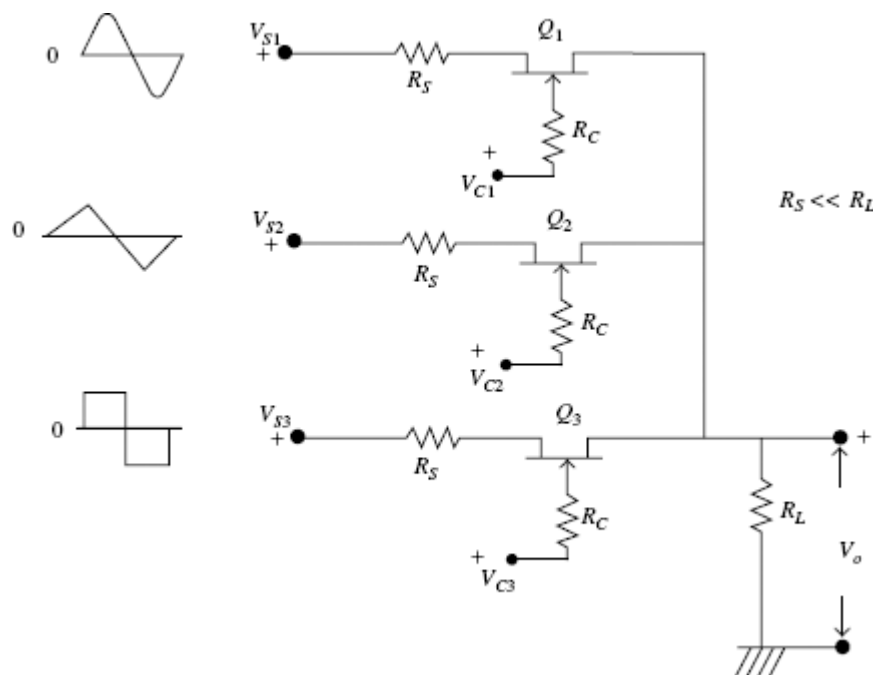
FIGURE 11.29(a) The sampling gate used for time division multiplexing
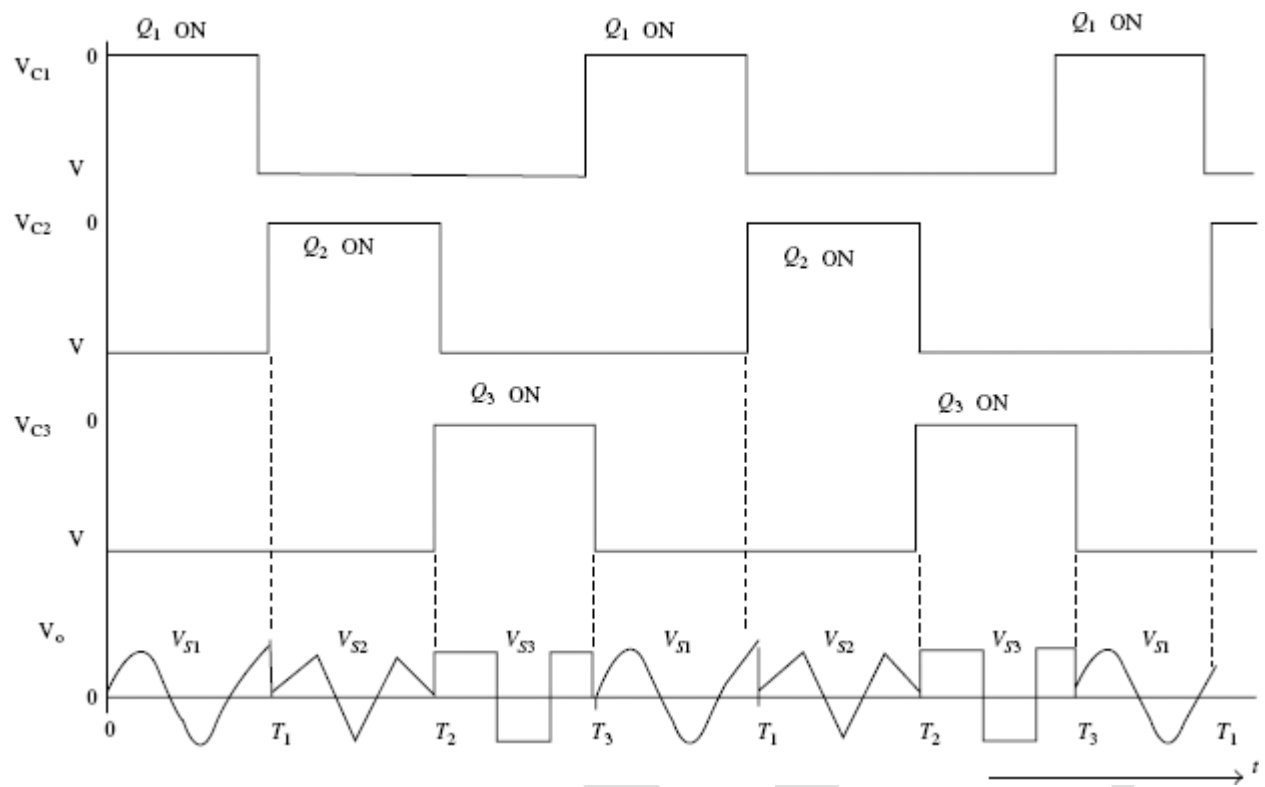
FIGURE 11.29(b) The control signals and the output of the multiplexer

UNIT-4 - a

Multivibrators

Multivibrator

A multivibrator is an electronic circuit used to implement a variety of simple two-state systems such as oscillators, timers and flip-flops. It is characterized by two amplifying devices (transistors, electron tubes or other devices) cross-coupled by resistors orcapacitors. The name "multivibrator" was initially applied to the free-running oscillator version of the circuit because its output waveform was rich in harmonics.[1] There are three types of multivibrator circuits depending on the circuit operation:

- astable, in which the circuit is not stable in either state —it continually switches from one state to the other. It does not require an input such as a clock pulse.
- monostable, in which one of the states is stable, but the other state is unstable (transient). A trigger causes the circuit to enter the unstable state. After entering the unstable state, the circuit will return to the stable state after a set time. Such a circuit is useful for creating a timing period of fixed duration in response to some external event. This circuit is also known as a one shot.
- bistable, in which the circuit is stable in either state. The circuit can be flipped from one state to the other by an external event or trigger.

Multivibrators find applications in a variety of systems where square waves or timed intervals are required. For example, before the advent of low-cost integrated circuits, chains of multivibrators found use as frequency dividers. A free-running multivibrator with a frequency of one-half to one-tenth of the reference frequency would accurately lock to the reference frequency. This technique was used in early electronic organs, to keep notes of different octaves accurately in tune. Other applications included early television systems, where the various line and frame frequencies were kept synchronized by pulses included in the video signal.

History

The classic multivibrator circuit (also called a plate-coupled multivibrator) is first described by H. Abraham and E. Bloch in Publication 27 of the French Ministère de la Guerre, and in Annales de Physique 12, 252 (1919). It is a predecessor of Eccles-Jordan trigger[2]derived from this circuit a year later.

Bistable Multivibrators

A bistable multivibrator has two stable states and this circuit also employs two devices, Q_1 and Q_2. If one device is ON, the other device is required to be OFF. If initially Q_1 is OFF, the voltage at the collector of Q_1 is $V_{C1} = V_{CC}$; and when Q_2 is ON, the voltage at this collector $V_{C2} \approx 0$ V. This is the initial stable state for the bistable multivibrator. The circuit of flipped from one stable state to other (i.e driving into the other stable state in which Q_1 is ON and Q_2 is OFF) by an external trigger. On the application of a trigger, Q_1 switches ON ($V_{C1} \approx 0$ V) and Q_2 switches OFF ($V_{C2} = V_{CC}$) and the states of Q_1 and Q_2 are flipped only when another trigger is applied. If V_{CC} is taken to represent "1" in binary and 0 V represents "0". So "1" level remains as "1" and "0" level remains as a "0" till the application of a trigger signal. Hence, this type of circuit is used as a one-bit memory element in digital circuits. An array of such circuits can be used to write or store a string of binary digits (0 s or 1 s), called a register. This becomes the basic memory unit in digital computers. This circuit is also known by many names such as binary, flip-flop, scale-of-two circuit and Eccles–Jordan circuit. If the ON device is driven to saturation, the binary is called a saturating binary. If, on the other hand, the ON device is held in the active region, the binary is called a non-saturating binary. An emitter-coupled binary is called a Schmitt trigger. This circuit, in addition to operating as a binary, can also be used as an amplitude comparator and as a squaring circuit.

BISTABLE MULTIVIBRATOR CIRCUITS

The two types of bistable multivibrator circuits considered here are fixed-bias bistable and self-bias bistable multivibrators. In the first circuit, two separate sources are used for biasing the devices whereas in the second one self-bias is used to derive the biasing voltage.

Besides the two circuits, there is a third variation of bistable mulivibrators, namely, the Schmitt trigger. This circuit, in addition to being used as a bistable, can also be used for other applications like waveshaping, comparators, etc

Fixed-bias Bistable Multivibrators

The circuit shown in Fig. 9.1(a) is called a fixed-bias bistable multivibrator as two separate dc sources are used to bias the transistors. The circuit consists of two inverters, the output of one is connected as the input to the other.

Let it be arbitrarily assumed that initially Q_1 is OFF and Q_2 is ON and in saturation. Then the voltage at the first collector is V_{CC} (the binary equivalent of which is 1) and the voltage at the second collector is $V_{CE(sat)}$ (the binary equivalent being 0). If a negative trigger is applied at the base of the ON device (Q_2), Q_2 goes into the OFF state and its collector voltage rises to V_{CC}. Consequently Q_1 goes into the ON state and its collector voltage falls to $V_{CE(sat)}$. Let us now verify whether Q_1 is really OFF and Q_2 is really ON and in saturation.

To Verify that Q_2 is ON and in Saturation. For this, we have to calculate its base current I_{B2} and its collector current I_{C2} to ensure that the base current is significantly higher than the minimum so that Q_2 is really in saturation. To calculate I_{B2} using <u>Fig. 9.1(b)</u>, we begin by assuming that Q_2 is in saturation and Q_1 is OFF and justify the assumption made.

To find I_{B2}, we calculate I_1 and I_2.

$$I_1 = \frac{V_{CC} - V_\sigma}{R_C + R_1} \tag{9.1}$$

$$I_2 = \frac{V_\sigma - (-V_{BB})}{R_2} \tag{9.2}$$

To calculate I_{C2}, we use the circuit shown in <u>Fig. 9.1(c)</u>.

$$I_3 = \frac{V_{CC} - V_{CE(sat)}}{R_C} \tag{9.4}$$

$$I_4 = \frac{V_{CE(sat)} - (-V_{BB})}{R_1 + R_2} \tag{9.5}$$

$$I_{C2} = I_3 - I_4 \tag{9.6}$$

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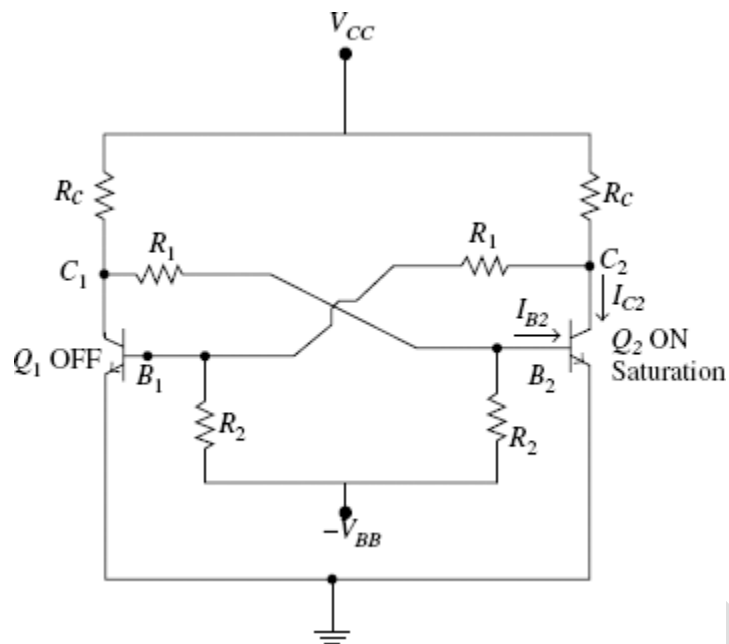
FIGURE 9.1(a) The fixed-bias bistable multivibrator
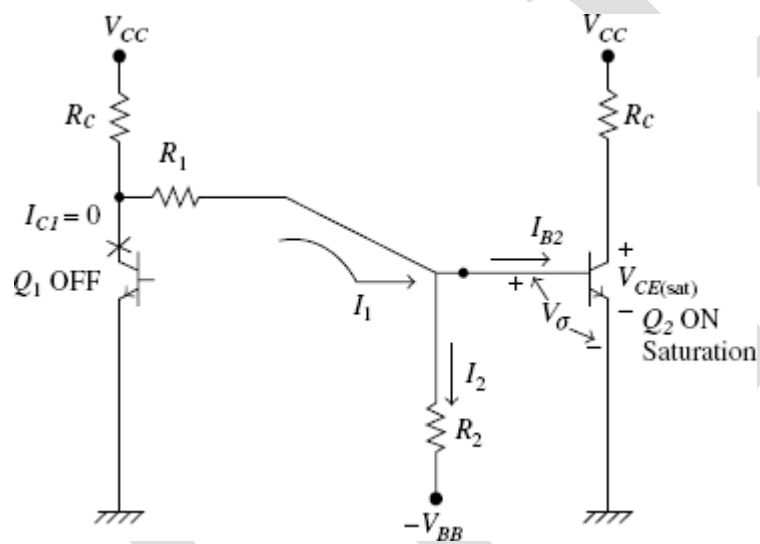
FIGURE 9.1(b) The circuit that enables the calculation of I_{B2}
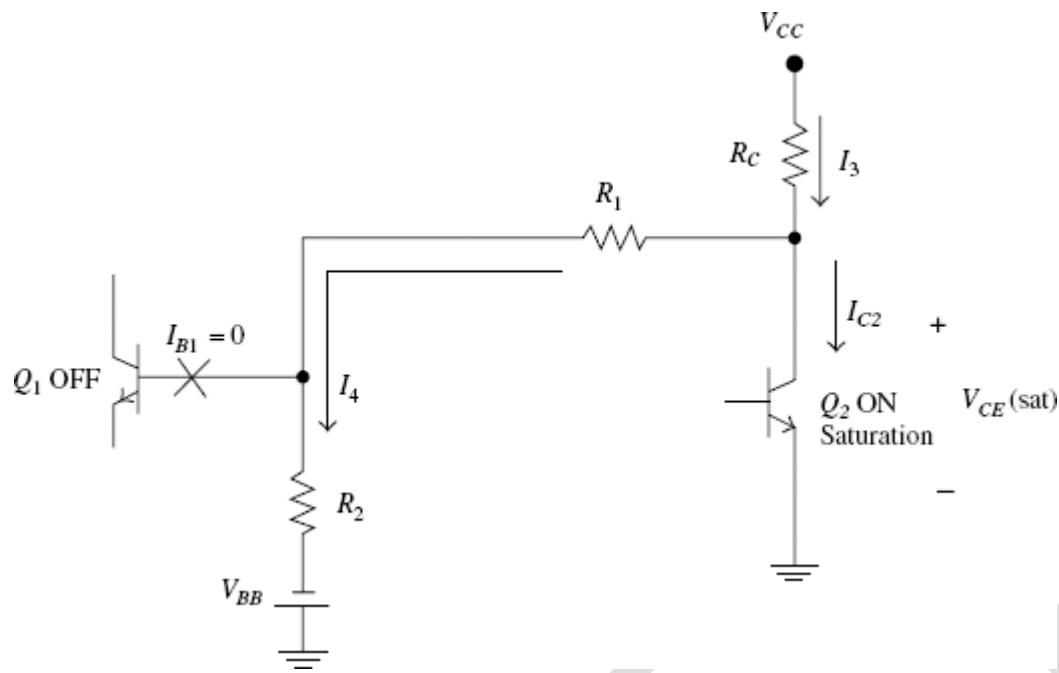
FIGURE 9.1(c) The circuit that enables calculation of I_{C2}

Now find $I_{B2(\text{min})}$ using the relation:

$$I_{B2(\text{min})} = \frac{I_{C2}}{h_{FE(\text{min})}}$$

If $I_{B2} \gg I_{B2(\text{min})}$, then Q_2 is in saturation, as assumed.

To Verify that Q_1 is OFF. The transistor Q_1 is OFF if its base–emitter diode is reverse-biased. To verify this, we calculate the voltage V_{B1} at the base of Q_1 using the circuit shown in Fig. 9.1(d) and check whether it reverse-biases the emitter diode or not. If the emitter diode is reverse-biased, the transistor is indeed in the OFF state.
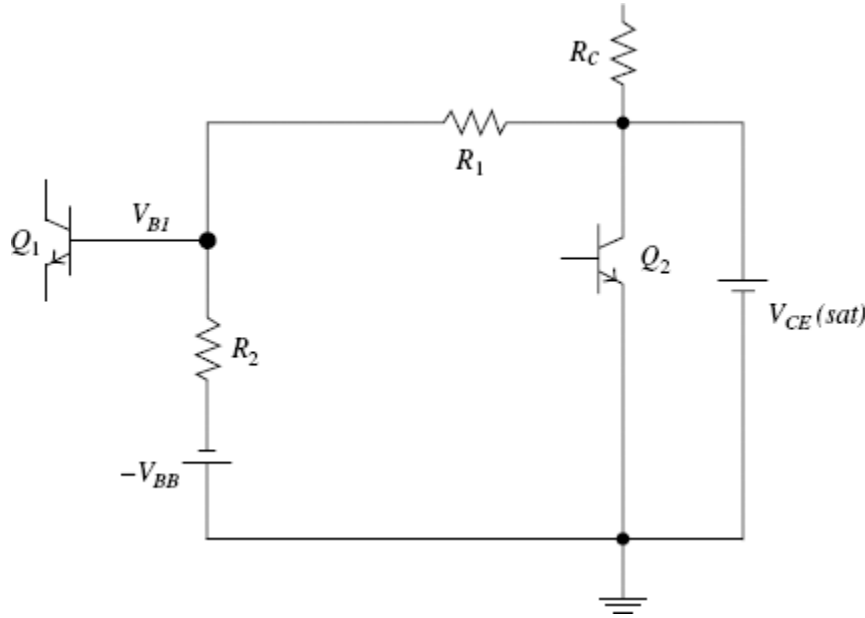
FIGURE 9.1(d) The circuit to calculate V_{B1}

The voltage V_{B1} at the base of Q_1 is due to the two sources: $-V_{BB}$ and $V_{CE(sat)}$. Using the superposition theorem:

$$V_{B1} = V_{CE(sat)} \frac{R_2}{R_1 + R_2} + (-V_{BB}) \frac{R_1}{R_1 + R_2} \qquad (9.7)$$

If the voltage between the base and emitter terminals of Q_1 reverse-biases the base–emitter diode, then Q_1 is OFF and $V_{C1} = V_{CC}$. However, V_{C1} is not exactly V_{CC} as it should be when Q_1 is OFF. Instead, it is smaller than this, because of the cross-coupling network comprising R_1 and R_2. There is a current I_1 through R_1 and R_C. Therefore, the actual voltage at the first collector is not necessarily V_{CC}, but somewhat lower than V_{CC}.

$$V_{C1} = V_{CC} - I_1 R_C \qquad (9.8)$$

The currents and voltages in the initial stable state are calculated, using Eqs. (9.1) to (9.8). Sometimes the output of the bistable multivibrator is required to drive some other circuit. Let the voltage V_{CC} at the collector of the OFF device drive another circuit, as shown in Fig. 9.1 (e). If the circuit to be driven, offers an input resistance R_i, this becomes the load ($=R_L$) for the bistable multivibrator. The effective load resistance at the collector, $R_C//R_L$, will be now small if R_L is small and the collector voltage falls to a value less than V_{CC}. If this falls appreciably, the ON device may not be driven into saturation as required. Therefore, we have to ensure that the voltage at the collector of the OFF device is not allowed to fall below a threshold level.

Hence, R_L is chosen such that R_L is $R_{L(min)}$ for which I_L is $I_{L(max)}$, but at the same time making sure that Q_2 is in saturation. $R_{L(min)}$ is called as the heaviest load and $I_{L(max)}$ as the corresponding load current [see Fig. 9.1(f)]. When I_{B2} drops to $I_{B2(min)}$, the corresponding R_L is considered as the heaviest load.

$$I_{B2(min)} = \frac{I_{C2}}{h_{FE(min)}}$$

Then,

$$I_{1(min)} = I_{B2(min)} + I_2 \qquad\qquad\qquad (9.9)$$
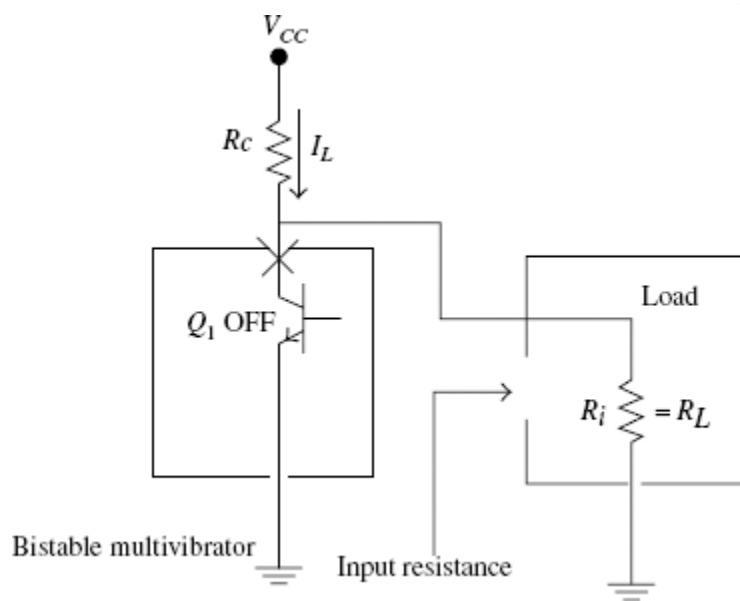
FIGURE 9.1(e) The output of the bistable multivibrator driving another circuit
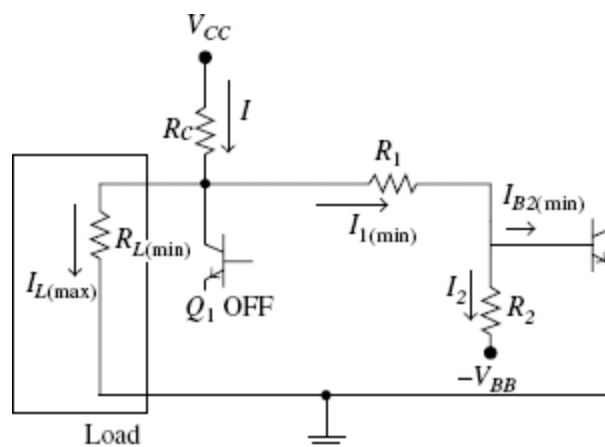
FIGURE 9.1(f) The calculation of the heaviest load

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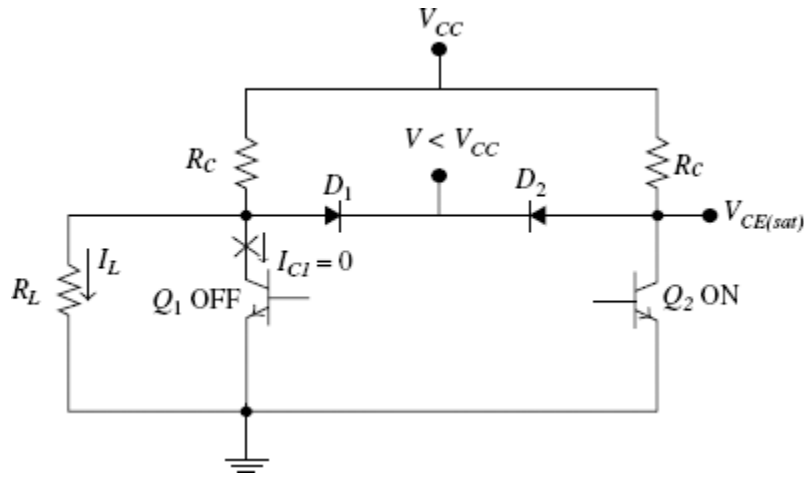
FIGURE 9.1(g) The use of collector catching diodes
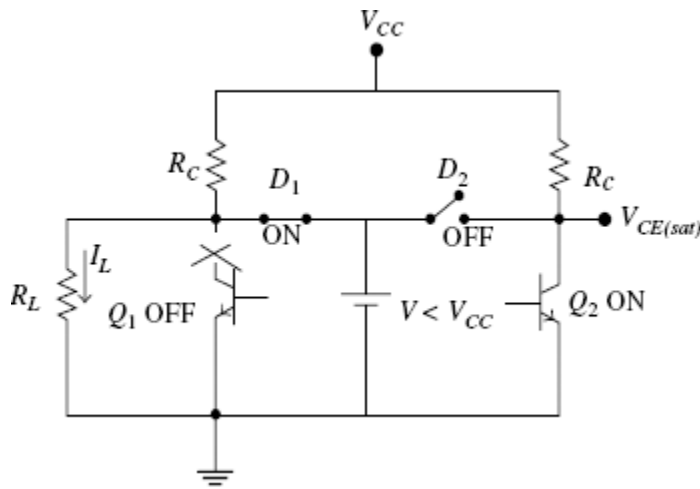
FIGURE 9.1(h) The simplified circuit of Fig. 9.1(g)

Therefore, the new value of V_{C_1} is

$$V_{C1(\text{min})} = I_{1(\text{min})}R_1 + V_{B2} \qquad (9.10)$$

Earlier V_{C_1} was given by Eq. (9.8). Due to R_L, V_{C_1} has now fallen to $V_{C1(\text{min})}$ as given by Eq. (9.10).

$$I = \frac{V_{CC} - V_{C1(\text{min})}}{R_C} \qquad (9.11)$$

$$I_{L(\text{max})} = I - I_{1(\text{min})} \qquad (9.12)$$

$$R_{L(\text{min})} = \frac{V_{C1(\text{min})}}{I_{L(\text{max})}} \qquad (9.13)$$

This is the minimum value of R_L that can be connected as load. It is seen that by connecting the load to a bistable multivibrator the voltage at the collector of the OFF device falls, if there

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is a loading on the collector. To ensure that the voltage does not fall below a specified threshold, diodes D_1 and D_2, called collector catching diodes, are used along with a source V, as shown in Fig. 9.1(g).

V_{C_1}, was the voltage, prior to connecting the load R_L at the first collector. Let $V < V_{C_1}$. Then, D_1 conducts and during this period D_2 is OFF, as $V_{C_2} = V_{CE(sat)}$. When D_1 is ON, it simply acts as a switch and hence, V is directly connected to the first collector. A simplified circuit of Fig. 9.1(g) is shown in Fig. 9.1(h). As V is a source that can deliver a large current, the loading (drawing more current) at this collector can be eliminated. As D_1 and D_2 clamp the collectors to V (hold the collector voltage at V), when the respective devices (Q_1 or Q_2) are OFF, these diodes are called collector catching diodes. To calculate the stable-state currents and voltages, let us consider Example 9.1.

Commutating Condensers. In Section 8.4, we learnt that a commutating condenser is connected across R_1 to reduce the transition time. As in a bistable multivibrator there are two cross-coupling resistances R_1 and R_1, C_1 and C_1 need to be connected across these resistances to transfer conduction from one device to the other, soon after the application of the trigger. Hence, the bistable multivibrator is modified as shown in Fig. 9.4.

However, the moment the commutating condensers are connected to reduce the transition time, voltages of value V_A and V_B exist across the two capacitors. When Q_1 is OFF and Q_2 is ON, the values of these two voltages can be calculated using the following equations:

$$V_A = V_{C1} - V_{B2} = V_{CC} - V_\sigma \qquad (9.20)$$

$$V_B = V_{C2} - V_{B1}$$

$$= V_{CE(sat)} - V_{B1} \text{ (a small negative voltage)} \qquad (9.21)$$
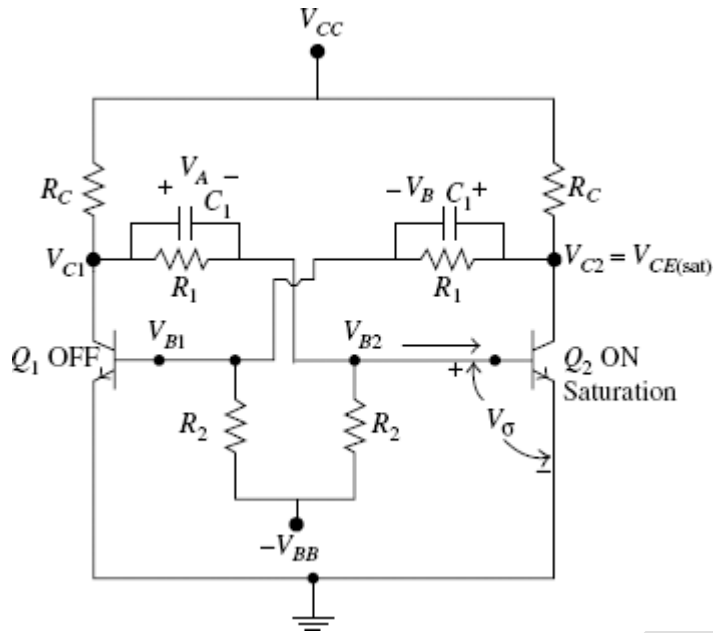
FIGURE 9.4 A fixed-bias bistable multivibrator with commutating condensers

If a trigger is applied to change the state of the devices, Q_1 quickly goes into the ON state when Q_2 switches into the OFF state as the transition time is negligible. However, the voltages across the two capacitors will not switch instantaneously. The multivibrator is said to have settled down in its new state completely only when the capacitor voltages also switch. The next trigger, to once again change the state of the two devices, can be applied only then. The interval during which the capacitor voltages interchange is called the settling time. Thus, settling time is defined as the time taken for the capacitor voltages to interchange after conduction is transferred from one device to the other, on the application of a trigger.

The Resolution Time and the Maximum Switching Speed of a Bistable Multivibrator

The sum of transition time and settling time is called the resolution time of the bistable multivibrator.

$$t_{res} = t_{trans} + t_{settling} \approx t_{settling}, \text{ as } t_{trans} \text{ is small.} \tag{9.22}$$

where, t_{res} is the resolution time, t_{trans} is the transition time, and $t_{settling}$ is the settling time.

Thus, the resolution time is the minimum time interval required between successive trigger pulses to reliably drive the multivibrator from one state to the other. The reciprocal of the resolution time is called the maximum switching speed of a bistable multivibrator.

$$f_{(max)} = \frac{1}{t_{res}} \qquad\qquad\qquad (9.23)$$

Equation (9.23) tells us as to how fast we can switch the bistable multivibrator from one stable state to the other. To be able to reliably trigger the bistable multivibrator from one stable state to the other, we have to wait for a time interval t_{res}. The transition time, as we have seen, is appreciably reduced by connecting commutating condensers. As a result, the resolution time is approximately equal to the settling time, during which period the voltages across the two commutating condensers interchange. The recharging time constants associated with the two condensers, C_1 and C_1' shown in Fig. 9.5(a)are used to calculate the resolution time t_{res}.

In order to distinguish between the two capacitors in the circuit, they are labelled differently as C_1 and C_1', though in actuality the two capacitors are equal i.e, $C_1 = C_1'$. To find the recharging time constant associated with the capacitor C_1', consider the circuit shown in Fig. 9.5(b).

As Q_2 is ON and in saturation, r_{bb}' appears between its base and emitter terminals. The net resistance in the circuit is R', as shown in Fig. 9.5(c).

$$R' = R_1 \,||\, (R_C + R_i) = R_1 \,||\, (R_C + r_{bb}') \approx R_1 \,||\, R_C \qquad\qquad (9.24)$$
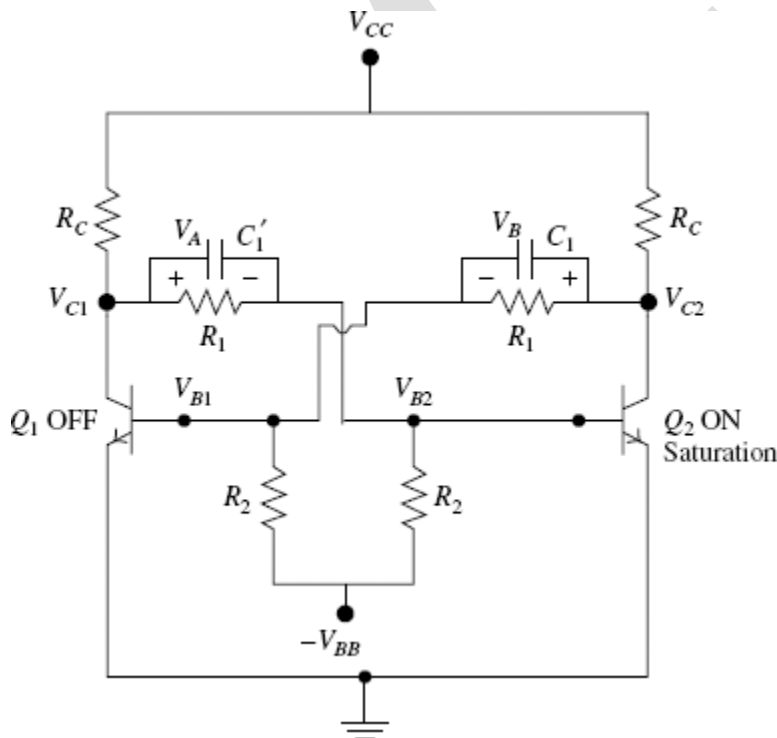
FIGURE 9.5(a) The bistable multivibrators with commutating condensers C'_1 and C_1

$R_i = r_{bb'}$
$R_2 >> R_i$ and the
effective resistance
$R_2 \| R_i$ is R_i
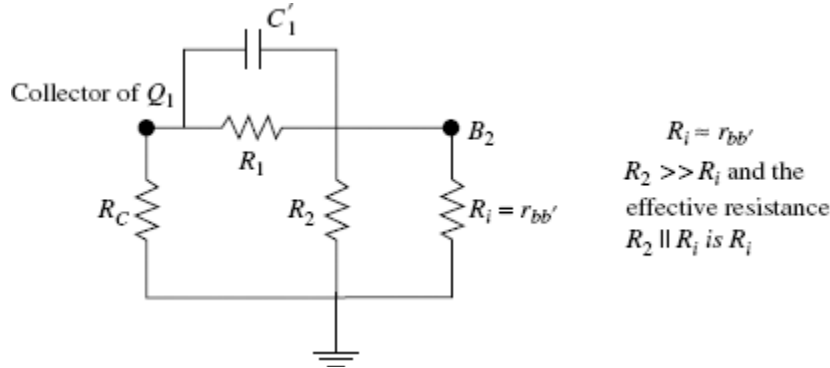
FIGURE 9.5(b) The circuit to calculate the recharging time constant of capacitor C'_1

$R_i = r_{bb'}$
$R_2 >> R_i$ and the
effective resistance
$R_2 \| R_i$ is R_i
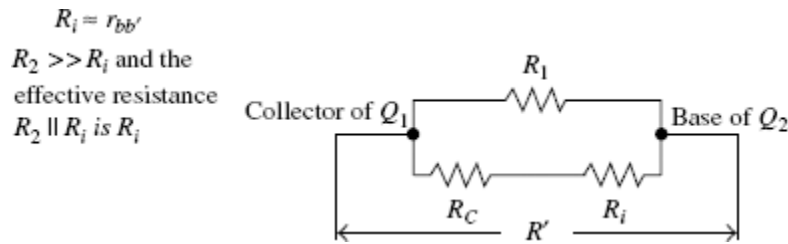
FIGURE 9.5(c) The calculation of the effective resistance, R
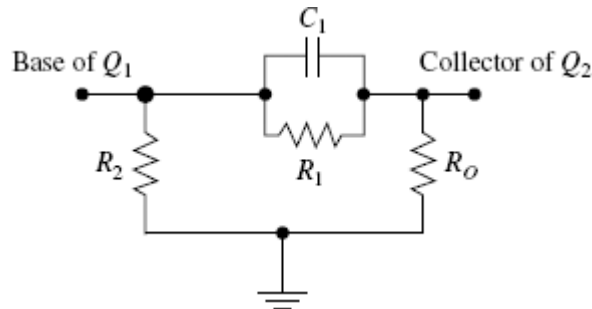
FIGURE 9.5(d) The circuit to calculate the recharging time constant of C_1
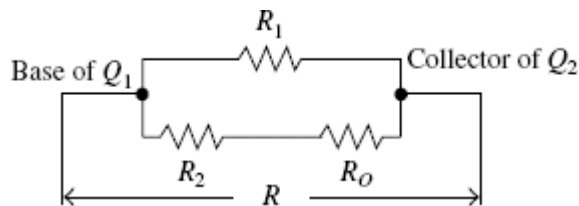
FIGURE 9.5(e) The calculation of the effective resistanc, R

Hence, the recharging time constant associated with this condenser C'_1 is,

$$\tau' = R' C'_1 \qquad\qquad (9.25)$$

To find the recharging time constant associated with C_1, the corresponding circuit is shown in Fig. 9.5(d). R_o is the output resistance of Q_2 (in saturation) taking R_C also into account, which is small. The net resistance in the circuit is R, as shown in Fig. 9.5(e).

$R = R_1 \,||\, (R_2 + R_o)$

$R = R_1 \,||\, R_2$ as R_o is small. $\hspace{4cm}$ (9.26)

The recharging time constant associated with $C_1 = \tau$ is calculated from Fig. 9.5(f).

$\tau = RC_1$ $\hspace{4cm}$ (9.27)

FIGURE 9.5(f) The circuit to calculate τ

From Eqs. (9.25) and (9.27) it is evident that $\tau > \tau'$.

After conduction is transferred from one device to the other, it is assumed that voltages across the capacitors interchange in a time period $(\tau + \tau')$. However as $\tau > \tau'$, if the resolution time is taken to be 2τ, the voltages across these capacitors would certainly interchange before the application of the next trigger. Hence,

$t_{res} = 2\tau = 2 \times \dfrac{R_1 R_2 C_1}{R_1 + R_2}$ $\hspace{2cm}$ (9.28)

And the reciprocal of it is,

$f_{(max)} = \dfrac{R_1 + R_2}{2 R_1 R_2 C_1}$ $\hspace{3cm}$ (9.29)

Methods of Improving the Resolution Time of a Bistable Multivibrator. The resolution time, as given by Eq. (9.28), is $t_{res} = 2C_1 (R_1 \,//\, R_2)$. For reducing the resolution time and hence, improving the switching speed, the following considerations have to be taken into account:

1. A finite transition time exists mainly because of stray capacitances of the transistor. Commutating condensers are used, to reduce the transition time, and once they are used there is a settling time. If devices with negligible stray capacitances are used, the problem of settling time does not arise at all.

Similarly, to reduce the resolution time the devices with negligible stray capacitances called as switching devices are chosen.

2. However, for the devices chosen, if the influence of stray capacitances can not be neglected, then invariably commutating condensers (C_1 and C_1) need to be used. For t_{res} to be small, C_1 must be small. Though, if C_1 is smaller, transition time is lengthened. Alternately, if C_1 is larger, settling time is lengthened. For perfect compensation, C_1 is chosen satisfying the requirement of a compensated attenuator, as discussed in Section 3.3.2 and is given by $C_1 = C_i(R_2/R_1)$, where C_i is the stray input capacitance of the transistor.

3. If t_{res} is to be smaller, a third option could be to have smaller values of R_1 and R_2. However, smaller values of R_1 and R_2 will load the collector of the OFF device, resulting in a reduced voltage at its collector. It is possible that this reduced voltage may not be able to drive the ON device into saturation, as desired. Secondly, smaller values of R_1 and R_2 tend to draw larger current from the dc sources, thereby, increasing the drain on the batteries.

Hence, to improve the resolution time, the transistors should be chosen carefully and a compromise should be arrived at in view of the points discussed in this section.

Methods of Triggering a Bistable Multivibrator

To switch the bistable multivibrator from one stable state to the other, a trigger of proper polarity and magnitude is applied at an appropriate point in the circuit. The purpose of a trigger is to change the state of the devices. The trigger can be a dc trigger or a pulse trigger. However, in circuits like counters (which we are going to consider later), the trigger is normally a pulse train. Here, the focus is on pulse triggering only. There are two methods of triggering a bistable multivibrator using pulses:

1. Unsymmetric triggering
2. Symmetric triggering.

Unsymmetric Triggering. In this method of triggering, one trigger pulse, taken from a source, is applied at one point in the circuit. The next trigger pulse taken from a different source is applied at a different point in the circuit [see Fig. 9.6(a)]. It has been mentioned earlier that the trigger is applied at the base of the ON device. However, since commutating condensers are connected in this circuit, the trigger pulse is not connected to the base of Q_2 directly, but is applied at the collector of Q_1 through a condenser. As the capacitor behaves as a short circuit when there is a sudden change in voltage, the negative pulse applied at the collector of Q_1 is coupled to the base of Q_2.

Let the set trigger be applied to the circuit at $t = 0$. If Q_1 is OFF, the voltage at this collector is V_{CC}. Therefore, D_1 is ON and this negative pulse appears at the base of Q_2 as the first collector and the second base are connected through C_1. Q_2 goes into the OFF state and Q_1 into the ON state.
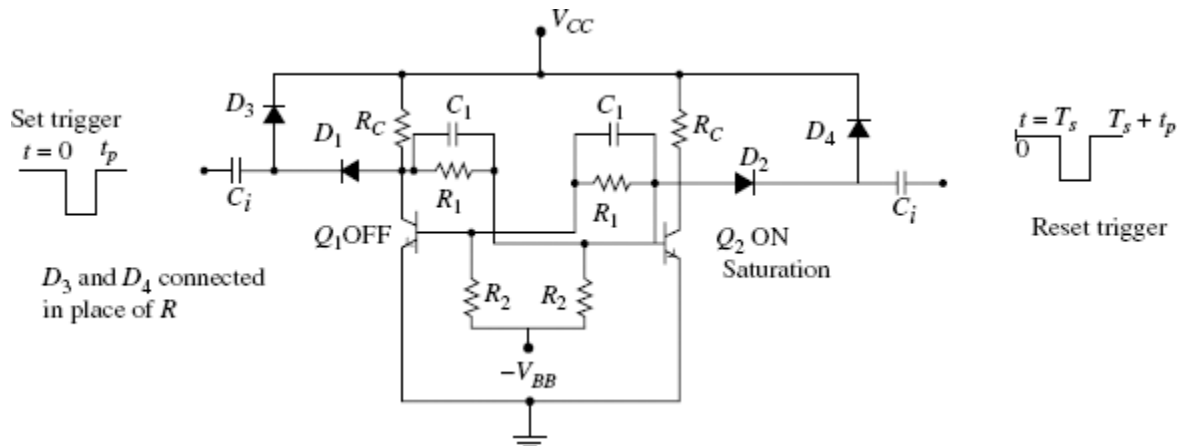
FIGURE 9.6(a) The unsymmetric triggering of a bistable multivibrator

The next trigger pulse, i.e., the reset pulse, is applied through D_2 at the second collector which is coupled to the first base through C_1. Q_1 now goes into the OFF state and Q_2 into the ON state. Let us look at the voltages at the two collectors as shown in Fig. 9.6(b).

The set trigger pulse applied at $t = 0$ sets the voltage at the second collector to V_{CC}. The reset pulse applied after a time interval T_s, resets the voltage at the second collector to $V_{CE(sat)}$. Hence, a pulse is generated at this collector and similarly at the first collector. The duration of this pulse is equal to the spacing between successive trigger pulses. Hence, unsymmetric triggering is used to generate a gated output, the width of this gate being the spacing between two successive triggers.

As discussed in Section 8.2.1, diodes D_3 and D_4 are used in place of a resistance R. When a negative trigger pulse appears, the diode is OFF (D_3 or D_4); the large reverse resistance of the diode avoids loading the trigger source. When the trigger is absent, the diode is ON and offers a negligible resistance so that the charge on the capacitor C_i can be quickly removed.

Symmetric Triggering. In symmetric triggering, successive trigger pulses taken from the same source and applied at the same point in the circuit will cause the multivibrator to change from one stable state to the other. This method of triggering is normally used in counters, as shown in Fig. 9.7(a).
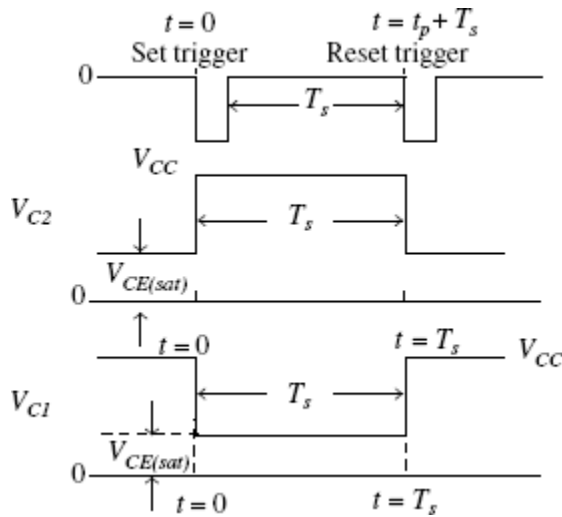
FIGURE 9.6(b) The voltages at the two collectors on the application of trigger pulses
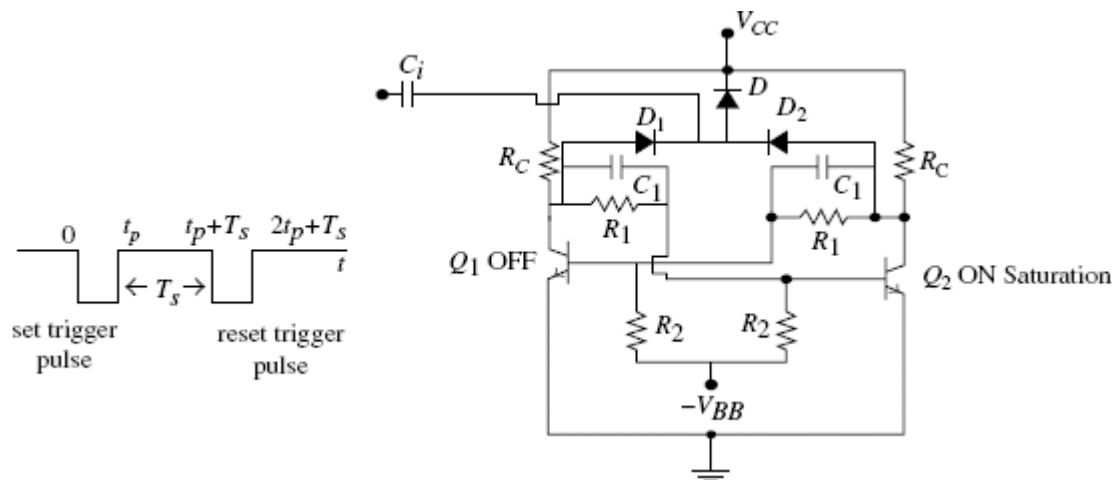
FIGURE 9.7(a) The symmetric triggering of a bistable multivibrator

In the circuit shown in Fig. 9.7(a) the purpose of D is similar to the diodes D_3 and D_4 used in Fig. 9.6(a). The first trigger pulse (Set pulse) makes D_1 conduct and this pulse is coupled to the base of Q_2 and drives Q_2 into the OFF state and Q_1 into the ON state. The next trigger pulse (Reset pulse) applied at $t = t_1$ is coupled to the first base as D_2 is now ON. Hence, Q_1 again goes into the OFF state and Q_2 into the ON state. D_1 and D_2 are called steering diodes as these diodes steer the trigger to the appropriate base.

A bistable multivibrator is represented by a block having a trigger input and the outputs Q and $\overline{Q}$ (collectors of Q_1 and Q_2), as shown in Fig. 9.7(b).

From the above waveforms, it is seen that for every two trigger pulses, there is one pulse at $\overline{Q}$. Hence, a bistable multivibrator is also called a scale-of-two-circuit.
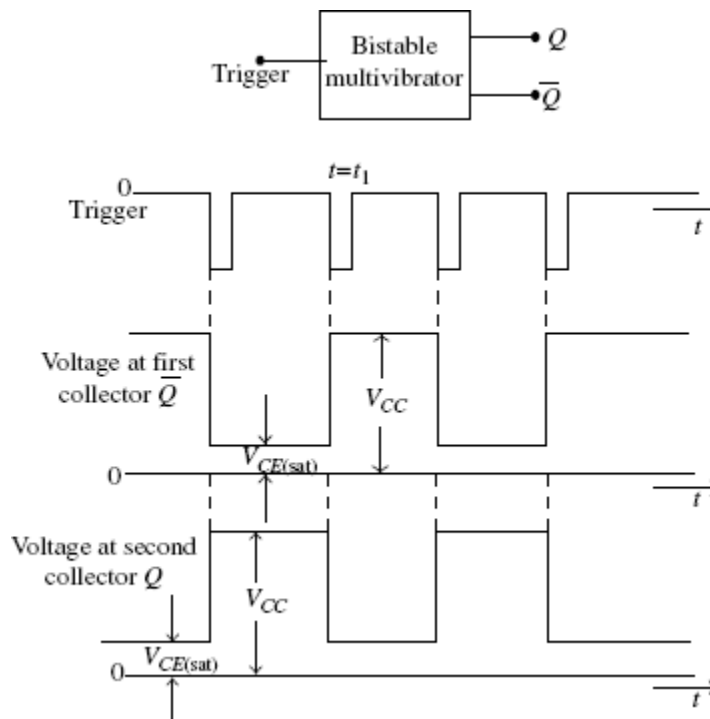
FIGURE 9.7(b) The trigger and outputs with symmetrical triggering of a bistable multivibrator

SCHMITT TRIGGERS

An emitter-coupled bistable multivibrator is also called a Schmitt trigger, named after the designer of the vacuum tube version. In addition to being used as a bistable multivibrator, it has some more important applications.

In the Schmitt trigger circuit shown in Fig. 9.12(a), it is seen that the output of the first transistor is connected to the input of the second transistor through a potential divider network comprising R_1 and R_2. This is simply an attenuator circuit. Normally R_1 and R_2 are reasonably large resistors so as to avoid loading the collector of Q_1. Further, the emitter resistance R_E stabilizes the currents and voltages. Note that the second collector and the first emitter are not involved in the regenerative loop (there is no cross-coupling from the second collector to the first base). So, when used as a bistable multivibrator, there is no loading on the second collector and the trigger is applied at the first base and the output is taken from the second collector.

As long as the battery voltage v_i is small, Q_1 is OFF. The voltage at this collector is approximately V_{CC}. This voltage is coupled to the second base through R_1 and R_2. As a

result, Q_2 can conduct. If Q_2 conducts, it can operate in the active region or it may be driven into saturation.

Let it be assumed that Q_2 is in the active region. The base current I_{B2} and collector current I_{C2} flows through R_E. Therefore, a voltage $V_{EN} = V_{EN2}$ is developed in R_E. As $V_{BE1} = V_{BN1} - V_{EN2}$ and if V_{BE1} reverse-biases the emitter diode of Q_1, then as assumed Q_1 is OFF.

If V_{BN1} (v_i) is increased, at a value ($V_{EN2} + V_{\gamma1}$), Q_1 begins to conduct. As a result, the voltage at the second base decreases, hence the base current of Q_2 decreases, its collector current also reduces and consequently the voltage at the second collector rises. If the input is increased further, Q_1 goes into the ON state and Q_2 into the OFF state. If the loop gain is less than unity (this condition can be satisfied by reducing the collector load of Q_1), there exists a region of linearity in the transfer characteristic. In this region an incremental change at the input Δv_i will cause a proportional change in the output, Δv_o as shown in Fig. 9.12(b). If the loop gain is made equal to 1 by adjusting R_{C1} and R_{C2}, the transfer characteristic is as shown in Fig. 9.12(c).

If on the other hand, the loop gain is made greater than 1, the transfer characteristic is an S-shaped characteristic, as shown in Fig. 9.12(d). When the input is increased from 0 to a larger value, at a voltage V_1, the output suddenly jumps from a smaller value to V_{CC} as shown in Fig. 9.13(a). Even if the input is increased further, the output remains at V_{CC}

If on the other hand, the input is decreased, then at a voltage V_2 the output falls from V_{CC} to a smaller value, as shown in Fig. 9.13(b). If these two curves are combined together, the resultant transfer characteristic, that gives the relation between the input and the output, is shown in Fig. 9.13(c).
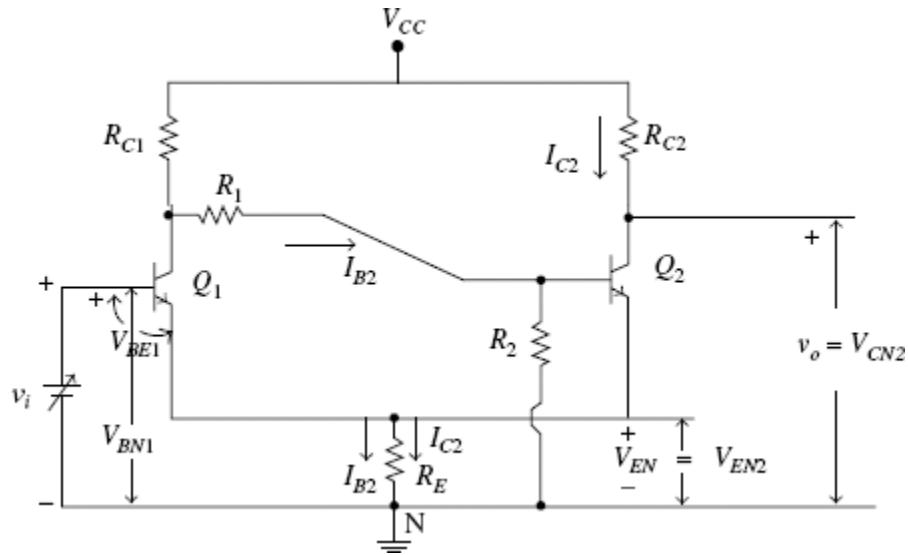
FIGURE 9.12(a) The Schmitt trigger

V_1 is called the upper trip point (UTP) and V_2 is called the lower trip point (LTP). The closed loop in Fig. 9.13(c) is termed the hysteresis loop and the difference in voltages V_1 and V_2 is called the hysteresis voltage, V_H. Thus, $V_H = V_1 - V_2$.

It is seen from the above discussion that a Schmitt trigger exhibits hysterisis, i.e., when the input v_i is increased to reach a voltage V_1 it is required to first pass through a point, V_2 at which the reverse transition takes place. Similarly, when the input now is reduced to reach V_2 it has to pass through the point V_1. This is called hysteresis. This characteristic of the Schmitt trigger is used to an advantage in waveshaping applications.
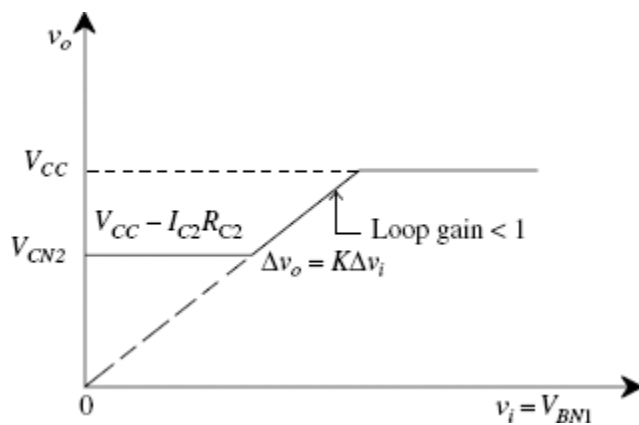
FIGURE 9.12(b) The transfer characteristic of a Schmitt trigger when the loop gain < 1
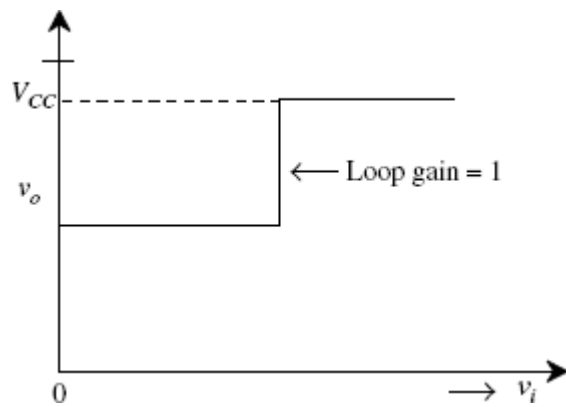
FIGURE 9.12(c) The transfer characteristic of a Schmitt trigger when the loop gain is 1
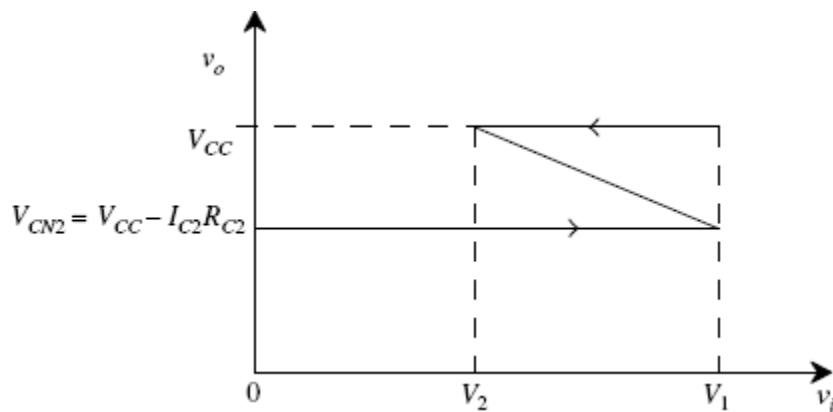
FIGURE 9.12(d) The transfer characteristic of a Schmitt trigger when the loop gains > 1
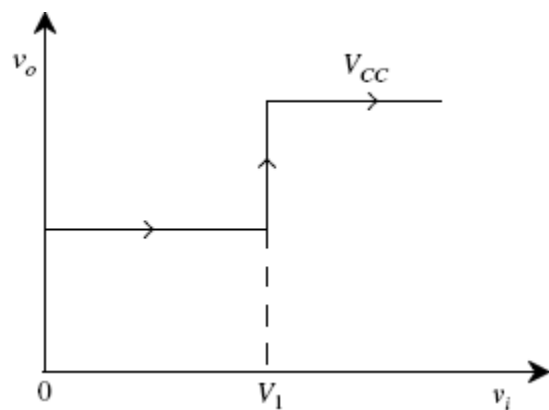
FIGURE 9.13(a) The output rises suddenly to V_{CC}
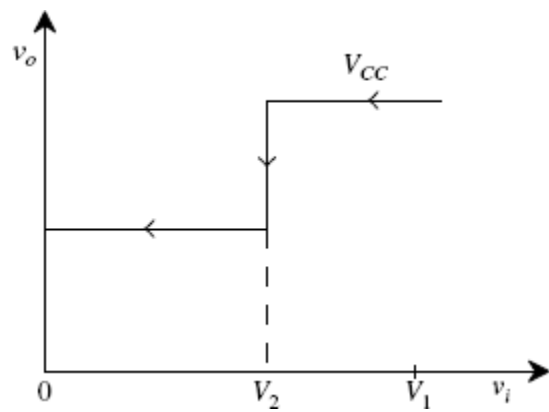
FIGURE 9.13(b) When the input is decreased the output falls from V_{CC}
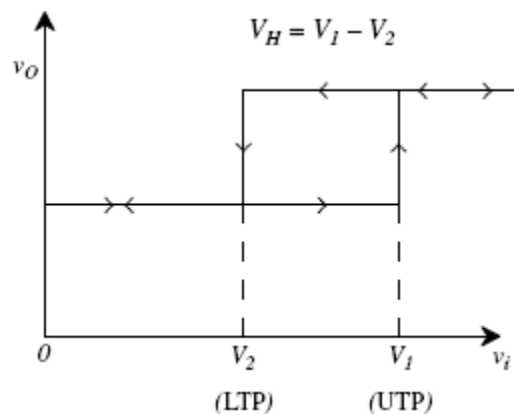
FIGURE 9.13(c) The transfer characteristic of a Schmitt trigger

9.4.1 Calculation of the Upper Trip Point (V_1)
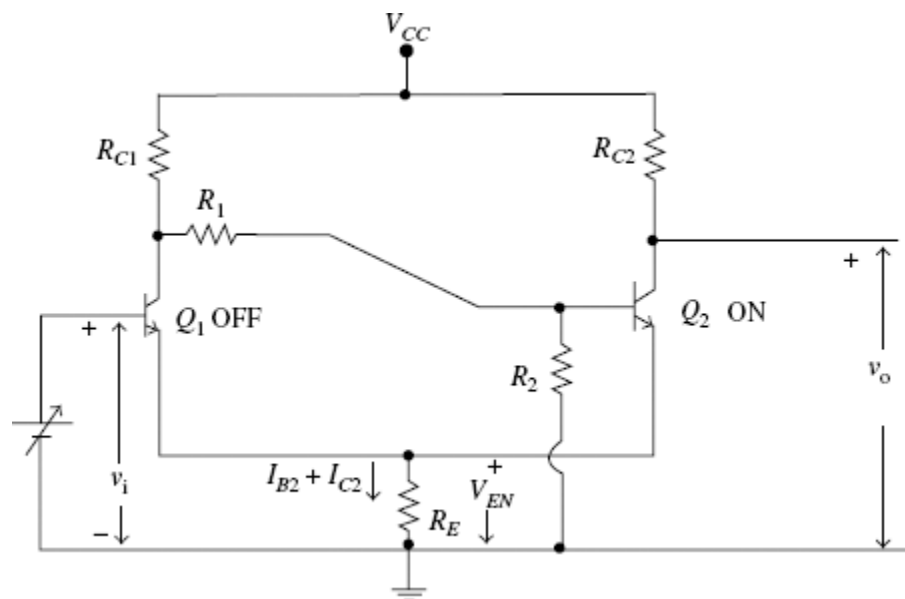
FIGURE 9.14 The Schmitt trigger circuit

In the Schmitt trigger circuit, shown in <u>Fig. 9.14</u>, when the input is increased, till V_1 is reached Q_1 is OFF and Q_2 is ON. As a result, I_{B2} and I_{C2} flow through R_E developing a voltage V_{EN} in R_E. Now, if the input is such that its value is $(V_{EN} + V_{\gamma 1}) = V_1(\text{UTP})$, Q_1 switches into the ON state and Q_2 switches into the OFF state.

If the circuit show in <u>Fig. 9.14</u> is Thévenised at the base of Q_2, the Thévenin voltage source is,

$$V' = V_{CC} \times \frac{R_2}{R_{C1} + R_1 + R_2} \tag{9.55}$$

And its internal resistance R' is given by the relation:

$$R' = R_2 \| (R_{C1} + R_1) \tag{9.56}$$

The resultant simplified circuit is shown in <u>Fig. 9.15(a)</u>.

$$I_{E2} = I_{B2} + I_{C2} = I_{B2}\left(1 + \frac{I_{C2}}{I_{B2}}\right) = I_{B2}(1 + h_{FE}) \tag{9.57}$$
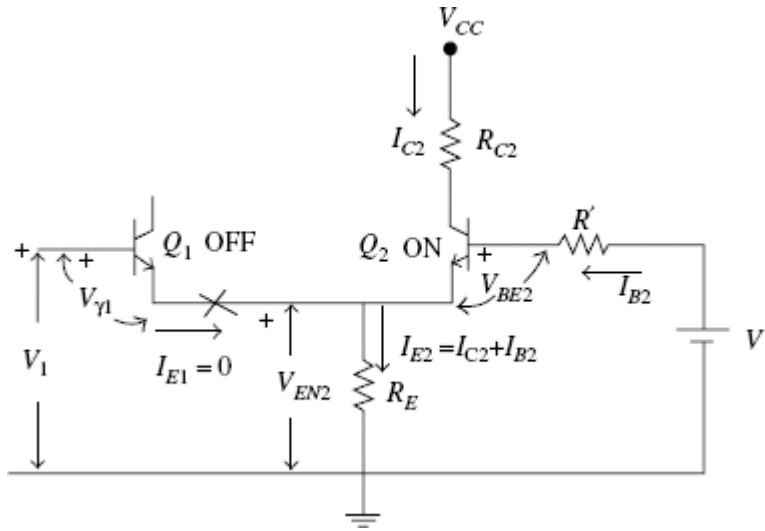
FIGURE 9.15(a) The circuit that enables computation of V_1

The total current in R_E is $I_{B2}(1 + h_{FE})$ and the current in R' is I_{B2}. As far as I_{B2} is concerned, R_E is seen to have increased by a factor $(1 + h_{FE})$. The net voltage in the base loop is, $(V' - V_{BE2})$ and is equal to the sum of the voltage drops across R' and $(1 + h_{FE})R_E$, as shown in <u>Fig. 9.15(b)</u>.

$$\therefore V_{EN2} = (V' - V_{BE2})\frac{R'_E}{R' + R'_E}$$

$$= (V' - V_{BE2})\frac{R_E(1 + h_{FE})}{R' + R_E(1 + h_{FE})} \tag{9.58}$$
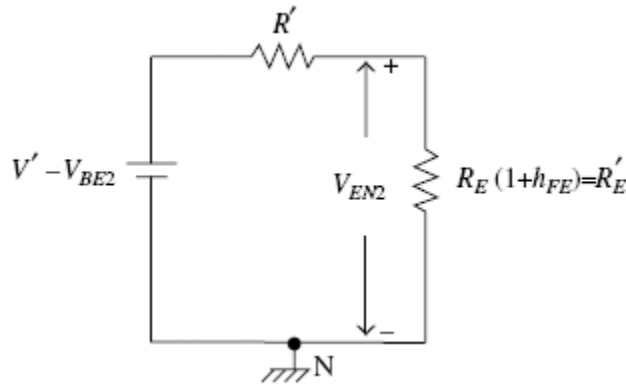
FIGURE 9.15(b) The circuit to calculate V_{EN2}

In Eq. (9.58), as:

$$R' << R_E(1 + h_{FE}) \quad R' + R_E(1 + h_{FE}) \cong R_E(1 + h_{FE})$$

Then Eq. (9.58) reduces to:

$$\therefore V_{EN2} = (V' - V_{BE2})\frac{R_E(1 + h_{FE})}{R_E(1 + h_{FE})} \tag{9.59}$$

$$= V' - V_{BE2} \tag{9.60}$$

From Fig. 9.15(a), using Eq. (9.60):

$$V_1 = V_{EN2} + V_{\gamma_1} \tag{9.61}$$

The calculation of V_1 is made based on the assumption that Q_2 is in the active region. Now, to verify whether Q_2 is in the active region, V_{CB2} is calculated and checked if this reverse-biases the collector diode by a reasonable voltage or not. If it does, the device Q_2 is indeed in the active region.

From the circuit in Fig. 9.15(a), we have:

$$V_{CB2} = V_{CE2} - V_{BE2} \quad \text{and} \quad V_{CE2} = V_{CC} - I_{C2}R_{C2} - V_{EN2}$$

$$\therefore V_{CB2} = V_{CC} - I_{C2}R_{C2} - V_{EN2} - V_{BE2} \tag{9.62}$$

To calculate V_{CB2} using Eq. (9.62), we have to find I_{C2}.

$$V_{EN2} = (I_{B2} + I_{C2})R_E = I_{C2}\left(1 + \frac{1}{h_{FE}}\right)R_E$$

$$V_{EN2} = I_{C2}R_E''$$ (9.63)

where,

$$R_E'' = \left(1 + \frac{1}{h_{FE}}\right)R_E$$ (9.64)

Substituting Eq. (9.63) in Eq. (9.61) we get:

$$V_1 = I_{C2}R_E'' + V_{\gamma 1}$$ (9.65)

where R_E'' is given by Eq. (9.64). From Eq. (9.63) I_{C2} is given as:

$$I_{C2} = \frac{V_{EN2}}{R_E''}$$ (9.66)

These calculations were made based on the assumption that Q_2 is in the active region. Having made the calculations, we once again verify whether Q_2 is really in the active region or not, to justify the validity of the calculations made. V_{CB2} is calculated using Eq. (9.62). If the base–collector diode is reverse-biased, then Q_2 is in the active region as assumed.

Calculation of the Lower Trip Point (V_2)

At the voltage V_1 (UTP), Q_1 is ON and Q_2 is OFF. Now if the input is reduced, till voltage V_2 is reached, Q_1 is ON and Q_2 is still OFF. However, when the voltage at the input is V_2 then the voltage at the second base is $V_{EN1} + V_\gamma 2$. Q_2 again switches into the ON state and Q_1 into the OFF state.

Consider the Schmitt trigger circuit shown in Fig. 9.14. The Thévenin voltage source at the first collector is:

$$V_t = V_{CC}\frac{R_1 + R_2}{R_{C1} + R_1 + R_2}$$ (9.67)

And its internal resistance R_t is,

$$R_t = R_{C1} \,//\, (R_1 + R_2)$$ (9.68)

The first collector and the second base are connected through R_1 and R_2, as shown in Fig. 9.16.

$$\therefore V_{BN2} = V_{CN1}\frac{R_2}{R_1 + R_2} = \alpha V_{CN1}$$ (9.69)

where

$$\alpha = \frac{R_2}{R_1 + R_2} \tag{9.70}$$

$$R_t = \frac{R_{C1}(R_1 + R_2)}{R_{C1} + R_1 + R_2} \tag{9.71}$$

The circuit that enables us to calculate V_2 is shown in Fig. 9.17.

Writing the KVL equation for the base loop of Q_2:

$$\alpha V_{CN1} = V_{\gamma 2} + (I_{B1} + I_{C1}) R_E \qquad V_{CN1} = V_t - I_{C1} R_t$$
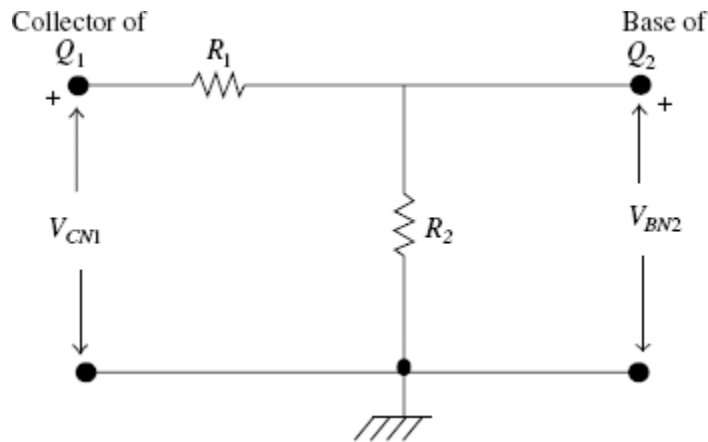
FIGURE 9.16 The coupling network from the first collector to the second base
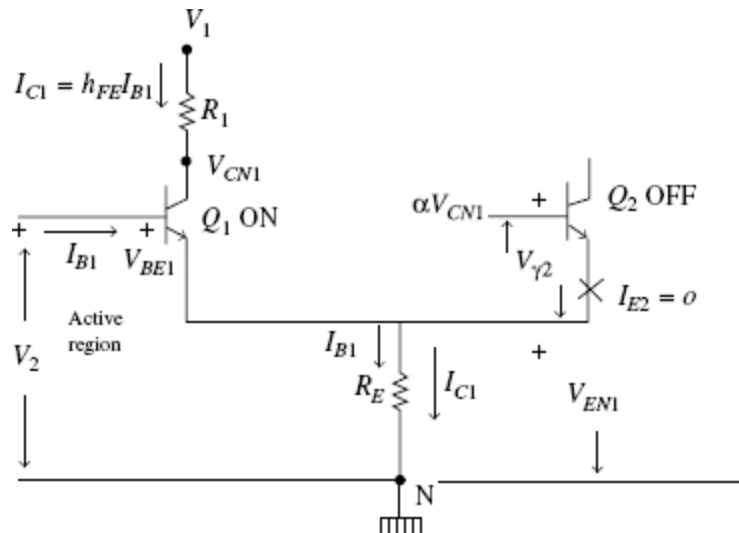
FIGURE 9.17 The circuit to calculate V_2

$$\alpha(V_t - I_{C1}R_t) = V_{\gamma 2} + I_{C1}\left(1 + \frac{1}{h_{FE}}\right)R_E$$

Let:

$$R_E'' = (1 + \frac{1}{h_{FE}})R_E \qquad\qquad (9.72)$$

$$\alpha V_t - I_{C1}\alpha R_t = V_{\gamma 2} + I_{C1}R_E'' \qquad I_{C1}(\alpha R_t + R_E'') = \alpha V_t - V_{\gamma 2}$$

$$I_{C1} = \frac{(\alpha V_t - V_{\gamma 2})}{(\alpha R_t + R_E'')} \qquad\qquad (9.73)$$

However, we have:

$$\alpha V_t = V_{CC}\frac{(R_1 + R_2)}{(R_{C1} + R_1 + R_2)} \times \left(\frac{R_2}{R_1 + R_2}\right) = V_{CC}\frac{R_2}{(R_{C1} + R_1 + R_2)} = V'$$

$$\alpha V_t = V' \qquad\qquad (9.74)$$

Therefore, from Eq. (9.73)

$$I_{C1} = \frac{(V' - V_{\gamma 2})}{(\alpha R_t + R_E'')} \qquad\qquad (9.75)$$

$$V_2 = V_{BE1} + I_{C1}R_E'' \qquad\qquad (9.76)$$

Using Eqs. (9.72), (9.74) and (9.75), V_2 is calculated. To understand the method of calculation for V_1 and V_2, let us consider Example 9.5.

EXAMPLE

Example 9.5: For the Schmitt trigger circuit shown in Fig. 9.18(a), calculate V_1 and V_2.
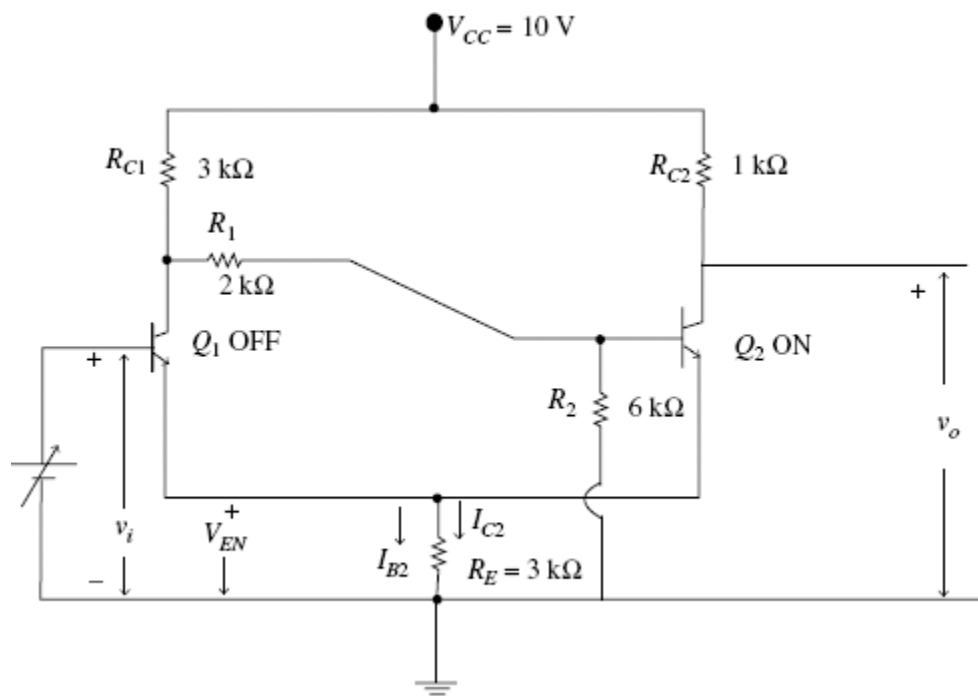
FIGURE 9.18(a) The Schmitt trigger with components mentioned

Solution:

a) Calculation of V_1:

Consider the Schmitt trigger circuit, shown in Fig. 9.18(a). From Eq. (9.55):

$$V' = V_{CC} \times \frac{R_2}{R_{C1} + R_1 + R_2} = 10 \times \frac{6}{3 + 2 + 6} = 5.45 \text{ V}$$

R' the internal resistance of this Thévenin source, as given by Eq. (9.56), is:

$$R' = R_2 // (R_{C1} + R_1) = 6 // (3 + 2) = \frac{6 \times 5}{6 + 5} = 2.73 \text{ k}\Omega$$

The resultant circuit is shown in Fig. 9.18(b).
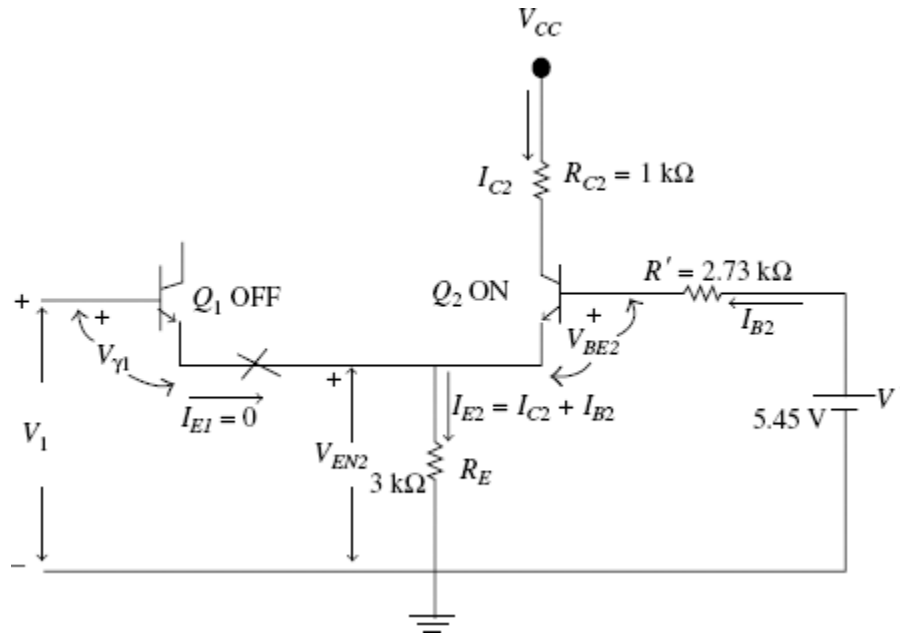
FIGURE 9.18(b) The circuit that enables computation of V_1

From Eq. (9.58):

$$V_{EN2} = (V' - V_{BE2}) \frac{R_E(1 + h_{FE})}{R' + R_E(1 + h_{FE})}$$

If Q_2 is in the active region, typically, for silicon V_{BE2} = 0.6 V and let h_{FE} = 50,

$R_E(1 + h_{FE})$ = 3(1 + 50) = 153 kΩ

Therefore,

$$V_{EN2} = (5.45 - 0.6) \times \frac{153}{2.73 + 153} = 4.85 \times \frac{153}{155.73} = 4.76 \text{ V}$$

Therefore,

$V_1 = V_{EN2} + V_{BE2}$ = 4.76 + 0.6 = 5.36 V.

The calculation of V_1 is made based on the assumption that Q_2 is in the active region. To find out whether Q_2 is in the active region or not, we calculate V_{CB2}.

$V_{CB2} = V_{CC} - I_{C2}R_{C2} - V_{EN2} - V_{BE2}.$

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From <u>Eq. (9.72)</u>

$$R_E'' = (1 + \frac{1}{h_{FE}})R_E = (1 + \frac{1}{50})3 = \frac{51}{50} \times 3 = 3.06\,\text{k}\Omega$$

Hence

$$I_{C2} = \frac{V_{EN2}}{R_E''} = \frac{4.76\,\text{V}}{3.06\,\text{k}\Omega} = 1.56\,\text{mA}$$

$$V_{CB2} = 10 - (1.56 \times 1) - 4.76 - 0.6 = 10 - 6.92 = 3.08\,\text{V}$$

As the collector of Q_2 is positive with respect to the base by 3.08 V the collector diode is reverse-biased. Hence, Q_2 is in the active region, as assumed.

(b) Calculation of V_2:

The circuit that enables us to calculate V_2 is shown in <u>Fig. 9.18(c)</u>. From the circuit values:

$$\alpha = \frac{R_2}{R_1 + R_2} = \frac{6}{2+6} = 0.75 \qquad R_t = \frac{3(2+6)}{3+2+6} = \frac{24}{11} = 2.18\,\text{k}\Omega$$

$$\alpha R_t = 0.75 \times 2.18\,\text{K} = 1.64\,\text{k}\Omega \qquad R_E'' = 3.06\,\text{k}\Omega \qquad V_2 = V_{BE1} + I_{C1}R_E''$$

$$I_{C1} = \frac{(V' - V_{\gamma 2})}{\alpha R_t + R_E''} = \frac{(5.45 - 0.5)}{1.64 + 3.06} = \frac{4.95}{4.7} = 1.05\,\text{mA}$$

$$\therefore V_2 = 0.6\,\text{V} + (1.05\,\text{mA})(3.06\,\text{k}\Omega) = 0.6\,\text{V} + 3.22\,\text{V} = 3.82\,\text{V}$$

Hence, for the given Schmitt trigger:

$$V_1 = 5.36\,\text{V} \quad V_2 = 3.82\,\text{V} \quad V_H = V_1 - V_2 = 5.36 - 3.82 = 1.54\,\text{V}$$
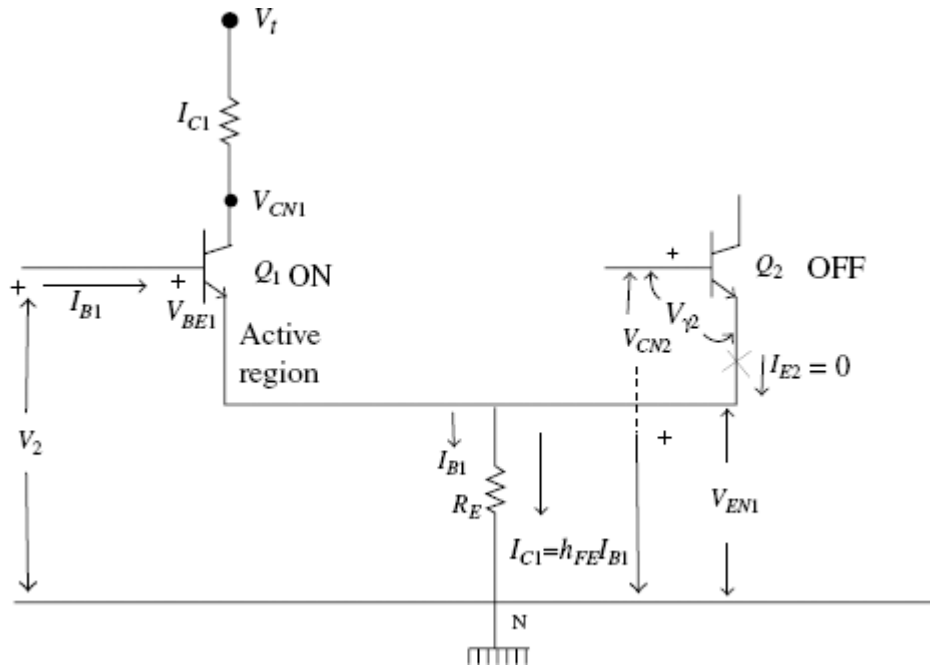
FIGURE 9.18(c) The circuit to calculate V_2

Methods to Eliminate Hysteresis in a Schmitt Trigger

It is evident from Fig. 9.13(c), that hysteresis is present in a Schmitt trigger because the loop gain is not exactly unity, but is greater than 1. Hysteresis is needed when a schmitt trigger used as a histable multitrigger and also when converting a time-varying signal into a square wave. But when it used as a comparator, hysteresis needs to be elimimated. The following schemes can be implemented to eliminate hysteresis in a Schmitt trigger:

1. V_1 and V_2 are made to coincide with the proper choice of R_1 and R_2. However, by this method, though, it is not possible to make V_1 identical to V_2, they can be brought close to each other in practice.

2. Another method to eliminate hysteresis is by introducing a resistance R_{e2} in series with the emitter terminal of Q_2, as shown in Fig. 9.19(a).

R_{e2} will change V_1, but has no effect on V_2. Therefore, by including R_{e2} in series with the emitter of Q_2, it is possible to reduce V_1 to the level of V_2,(V_1 is made equal to V_2), thereby reducing hysteresis. The method to calculate R_{e2}, for the circuit shown in Fig. 9.19(b), calculate V' and R' as illustrated in Section 9.4.1, as shown in Fig. 9.15(a).

From Fig. 9.19(b), we have:

$$V_{EN} = V_{EN2} = (V' - V_{BE2})\frac{(1 + h_{FE})R_E}{R' + (1 + h_{FE})(R_{e2} + R_E)} \tag{9.77}$$

And $V_1 = V_{EN2} + V_{\gamma1} = (V' - V_{BE2})\dfrac{(1 + h_{FE})R_E}{R' + (1 + h_{FE})(R_{e2} + R_E)} + V_{\gamma1}$ $\qquad$ (9.78)
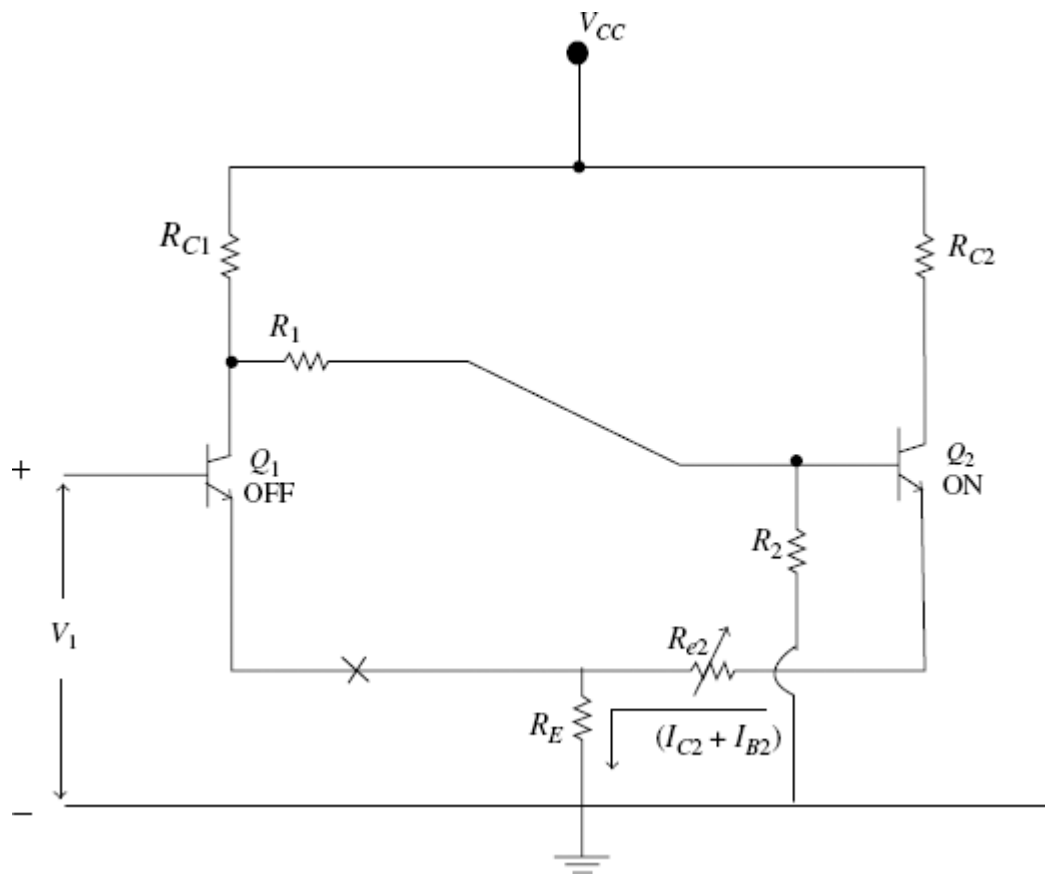
FIGURE 9.19(a) An alternate method to eliminate hysteresis
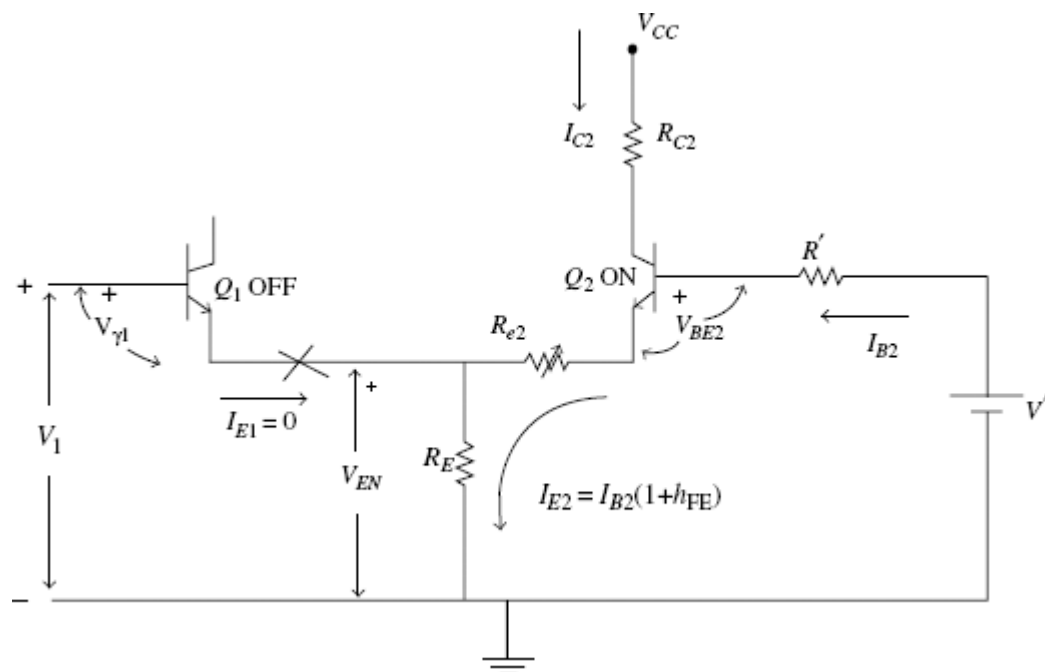
FIGURE 9.19(b) The circuit to calculate R_{e2}

To eliminate hysteresis, V_1 should be made equal to V_2, which means that in <u>Eq. (9.78)</u> V_1 is replaced by V_2

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$$(V' - V_{BE2})\frac{(1 + h_{FE})R_E}{R' + (1 + h_{FE})(R_{e2} + R_E)} + V_{\gamma 1} = V_2 \qquad (9.79)$$

R_{e2} that eliminates hysteresis is calculated using Eq. (9.79). To further understand the procedure let us consider Example 9.6.

EXAMPLE

Example 9.6: From the problem in Example 9.5, we have V_1 = 5.36 V, V_2 = 3.82 V, V' = 5.45 V, R' = 2.73 kΩ, R_E = 3kΩ, h_{FE}= 50, V_{BE2} = 0.6 V. Find the value of R_{e2} that ensures V_1 = V_2 = 3.82 V and eliminates hysteresis.

Solution: We have from Eq. (9.79):

$$(V' - V_{BE2})\frac{(1 + h_{FE})R_E}{R' + (1 + h_{FE})(R_{e2} + R_E)} + V_{\gamma 1} = V_2$$

$$(5.45 - 0.6)\frac{(1 + 50)3}{2.73 + (1 + 50)(R_{e2} + 3)} + 0.5 = 3.82$$

$$\frac{742.05}{155.73 + 51\,R_{e2}} + 0.5 = 3.82$$

Therefore,

$$R_{e2} = \frac{742.05 - 517.02}{169.32} = \frac{225.03}{169.32} = 1.33\ \text{k}\Omega$$
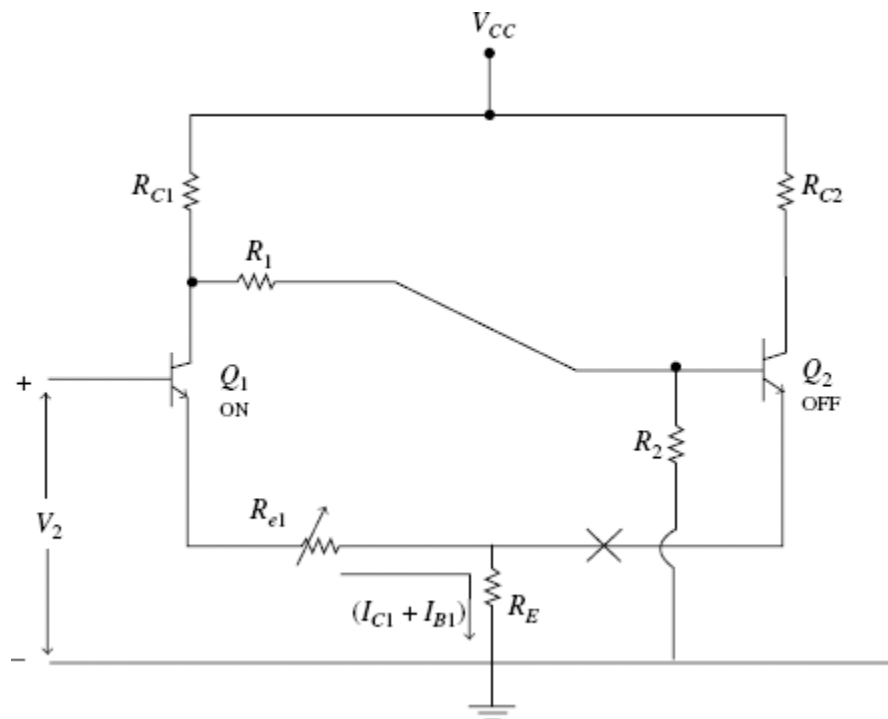
FIGURE 9.19(c) Another method to eliminate hysteresis

(iii) Another method to eliminate hysteresis is to introduce a resistance R_{e1} in series with the emitter terminal of Q_1, as shown in Fig. 9.19(c).

R_{e1} is not going to change V_1 but will only influence V_2. To eliminate hysterisis, R_{e1} is chosen such that V_2 is increased to the level of V_1. To achieve this, we must ensure that V_2 plus the voltage drop across R_{e1} is V_1.

$$V_1 = V_2 + R_{e_1}(I_{C1} + I_{B1}) \tag{1}$$

From Eq. (1):

$$R_{e1} = \frac{V_1 - V_2}{I_{C1} + I_{B2}} = \frac{V_H}{I_{C1} + I_{B1}} \tag{2}$$

$$I_{C1} + I_{B1} = I_{C1}\left(1 + \frac{1}{h_{FE}}\right) = I_{C1}\frac{(1 + h_{FE})}{h_{FE}} \tag{3}$$

Substituting Eq. (3) in Eq. (2), we get:

$$R_{e1} = \frac{V_H}{I_{C1}} \times \frac{h_{FE}}{(1 + h_{FE})} \tag{4}$$

To understand the procedure to calculate R_{e1}, let us consider an example.

Example 9.7: From the problem in <u>Example 9.5</u>, we have $V_1 = 5.36$ V, $V_2 = 3.82$ V, $I_{C_1} = 1.05$ mA, $h_{FE} = 50$. Find the value of R_{e_1}.

Solution:

Using <u>Eq. (9.83)</u>,

$$R_{e_1} = \frac{(5.36 - 3.82)}{1.05} \times \frac{50}{51} = 1.43 \,\text{k}\Omega.$$

9.4.4 Applications of a Schmitt Trigger

The following are some applications of a Schmitt trigger:

(a) An emitter-coupled bistable multivibrator is called the Schmitt trigger. Hence, a Schmitt trigger can be used as a bistable multivibrator. Consider the transfer characteristic, shown in <u>Fig. 9.20(a)</u>.

To use this circuit as a bistable multivibrator, the first device Q_1 is biased to have a voltage V at its base. Initially, let the output be at 0 level ($V_{CC} - I_{C_2}R_{C_2}$). To change this to 1(V_{CC}) apply a positive pulse at the base of Q_1, whose magnitude is more positive than ($V_1 - V$) as shown in <u>Fig. 9.20(b)</u>.

To once again change the output to a 0 level, apply a pulse at the base of Q_1, which is negative with respect to V and whose magnitude is more negative than ($V_2 - V$) as shown in <u>Fig. 9.20(c)</u>.

(b) A Schmitt trigger can be used as an amplitude comparator. In an amplitude comparator, the amplitude of a time varying signal is compared with a reference and it tells us the time instant at which the input has reached this set reference level. For example, consider the diode comparator circuit shown in <u>Fig. 9.21(a)</u>. As long as $v_i < V_R$, D is OFF and $v_o = v_i$. When $v_i \geq V_R$, D is ON and $v_o = V_R$.
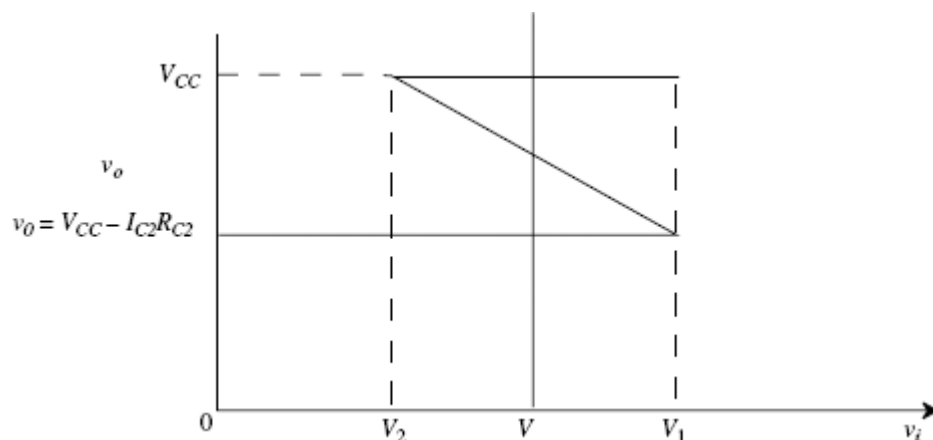
FIGURE 9.20(a) The transfer characteristic of a Schmitt trigger
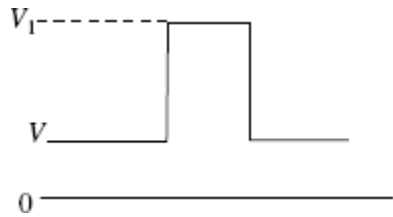
FIGURE 9.20(b) The trigger to change the output from 0 to 1 level
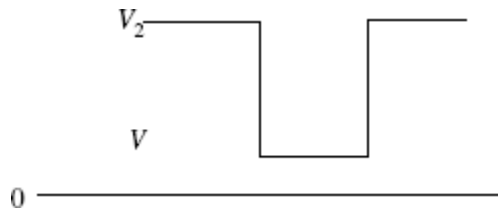
FIGURE 9.20(c) The trigger to change the output from 1 to 0 level
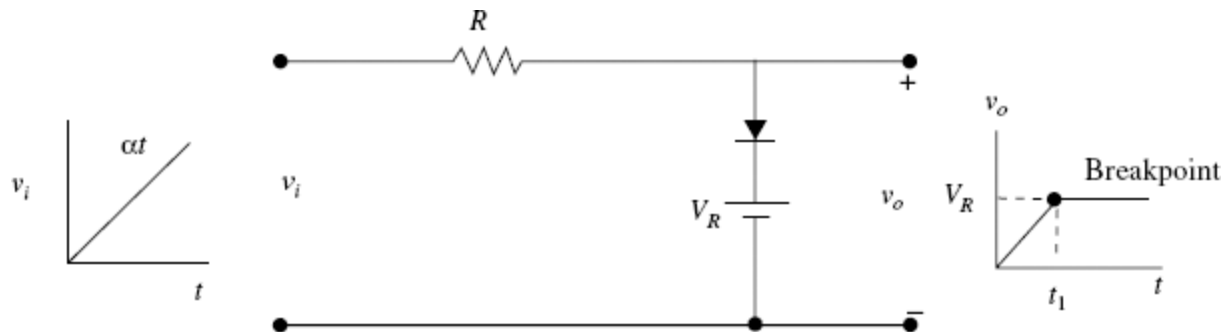
FIGURE 9.21(a) A diode comparator

The output follows the input till $t = t_1$ and then the slope of the output abruptly changes. This is called the break point, and t_1 is the time instant at which v_i has reached V_R.

Now consider the Schmitt trigger (in which hysteresis is eliminated) as a comparator with input and output shown in Fig. 9.21(b). A relatively small dc voltage is there at the output till $V_1(= V_2)$ is reached at the input. The moment the input is V_1, the output abruptly jumps to V_{CC}. The slope of the input has no relation to the slope of the signal at the output. Thus, a Schmitt trigger can be used as a better amplitude comparator.

(c) A Schmitt trigger can be used as a waveshaping circuit (or a squaring circuit). It can be used to convert any arbitrarily time varying signal into a square-wave output. The only condition to be satisfied is that the input signal has amplitude more than V_1 and also less than V_2. Consider the input for which the output is plotted as shown in Fig. 9.22.
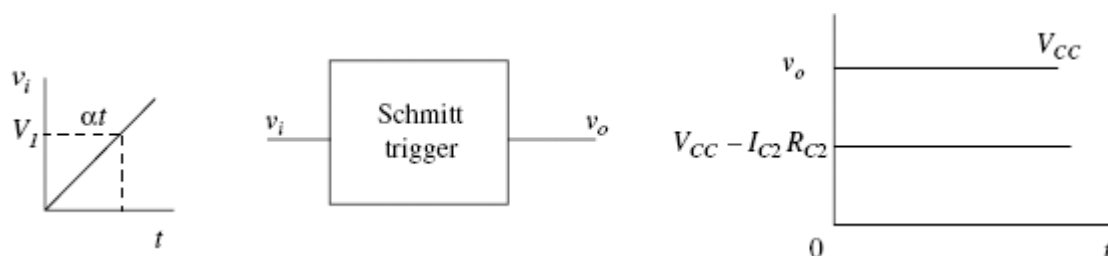
FIGURE 9.21(b) A Schmitt trigger as comparator
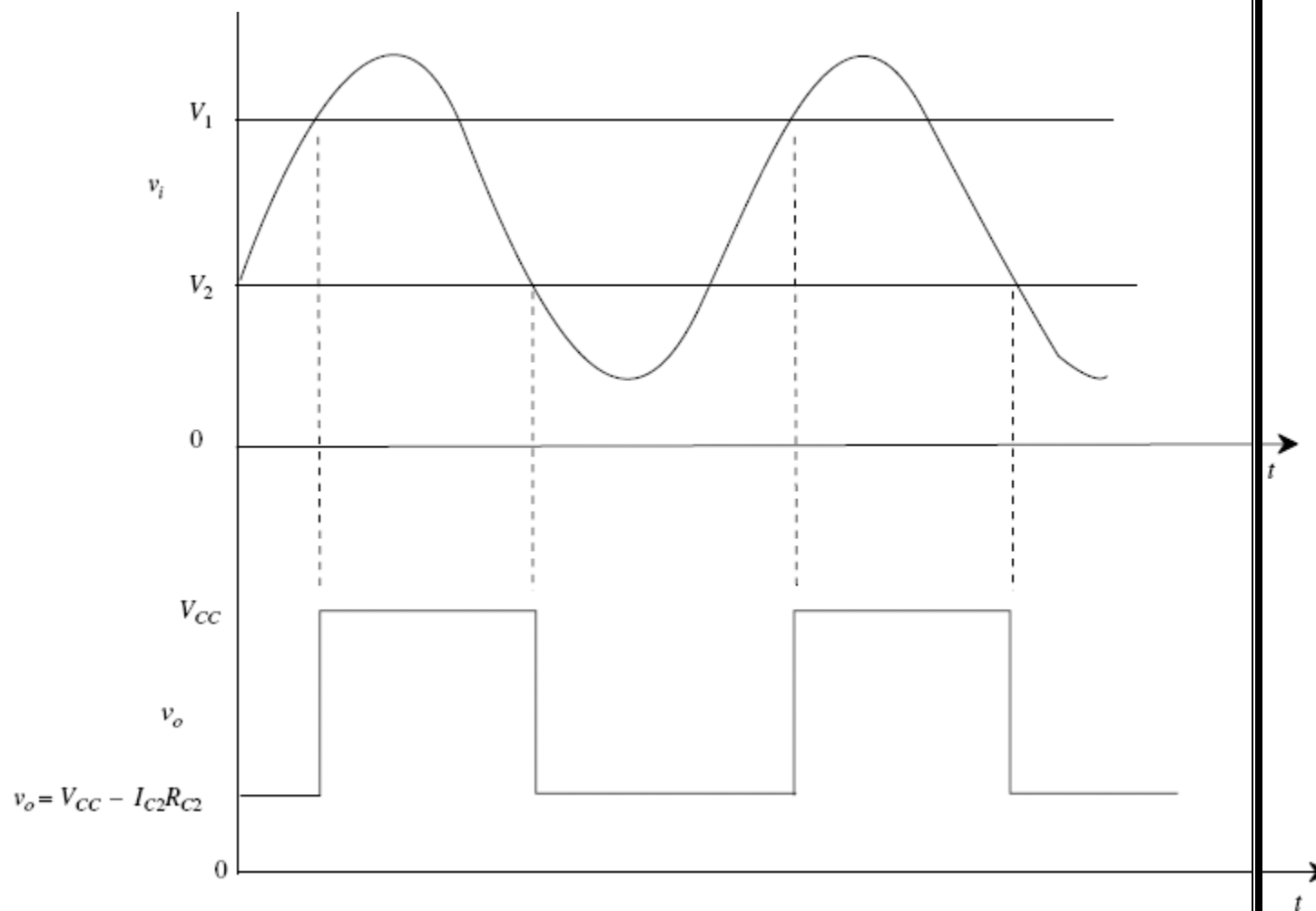
FIGURE 9.22 The Schmitt trigger as a squaring circuit
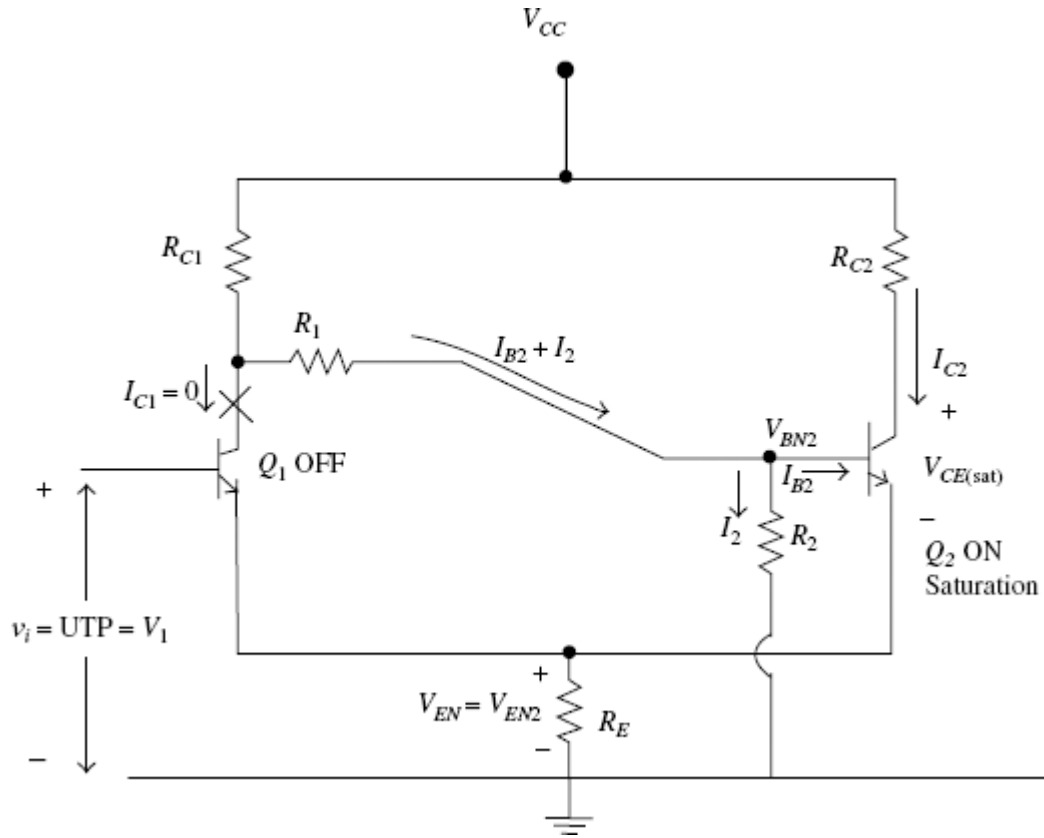
FIGURE 9.23(a) A Schmitt trigger circuit

The Design of a Schmitt Trigger

In this section, the procedure to design a Schmitt trigger is presented. For designing the Schmitt trigger shown in <u>Fig. 9.23(a)</u>, UTP (V_1) and LTP (V_2) values, h_{FE}, desired I_C and V_{CC} are to be specified.

(a) Till UTP is reached Q_1 is OFF and Q_2 is ON and in saturation. Just at V_1 (UTP), Q_1 goes ON and Q_2 goes OFF.

Therefore, $V_1 = \text{UTP} = V_{BN2}$ and $I_E = I_C$ is specified. Therefore:

$$R_E = \frac{V_1 - V_{BE2}}{I_E} \tag{9.80}$$

R_E is chosen using <u>Eq. (9.80)</u>. If Q_2 is in saturation, $V_{CE} = V_{CE(sat)}$. From the circuit shown in <u>Fig. 9.23(a)</u>, we have $I_{C2}R_{C2} = V_{CC} - V_{CE(sat)} - V_{EN2}$

Therefore,

$$R_{C2} = \frac{V_{CC} - V_{CE(sat)} - V_{EN2}}{I_{C2}} \tag{9.81}$$

R_{C2} is calculated using Eq. (9.81).

Assume that

$$I_2 = \frac{I_{C2}}{10} \qquad\qquad (9.82)$$

Using Eq. (9.82):

$$R_2 = \frac{V_{BN2}}{I_2} = \frac{V_1}{I_2} \qquad\qquad (9.83)$$

Using the value of h_{FE} specified, we can now calculate $I_{B2(min)}$ as:

$$I_{B2(min)} = \frac{I_{C2}}{h_{FE}} \qquad (9.84)$$

For Q_2 to be in saturation $I_{B2(sat)}$ must be larger than $I_{B2(min)}$, choose

$$I_{B2(sat)} = 1.5 \times I_{B2(min)} \qquad (9.85)$$

Using Eq. (9.82) and (9.85), we can calculate $(I_2 + I_{B2})$.

From the circuit shown in Fig. 9.23(a):

$$R_{C1} + R_1 = \frac{V_{CC} - V_{BN2}}{I_2 + I_{B2}} = R \qquad (9.86)$$

R is calculated using Eq. (9.86).

$$R_1 = R - R_{C1} \qquad\qquad (9.87)$$

R_1 is chosen using Eq. (9.87).
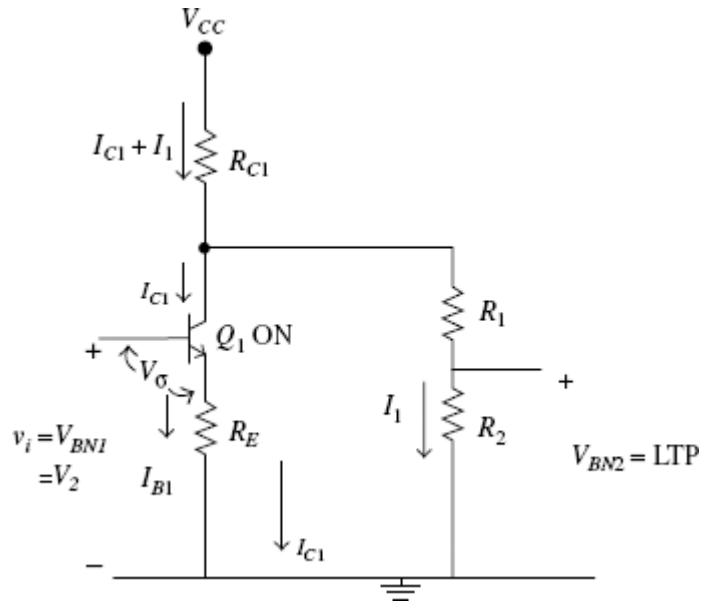
FIGURE 9.23(b) The circuit at LTP

(b) At LTP = V_2, consider the circuit shown in <u>Fig. 9.23(b)</u>.

$V_{BN2} = V_{BN1} = \text{LTP} = V_2$

Let I_1 be the current in R_2,

$$I_1 = \frac{V_{BN2}}{R_2} = \frac{V_2}{R_2} \qquad\qquad (9.88)$$

$$I_{C1} = I_{E1} = \frac{V_2 - V_\sigma}{R_E} \qquad\qquad (9.89)$$

Writing the KVL equation of the outer loop consisting of R_{C1}, R_1 and R_2:

$V_{CC} = (I_{C1} + I_1)R_{C1} + I_1(R_1 + R_2)$

Using <u>Eq. (9.87)</u>:

$V_{CC} = (I_{C1} + I_1)R_{C1} + I_1(R - R_{C1} + R_2)$

Therefore,

$$V_{CC} = I_{C1}R_{C1} + I_1(R + R_2) \qquad\qquad (9.90)$$

From <u>Eq. (9.90)</u>,

$$R_{C1} = \frac{V_{CC} - I_1(R + R_2)}{I_{C1}} \qquad\qquad (9.91)$$

R_{C1} is calculated using Eq. (9.95),

$R_1 = R - R_{C1}$

Monostable Multivibrators

INTRODUCTION

A monostable multivibrator is one in which there is a stable state and a quasi-stable state. This circuit has two devices Q_1 and Q_2, one being in the OFF state, say Q_1, and the other, Q_2, in the ON state—preferably in saturation. These devices remain in this state forever and only on the application of a trigger, the multivibrator goes into the quasi-stable state, i.e., Q_1 is ON and Q_2 is OFF. After a time interval T, the multivibrator will return to the stable state, i.e., Q_1 is OFF and Q_2 is ON. Thus, this circuit generates a pulse of duration T. Let us consider two types of monostable multivibrators:

1. Collector-coupled monostable multivibrator
2. Emitter-coupled monostable multivibrator

The output of this circuit is a pulse of time duration, T called the pulse duration, pulse width or gate width. Some other circuits can also be controlled with the help of this output for a finite time duration. Its main application is as a gate

COLLECTOR-COUPLED MONOSTABLE MULTIVIBRATORS

The collector-coupled monostable multivibrator is shown in <u>Fig. 8.1</u>. When compared to an astable multivibrator as shown in <u>Fig. 7.1</u>, it is evident that the output from the second collector to the first base is through a resistance R_1. Hence, this circuit has one stable state and one quasi-stable state.

As a negative voltage is connected to the base of the first device, it is possible that Q_1 may be OFF. In the stable state, let Q_1 be OFF and Q_2 be ON and in saturation. Therefore:

$$V_{C_1} = V_{CC} \quad V_{C_2} = V_{CE(\text{sat})} \quad V_{B_2} = V_{BE(\text{sat})} = V_\sigma$$

The capacitor, C now tries to charge to V_{CC} through R_C of Q_1 and a small input resistance of Q_2, as shown in <u>Fig. 8.2</u>. As $t \to \infty$, this voltage reaches V_{CC}. To change the state of the devices, a trigger is applied at an appropriate point in the circuit.
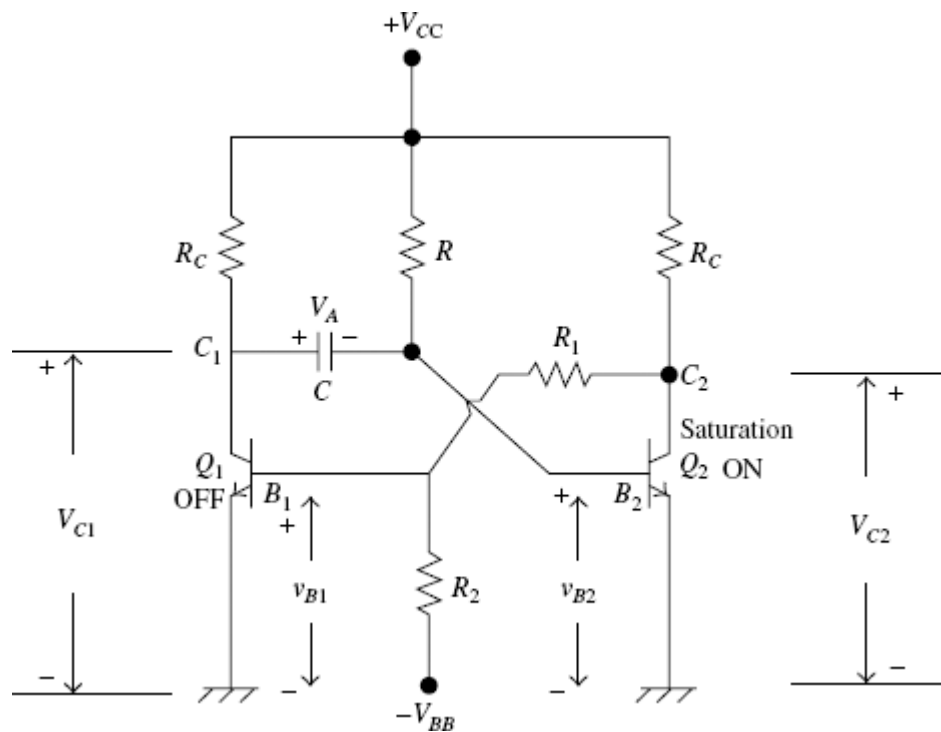
FIGURE 8.1 The collector-coupled monostable multivibrator
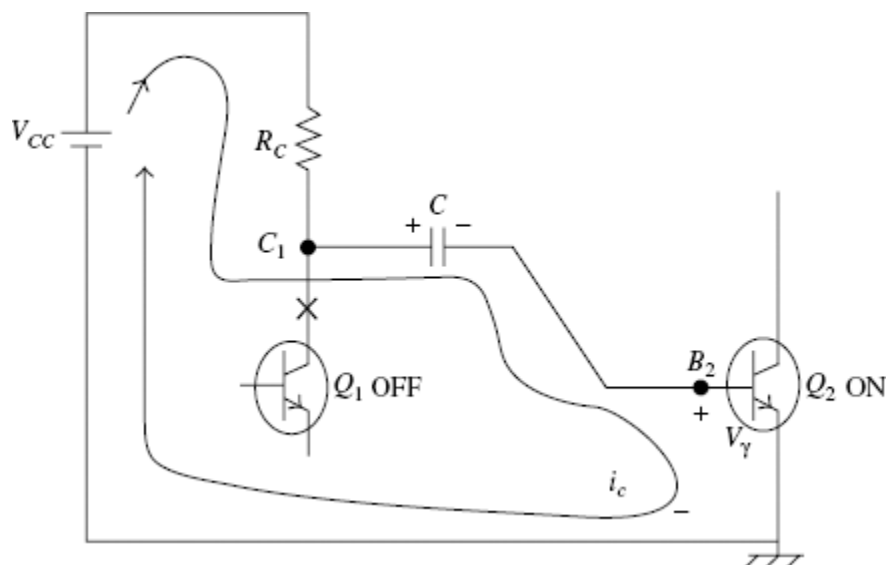
FIGURE 8.2 The charging of capacitor C

Triggering a Monostable Multivibrator

A trigger is a sharp positive or negative pulse of desired amplitude. A negative pulse may be applied at the base of the ON device to drive it into the OFF state or a positive pulse may be applied at the base of the OFF device to drive it into the ON state, as the devices used here are $n–p–n$ devices. When a negative trigger is applied to drive an ON device into the OFF state, the instant the trigger is present; the base current of the device begins to reduce. However, when a positive trigger is applied to drive an OFF device into the ON state, the device will not draw any current till the amplitude of the pulse is V_γ. Thus, it is always preferable to drive an ON device into the OFF state rather than trying to drive an OFF device into the ON state, unless warranted otherwise. Obviously, the triggering sensitivity (ability to change state with a smaller pulse) is better if an ON device is driven into the OFF state rather than applying the other option. Therefore, we now try to drive Q_2 into the OFF state by the application of a negative pulse at the base of Q_2, which is ON and in saturation. The input resistance of Q_2 is very small and hence, loads the trigger source. To avoid loading, the trigger may be applied as shown in <u>Fig. 8.3</u>.

The negative trigger, to drive Q_2 OFF is now applied at the collector of Q_1 through C_i and diode D_1—which conducts only for negative trigger pulses. R_d is the resistance returned to V_{CC}, which is the input resistance offered by the circuit to the trigger source. If R_d is small, it loads the trigger source. Therefore, here, R_d will have to be large. However, when D_1 is ON, charge is built up on the condenser C_i, which should be quickly removed before the application of the next trigger pulse; thus, R_d should be small on this count. A single resistance cannot satisfy both these conflicting requirements. Hence, in place of the resistance R_d, D_2 is connected, which satisfies both the requirements. When the trigger signal is present, D_2 is OFF and offers large input resistance to the trigger source. When the trigger signal is not there, D_2 conducts, offering negligible resistance so that the accumulated charge on condenser C_i is quickly removed. As C is connected between the first collector and second base, the trigger signal is instantaneously connected to B_2.

Calculation of the Time Period (T)

On the application of a trigger at $t = 0$, with a negative pulse at B_2, Q_2 goes into the OFF state and Q_1 is driven into the ON state and preferably into saturation. Hence, there is a current I_1 in Q_1. V_{C1} is $V_{CE(sat)}$, if $I_1 = I_{C(sat)}$, as shown in Fig. 8.4(a).

The charge on the capacitor C now decays with a time constant $\tau = RC$, as shown in Fig. 8.4(b). Consequently, the voltage at B_2 changes as a function of time and this voltage, V_{B2} at B_2, reaches V_γ after a time interval T. The moment the voltage at B_2 is once again V_γ, Q_2 has a small base current, which in turn gives rise to collector current. Earlier the voltage at this collector was V_{CC} as Q_2 was OFF. Due to this collector current, the voltage at the collector of Q_2 falls, giving rise to a negative step. This negative step is coupled to the base of Q_1 through R_1 and R_2 and thus, the base current of Q_1 reduces, reducing its collector current. The voltage at the first collector now rises (earlier it was $V_{CE(sat)}$), resulting in a positive step. This change in voltage is coupled to the second base, increasing its base current further. As the collector current increases, the voltage at this collector reduces; this change in the voltage is once again coupled to the first base, reducing its base current further. Its collector current is now reduced, giving rise to a further increase in the voltage at the first collector, which once again is coupled to the second base. It is observed that regeneration takes place and Q_2 is switched ON and $Q_1$is switched OFF, thus ending the quasi-stable state (also look at the voltage variation at B_2 of Q_2 shown in Fig. 8.5).
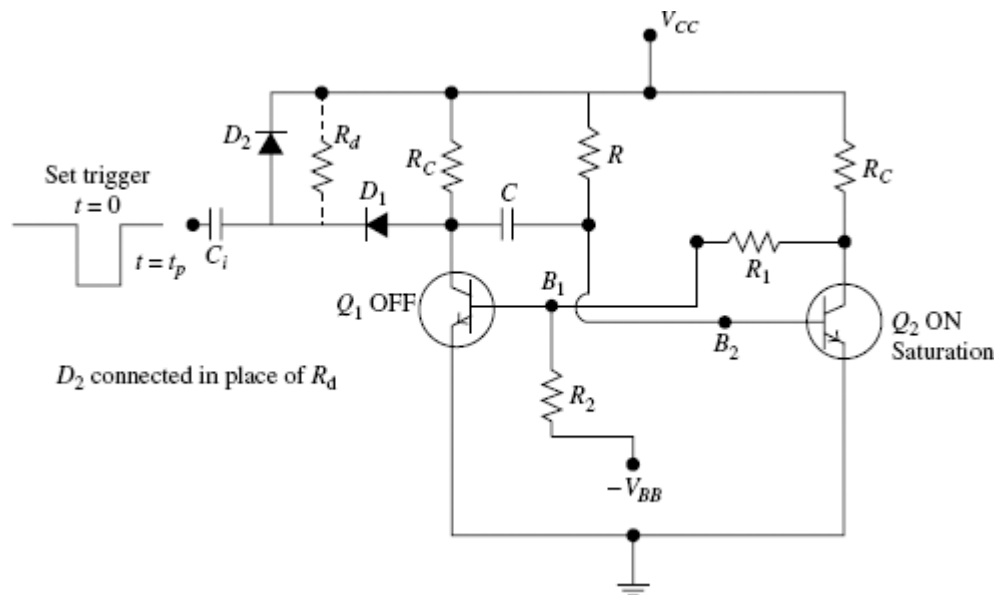
FIGURE 8.3 The triggering of a monostable multivibrator
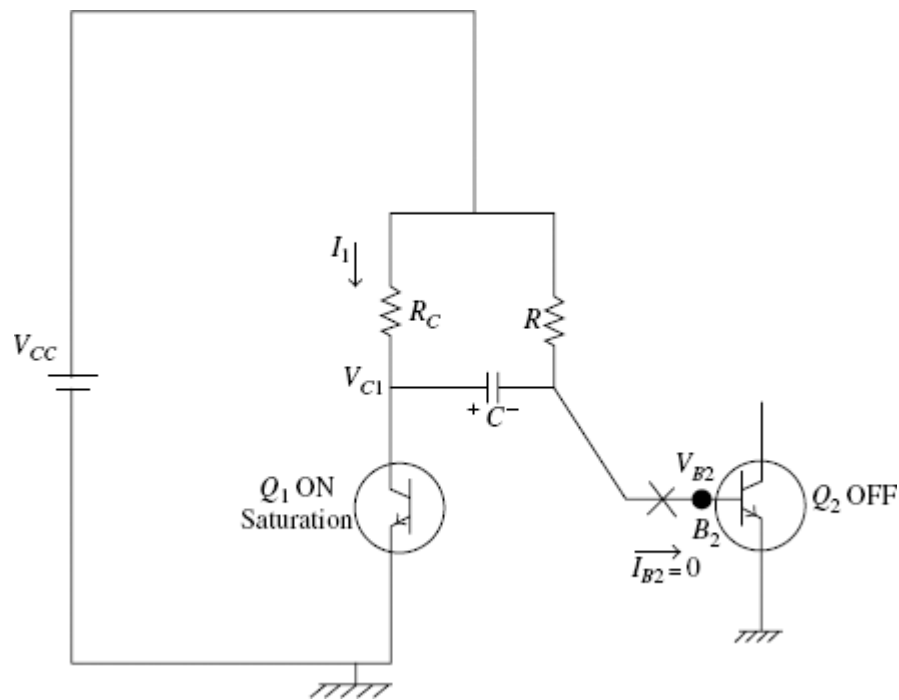
FIGURE 8.4(a) When Q_1 is ON, in the quasi-stable state
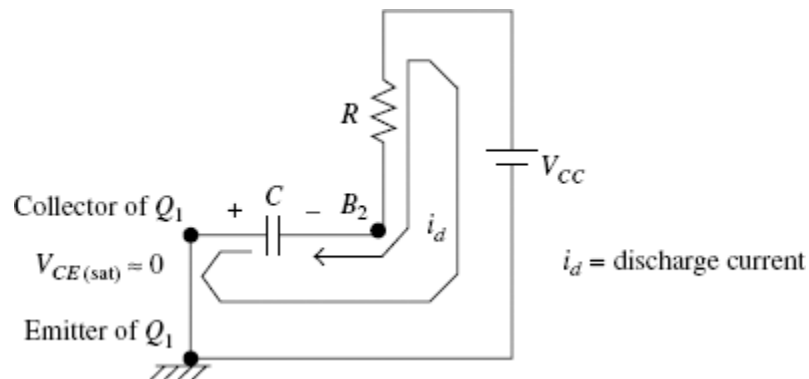
FIGURE 8.4(b) Discharge of C
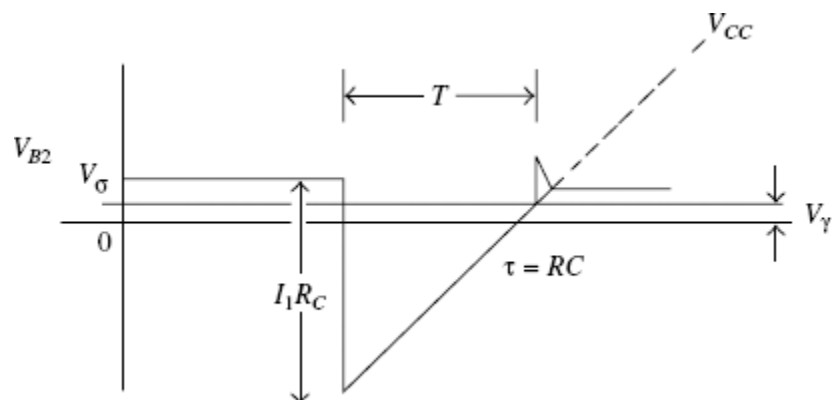
FIGURE 8.5 The voltage variation at the base of Q_2, in the quasi-stable state

We have from Eq. (7.1),

$_{B2}(t) = v_f - (v_f - v_i)e^{-t/\tau}$

Here, $v_f = V_{CC}$, and if Q_1 is in saturation,

$v_i = V_\sigma - I_1 R_C = V_\sigma - [V_{CC} - V_{CE(sat)}] = V_\sigma - V_{CC} + V_{CE(sat)}$

and the time constant, $\tau = RC$

Using Eq. (7.1)

$$V_{B2}(t) = V_{CC} - [V_{CC} - V_\sigma + V_{CC} - V_{CE(sat)}]e^{-t/\tau} \qquad (8.1)$$

However, at $t = T$, $V_{B2}(t) = V_\gamma$

$$V_\gamma = V_{CC} - [2V_{CC} - (V_\sigma + V_{CE(sat)})]e^{-T/\tau_1}$$

As $\dfrac{V_\sigma + V_{CE(sat)}}{2} \approx V_\gamma$

$$T = \tau \ln 2 \frac{V_{CC} - V_\gamma}{V_{CC} - V_\gamma}$$

$$T = 0.69\tau \qquad (8.2)$$

The time period T can be calculated as $T = 0.69\,RC$, if Q_1 in the quasi-stable state is in saturation.

The Effect of Temperature on Gate Width

If the temperature effects are not taken into consideration, the gate width of a collector-coupled monostable multivibrator is given as $T = 0.69\,\tau$. When the temperature changes are taken into consideration, this gate width is likely to change. Consider a transistor which is in the OFF state as shown in Fig. 8.6(a).

Ideally, $I_C = 0$. However, there exists a leakage current called $I_{CBO} = I_{CO}$. The collector cut-off current, I_{CO} is reasonably large in Ge devices, but is small in Si devices. For Si devices at room temperature (25°C), typically I_{CO} is in the order of nanoamperes. However, as the temperature increases I_{CO} also increases, and gets doubled for every 10°C rise in temperature. When $I_C = 0$, $V_{CE} = V_{CC}$ If $I_{CO} = 10 \ \mu A$ and $R_C = 2 \ k\Omega$, then

$$V_{CE} = V_{CC} - I_{CO} \, R_C = 10 - (0.01)(2) = 9.98 \text{ V}$$

Thus, the voltage at the collector is 9.98 V instead of 10 V. In normal applications, this may not be important. However, in precision applications, temperature effects will have to be considered. Now consider the collector-coupled monostable multivibrator in Fig. 8.6(b). In the stable state, when capacitor C is fully charged, it behaves as an open circuit for dc. If the multivibrator is now driven into the quasi-stable state, the voltage to which the capacitor is returned is seen to be $V' = V_{CC} + I_{CO}R$, instead of V_{CC}. Hence, when capacitor C discharges, the final voltage $v_f = V'$.

Let us now calculate the time period. We have from Eq. (7.1):

$$V_{B2}(t) = v_f - (v_f - v_i)e^{-t/\tau}$$

Here,

$$v_f = V' = V_{CC} + I_{CO}R \qquad\qquad (8.3)$$

And if Q_1 is in saturation,

$$v_i = V_\sigma - I_1 R_C = V_\sigma - [(V_{CC} - V_{CE(\text{sat})}] = V_\sigma - V_{CC} + V_{CE(\text{sat})}$$

Neglecting the junction voltages $v_i = -V_{CC}$, and the time constant, $\tau = RC$.   Using Eq. (7.1):

$$V_{B2}(t) = V' - (V' + V_{CC})e^{-t/\tau} \qquad\qquad (8.4)$$

However, at $t = T$, $V_{B2}(t) = V_\gamma \approx 0$.
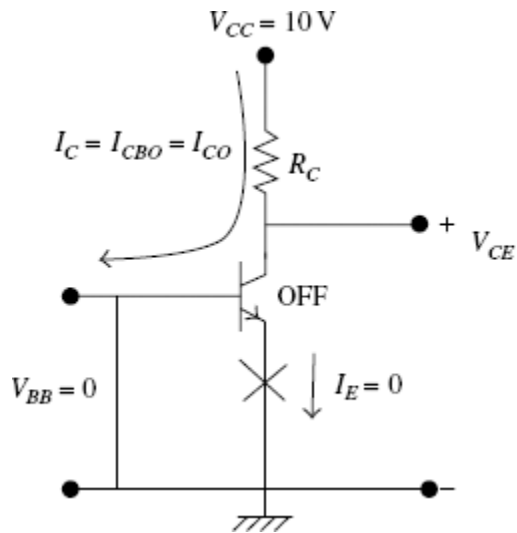
$$0 = V' - (V' + V_{CC})e^{-T/\tau}$$

FIGURE 8.6(a) Transistor in the OFF state
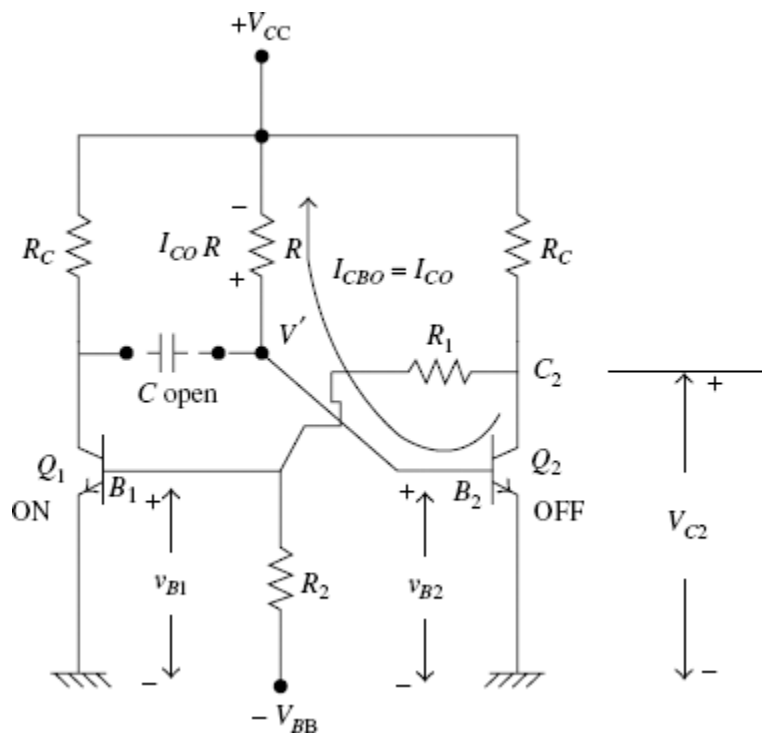
FIGURE 8.6(b) The collector-coupled monostable multivibrator considering I_{CO}

$$V' = (V' + V_{CC})e^{-T/\tau} \tag{8.5}$$

$$T = \tau \ln \frac{V' + V_{CC}}{V'} \tag{8.6}$$

Substituing <u>Eq. (8.3)</u> in <u>Eq. (8.6)</u>:

$$T = \tau \ln \frac{2V_{CC} + I_{CO}R}{V_{CC} + I_{CO}R} = \tau \ln 2 + \tau \ln \left(\frac{1 + \dfrac{I_{CO}R}{2V_{CC}}}{1 + \dfrac{I_{CO}R}{V_{CC}}} \right)$$

If

$$\phi = \frac{I_{CO}R}{V_{CC}} \qquad\qquad (8.7)$$

The gate width of the monostable multivibrator will now be less than the gate width calculated using <u>Eq. (8.2)</u>. This effect can be more pronounced with Ge transistors and at elevated temperatures

<div align="center">

<u>CALCULATION OF THE VOLTAGES TO PLOT THE WAVEFORMS</u>

</div>

<u>To plot the waveforms</u> at the two collectors and the two bases, the voltages in the circuit are to be calculated; when the multivibrator is in the stable state, when it is driven into the quasi-stable state and finally when it returns to the initial stable state. Consider the collector-coupled monostable multivibrator as shown in <u>Fig. 8.1</u>.

<div align="center">

In the Stable State ($t < 0$)

</div>

Here, the assumption is that Q_2 is ON and in saturation while Q_1 is OFF. In this situation, the need is to verify whether Q_2 is really in saturation or not and whether Q_1 is in the OFF state.

To Verify that Q_2 is in Saturation. For this we need to calculate I_{C2} and I_{B2} and then verify whether I_{B2} is significantly larger than I_{B2} (min) or not. If $I_{B2} >> I_{B2}$ (min), then Q_2 is really in saturation. To verify this, consider the circuit shown in<u>Fig. 8.7(a)</u>. From <u>Fig. 8.7(a)</u>,

$$I_2 = \frac{V_{CC} - V_{CE(sat)}}{R_C} \qquad\qquad (8.9)$$

$$I_3 = \frac{V_{CE(sat)} - (-V_{BB})}{R_1 + R_2} \qquad\qquad (8.10)$$
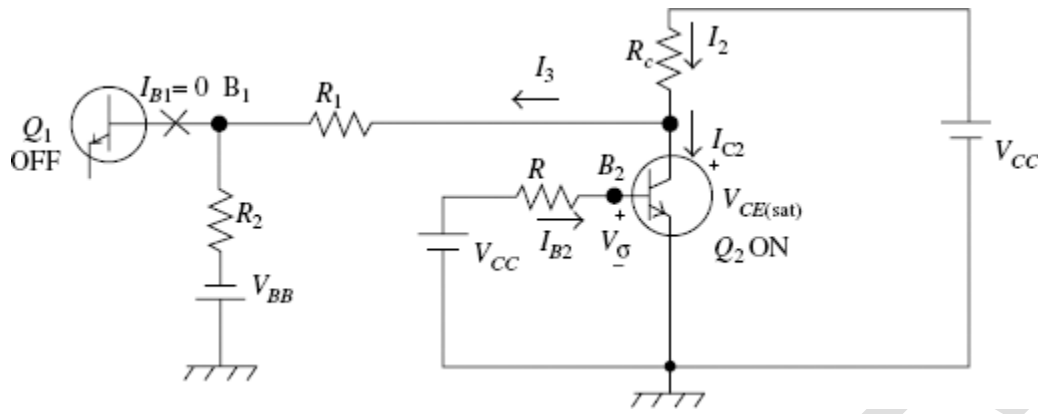
FIGURE 8.7(a) In the stable state Q_1 is OFF and Q_2 is ON

$$\therefore I_{C2} = I_2 - I_3 \tag{8.11}$$

$$I_{B2} = \frac{V_{CC} - V_\sigma}{R} \tag{8.12}$$

$$I_{B2(min)} = \frac{I_{C2}}{h_{FE(min)}} \tag{8.13}$$

For Q_2 to be in saturation, I_{B2} should be at least 1.5 I_{B2} (min). If $I_{B2} >> I_{B2}$ (min), Q_2 is really in saturation, as per the assumption made. Hence $V_{C2} = V_{CE(sat)}$ and $V_{B2} = V_{BE(sat)} = V_\sigma$.

To Verify that Q_1 is OFF. To show that Q_1 is OFF, the voltage V_{B1} at B_1 is to be found out and then checked whether the base–emitter diode is reverse-biased or not. If this diode is reverse-biased, then Q_1 is OFF. To calculate the voltage V_{B1} at B_1, consider the circuit shown in **Fig. 8.7(b)**. The voltage V_{B1} is due to the two sources; the V_{BB} source and the $V_{CE(sat)}$

source. Use the superposition theorem to calculate V_{B1}, considering one source at a time. Shorting the V_{BB} source, the resultant circuit is as shown in <u>Fig. 8.7(c)</u>.

$$V_{B1}(V_{BB} = 0) = V_{CE(sat)} \times \frac{R_2}{R_1 + R_2} \tag{8.14}$$

Now shorting the $V_{CE(sat)}$ source, the resultant circuit is as shown in <u>Fig. 8.7(d)</u>.

$$V_{B1}(V_{CE(sat)} = 0) = -V_{BB} \times \frac{R_1}{R_1 + R_2} \tag{8.15}$$

Combining <u>Eqs. (8.14)</u> and <u>(8.15)</u>, the net voltage V_{B1} at B_1 due to the two sources $V_{CE(sat)}$ and $-V_{BB}$ is:

$$V_{B1} = V_{CE(sat)} \times \frac{R_2}{R_1 + R_2} + (-V_{BB}) \times \frac{R_1}{R_1 + R_2}. \tag{8.16}$$

If the base of Q_1 is negative with respect to the emitter, the base–emitter diode is reverse-biased. Therefore, Q_1 is OFF, as assumed. Hence, $V_{C_1} = V_{CC}$. The voltage across the capacitor terminals is,

$$V_A = V_{C1} - V_{B2} = V_{CC} - V_\sigma \tag{8.17}$$

In the Quasi-stable State ($t = 0+$)

At $t = 0$, a negative pulse of proper amplitude is applied at the base of Q_2 that drives Q_2 into the OFF state. As a result Q_1 goes into the ON state and into saturation as shown in Fig. 8.7(e).

FIGURE 8.7(b) The circuit for calculating V_{B1}
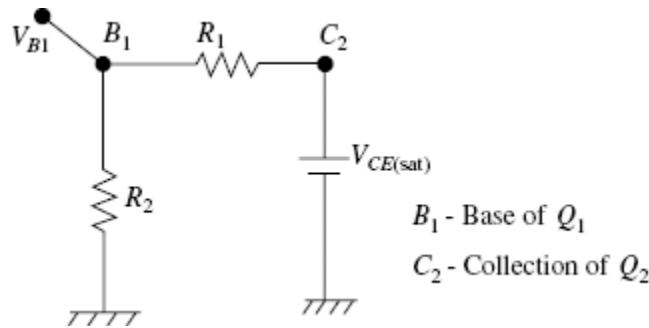
FIGURE 8.7(c) The circuit to calculate V_{B1} due to V_{CE}(sat) source
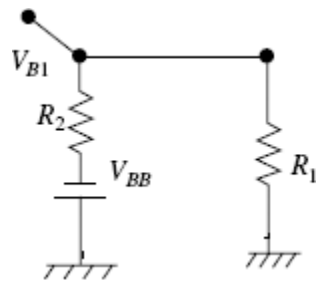
FIGURE 8.7(d) The circuit to calculate V_{B1} due to $-V_{BB}$ source
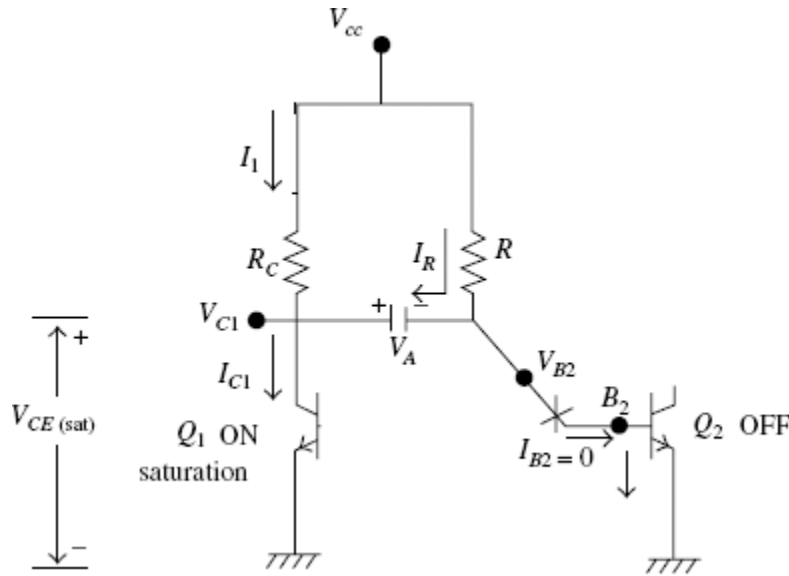
FIGURE 8.7(e) In the quasi-stable state Q_1 is ON and Q_2 is OFF

First let us verify whether Q_1 is really in saturation or not. Let us calculate I_{C1}.

$$I_{C1} = I_1 + I_R \tag{8.18}$$

$$I_1 = \frac{V_{CC} - V_{CE(sat)}}{R_C} \tag{8.19}$$

To calculate I_R, write the KVL equation of the loop consisting of R_C, C and R.

$$I_R R = I_1 R_C + V_A \tag{8.20}$$

Using Eqs. (8.19) and (8.20), we get I_1 and I_R.

Therefore,

$$I_{B1(min)} = \frac{I_{C1}}{h_{FE(min)}} \tag{8.22}$$

To Calculate I_{B1}. Considering Fig. 8.7(f):

$$I_{B1} = I_3 - I_4 \tag{8.23}$$

$$I_3 = \frac{V_{CC} - V_\sigma}{R_C + R_1} \tag{8.24}$$

$$I_4 = \frac{V_\sigma - (-V_{BB})}{R_2} \tag{8.25}$$

If $I_{B1} \gg I_{B1(min)}$, then Q_1 is in saturation,

If $I_{B1} \gg I_{B1(min)}$, then Q_1 is in saturation,

$$V_{C2} = V_{CC} - I_3 R_C \qquad\qquad (8.26)$$

$$V_{B2} = V_{CC} - I_R R \qquad\qquad (8.27)$$

In the quasi-stable state, only V_{B2} changes and all other voltages remain unaltered. At $t = T$, when $V_{B2} = V_\gamma$, the quasi-stable state ends and the multivibrator returns to the initial stable condition of Q_1 and Q_2 in the OFF and ON states, respectively.

At the End of the Quasi-stable State (at $t = T +$)

At the end of the quasi-stable state, Q_1 goes OFF and Q_2 goes ON and into saturation. In this process, overshoots (increase over and above the expected value) can occur at the base of Q_2 and at the collector of Q_1, because the voltage change occurs abruptly. The amount of overshoot is accounted for by the base spreading resistance $r_{bb'}$ which is the resistance seen between the external base lead and the internal base terminal and is the resistance offered to a recombination current. This is typically less than 1 kΩ, as shown in Fig. 8.7(g).

From Fig. 8.7(g),

$$I_{B2} = I'_{B2} + I'_R \qquad\qquad (8.28)$$

As

$$R \gg R_C, \quad I'_R \ll I'_{B2}. \qquad\qquad (8.29)$$

Neglecting the current I_R when compared to I'_{B2} the circuit reduces to as shown in Fig. 8.7(h).

The voltages at B_2 and C_1 are

$$V'_{B2} = I'_{B2} r_{bb'} + V_\sigma \qquad\qquad (8.30)$$

The overshoot δ at the second base is the variation over and above V_γ.

$$\delta = V'_{B2} - V_\gamma$$

Using Eq. (8.30):

$$\delta = V'_{B2} - V_\gamma = I'_{B2}r_{bb'} + V_\sigma - V_\gamma. \qquad (8.32)$$

Similarly the overshoot δ' at the first collector is the variation over and above $V_{CE(\text{sat})}$

Therefore,

Using Eq. (8.31):

$$\delta' = V_{CC} - I'_{B2}R_C - V_{CE(\text{sat})}. \qquad (8.33)$$
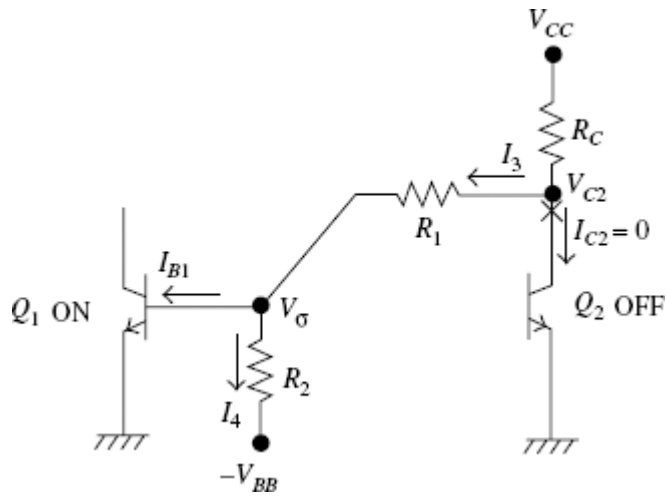
FIGURE 8.7(f) Circuit that is used to calculate I_{B1}
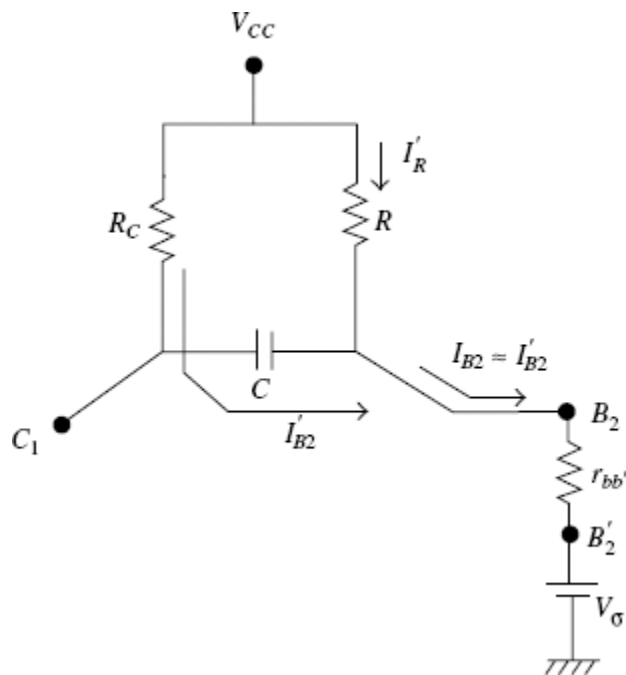
FIGURE 8.7(g) The circuit at the end of the quasi-stable state
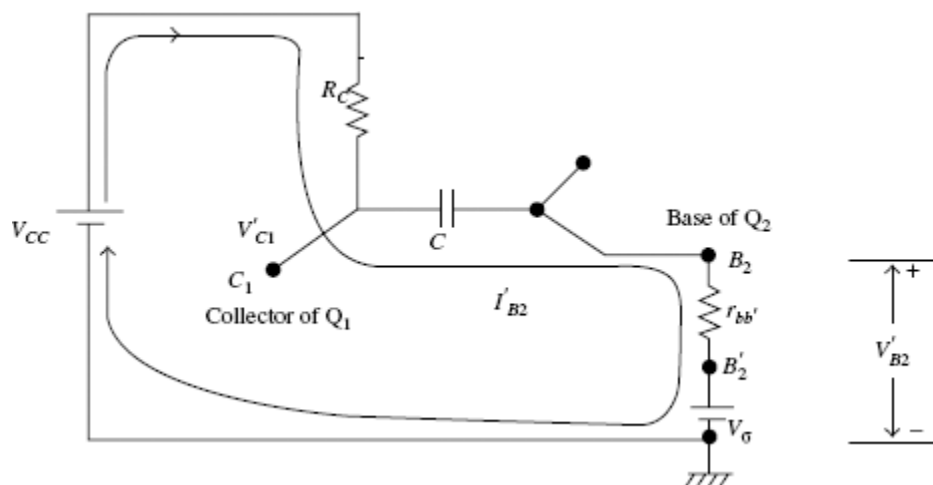
FIGURE 8.7(h) The simplified circuit of <u>Fig. 8.7(g)</u>

The first collector and the second base are connected through a condenser C and as the condenser will not allow any sudden changes in the voltages, whatever is the change that takes place at the first collector an identical change is required to take place at the second base. Hence, $\delta = \delta'$.

$$I'_{B2}r_{bb'} + V_\sigma - V_\gamma = V_{CC} - I'_{B2}R_C - V_{CE(sat)}$$

$$I'_{B2}(r_{bb'} + R_C) = V_{CC} - V_{CE(sat)} - V_\sigma + V_\gamma$$

$$\therefore I'_{B2} = \frac{V_{CC} - V_{CE(sat)} - V_\sigma + V_\gamma}{r_{bb'} + R_C} \tag{8.34}$$

$$V'_{C1} = V_{CC} - I'_{B2}R_C \tag{8.35}$$

$$V'_{B2} = I'_{B2}r_{bb'} + V_\sigma \tag{8.36}$$

The waveforms can now be plotted. To plot the waveforms of a collector-coupled monostable multivibrator with specific component values mentioned, consider the following example.

COMMUTATING CONDENSERS

In the initial stable state Q_2 is ON and in saturation, Q_1 is OFF. Once a trigger is applied [see Fig. 8.3] to change the state of the devices in the monostable multivibrator, because of the stray capacitances of the devices they may not go into the next state immediately. This is a problem which needs to be overcome.

Now, let a negative pulse be applied at the base Q_2 to drive it into the OFF state and consequently Q_1 into the ON state. Prior to the application of this trigger the voltage at the second collector was $V_{CE(sat)}$. On the application of a trigger at $t = 0$, as Q_2 goes into the OFF state, the voltage at its collector rises from $V_{CE(sat)}$ to V_{CC}. Let the change in voltage at the second collect be v_i, a step voltage. That is,

$$v_i = V_{CC} - V_{CE(sat)} \tag{8.44}$$

This voltage change at the second collector is coupled to the first base through R_1 and R_2, as shown in Fig. 8.9(a). As a result, Q_1 is expected to switch into the ON state.

If the attenuator is a simple resistive attenuator as seen in Fig. 8.9(a), the moment Q_2 switches into the OFF state, Q_1quickly switches into the ON state. However, between the input terminals of Q_1 if a stray capacitance C_i is present, then the attenuator circuit in Fig. 8.9(a) gets modified as shown in Fig. 8.9(b).

FIGURE 8.9(a) A simple resistive attenuator
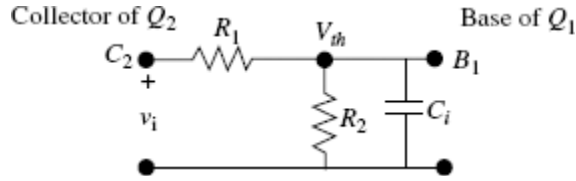
FIGURE 8.9(b) An attenuator considering the stray capacitance

To reduce this two loop network into a single loop network, let us Thévenise the circuit.

$$V_{th} = v_i \frac{R_2}{R_1 + R_2} = \alpha V_i \qquad (8.45)$$

here

$$\alpha = \frac{R_2}{R_1 + R_2} \qquad (8.46)$$

and

$$R_{th} = R_1 || R_2 \qquad (8.47)$$

Then the circuit shown in Fig. 8.9(b) reduces to that shown in Fig. 8.9(c).

Now, only when the voltage at B_1 rises to 90 per cent of its final value, the device Q_1 is assumed to switch from the OFF state into the ON state. This time interval is the rise-time of the circuit.

$$t_r = 2.2 R_{th} C_i \qquad (8.48)$$

EMITTER-COUPLED MONOSTABLE MULTIVIBRATORS

In the collector-coupled monostable circuit, for the gate width T to be stable, the ON device, in the quasi-stable state, is required to be driven into saturation [see Eq. (8.2)]. Once a device is driven into saturation the storage time becomes longer. Hence, the switching speed of the multivibrator is reduced, which is considered as the main limitation of this circuit.

Further, as there is a cross-coupling from the second collector to the first base in the collector-coupled monostable multivibrator, if the cross-coupling network loads the collector circuit, the voltage change at this collector may not necessarily be V_{CC}. This reduced voltage change at the second collector may not in turn drive Q_1 into saturation, in the quasi-stable state. These limitations can be eliminated in an emitter-coupled monostable multivibrator, as shown in Fig. 8.11(a).

In this circuit, there is no cross-coupling from the second collector to the first base. Hence, the second collector is not loaded by this cross-coupling network. Therefore, the second collector is an appropriate point at which the output can be taken.

The first base is not involved in regeneration and hence, becomes a suitable point at which the trigger can be injected. When Q_1 is driven into the ON state in the quasi-stable state of a collector-coupled monostable multivibrator, the current I_1 in Q_1 cannot be stable and thus, Q_1 is preferably driven into saturation to make gate width, T stable. However, in the emitter-coupled monostable multivibrator when Q_1 goes ON, the current I_1 in Q_1 can be maintained stable because of a substantial emitter resistance (provides negative feedback), even if the device is in the active region. This reduces the storage time and hence, improves the switching speed of the multivibrator. The operation of the multivibrator in Fig. 8.11(a) is explained in the following paragraphs.

In the stable state, let Q_1 be OFF and Q_2 be ON and in saturation, as shown in Fig 8.11(b). During this period, the capacitor C charges through R_{C1}, and the input resistance between the base and reference terminal, R_{i2}. The charging time constant is $(R_{C1} + R_E + r_{bb'})\, C$.

To drive the multivibrator into the quasi-stable state, a positive pulse of proper magnitude is applied at the base of Q_1, as shown in Fig. 8.11(d). As a result, Q_1 is driven into the active region and Q_2 into the OFF state. Now, the capacitor C discharges through the small resistance between the collector and emitter terminals of Q_1, R_E and R. As a result, the voltage at B_2 varies as a function of time. When the voltage at B_2 is such that it drives Q_2 into the ON state, the multivibrator comes back into the initial stable condition of Q_1 OFF and Q_2 ON. The discharging time constant is $C(R_o + R_E + R) \approx RC$ as $R >> (R_E + R_o)$.
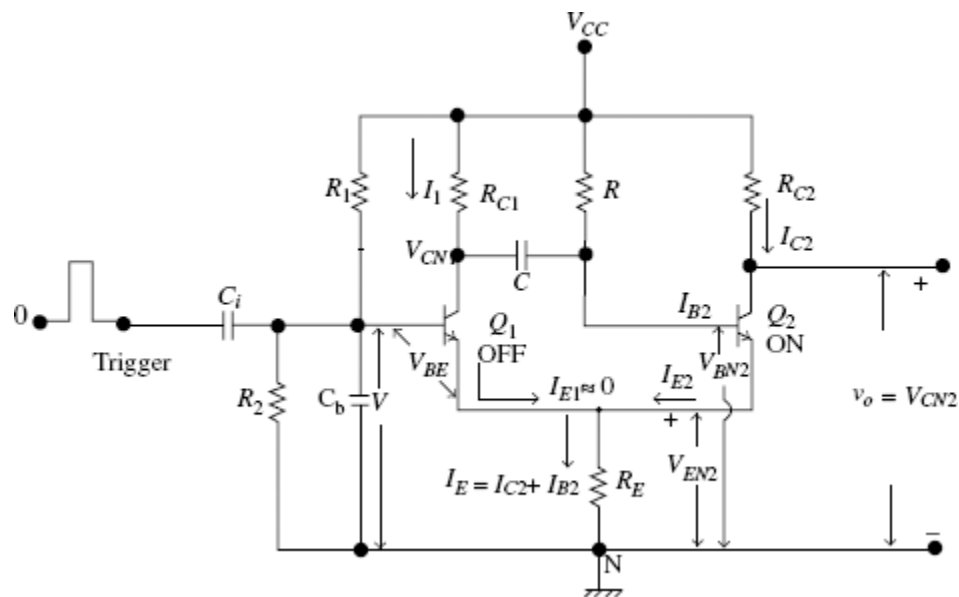
FIGURE 8.11(a) The emitter-coupled monostable multivibrator
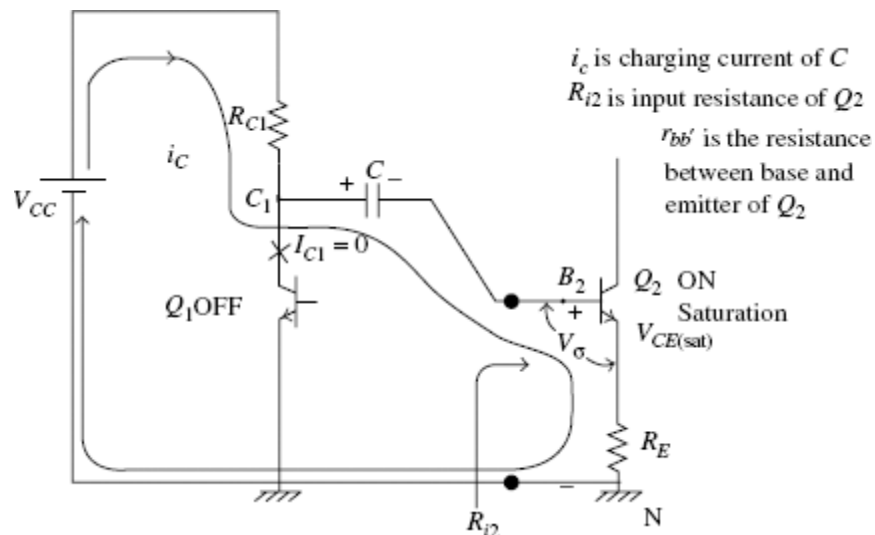
FIGURE 8.11(b) In the stable state, Q_1 is OFF and Q_2 is ON
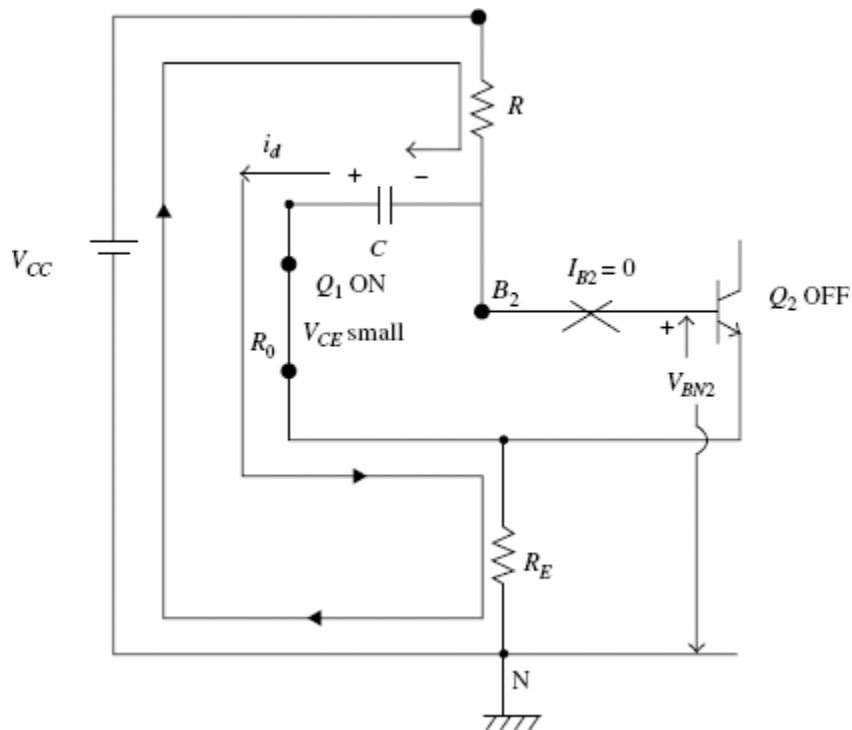
FIGURE 8.11(c) Discharge of capacitor C in the quasi-stable state when Q_1 is ON and Q_2 is OFF

To Calculate the Gate Width (T)

To calculate the gate width T, consider the voltage variation at the base of Q_2, as shown in **Fig. 8.11(d)**. In the stable state, Q_1 is OFF and Q_2 is ON and in saturation. Let V_{BN2} ($0-$) be the voltage at B_2 in the stable state. At $t = 0$, a trigger is applied, Q_1 goes ON and the voltage at its collector falls by I_1R_C. A similar change in the voltage occurs at the second base. Therefore, V_{BN2} also falls by I_1R_C. Now the charge on the capacitor C discharges with a time constant $\tau \approx RC$. The moment the voltage at the second base is ($V_{EN1} + V_{\gamma2}$), Q_2 again goes into the ON state and Q_1 into the OFF state, thus ending the quasi-stable condition. The voltage at the base of Q_2 at any given time, after the application of a trigger, is given by:
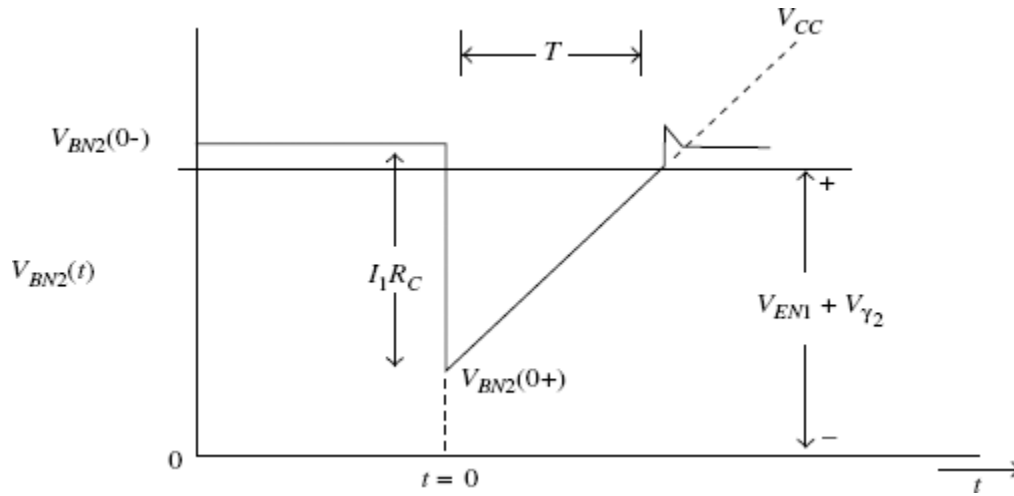
$$V_{BN_2}(t) = v_f - (v_f - v_i)e^{-t/\tau}$$

$$v_f = V_{CC}$$

$$v_i = V_{BN_2}(0-) - I_1 R_{C_1}$$

$$V_{BN_2}(t) = V_{CC} - (V_{CC} - V_{BN_2}(0-) + I_1 R_{C_1})e^{-t/\tau}$$

At $t = T$, $V_{BN_2}(T) = V_{EN_1} + V_{\gamma_2}$

Therefore,

$$V_{EN_1} + V_{\gamma_2} = V_{CC} - (V_{CC} - V_{BN2}(0-) + I_1 R_{C1})e^{-T/\tau}$$

$$T = \tau \ln\frac{V_{CC} - V_{BN2}(0-) + I_1 R_{C1}}{V_{CC} - V_{EN1} - V_{\gamma_2}} \tag{8.52}$$

The gate width T can be calculated using Eq. (8.52). To plot the waveforms of an emitter-coupled monostable multivibrator, we calculate the voltages in the stable state, in the quasi-stable state and when the multivibrator returns to its original stable state.

Astable Multivibrators

INTRODUCTION

Multivibrators are switching circuits that employ positive feedback by cross-coupling the output of one stage to the input of the other stage, such that if one device is ON, the other is OFF. The interchange of states is possible either by the use of external pulses or by internal

capacitive coupling. These circuits are used either to generate waveforms of a desired nature or to store binary information. Multivibrators are of three types—astable, monostable and bistable. An astable multivibrator is basically a square-wave generator. A monostable multivibrator generates a gated output (pulse) of a desired duration. A bistable multivibrator stores binary bits. In this chapter, we focus on astable multivibrators.

A transistor Q_1 or Q_2 is said to be in the stable state, if it is either ON or OFF permanently. If the state of the device, say Q_1, changes from ON to OFF, and automatically returns to the ON state after a time duration, the device is said to be in the quasi-stable state for this specified time interval. The devices in this multivibrator will not remain in any one state (ON or OFF) forever. The change of state in the device occurs automatically after a finite time interval, depending on the circuit components employed. Hence, this circuit has two quasi-stable states.

In an astable multivibrator, if Q_1 is ON, then Q_2 is OFF; and they will remain in this state for a limited time duration, after which Q_1 automatically switches into the OFF state and Q_2 into the ON state and so on. The output of the circuit is a square wave with two time periods, T_1 and T_2. If $T_1 = T_2 = T/2$ the circuit is a symmetric astable multivibrator. If $T_1 = T_2$, it is called an un-symmetric astable multivibrator. The main application of an astable multivibrator is as a clock in digital circuits.

The astable multivibrator is essentially a square-wave generator (oscillator). We consider two circuits: the collector-coupled astable multivibrator and the emitter-coupled astable multivibrator in the following sections.

COLLECTOR-COUPLED ASTABLE MULTIVIBRATORS

A collector-coupled astable multivibrator is shown in <u>Fig. 7.1</u>. Here, there is a cross-coupling from the second collector to the first base and also a cross-coupling from the first collector to the second base. This means that the output of one device is the input for the other. While analysing the functioning of this circuit, it is assumed that the circuit is an oscillator; and working backwards, we can justify that it does indeed oscillate.
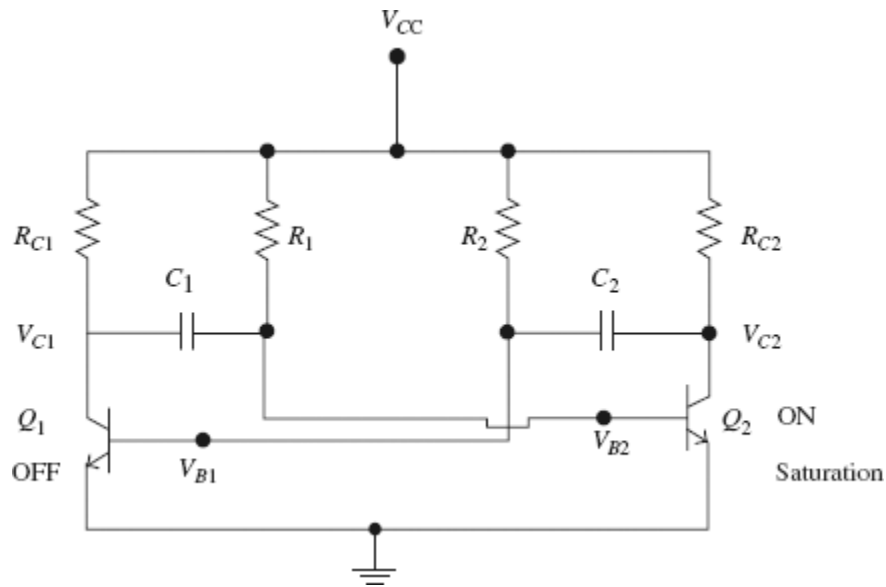
FIGURE 7.1 A collector-coupled astable multivibrator

Let us assume that at the given instant of time Q_1 is OFF and Q_2 is ON and saturated. Then $V_{B2} = V_o$, $V_{C2} = V_{CE(sat)}$ and $V_{C1} = V_{CC}$. With Q_1 OFF and Q_2 ON, C_1 will try to charge to the supply voltage through the collector resistance R_{C1} and the small resistance of Q_2 ($\approx r_{bb'}$), as shown in Fig. 7.2.

However, prior to this condition, Q_2 must have been in the OFF state and Q_1 must have been in the ON state. As a result, C_2 must have been charged through R_{C2} and $r_{bb'}$ of Q_1, as shown in Fig. 7.3.

When Q_2 suddenly switches from the OFF state into the ON state, the voltage between its collector and emitter terminals is V_{CE} (≈ 0 V). Hence, the collector of Q_2 is at ground potential, i.e., the positive end of the capacitor C_2 is at the ground potential and its negative terminal is connected to the base of Q_1. As a large negative voltage is now coupled to the base of Q_1, it is in the OFF state (see Fig. 7.4). However, Q_1 will not remain in the OFF state forever. Now, with Q_2 ON, the charge on the condenser C_2 discharges with a time constant $\tau_2 = R_2 C_2$
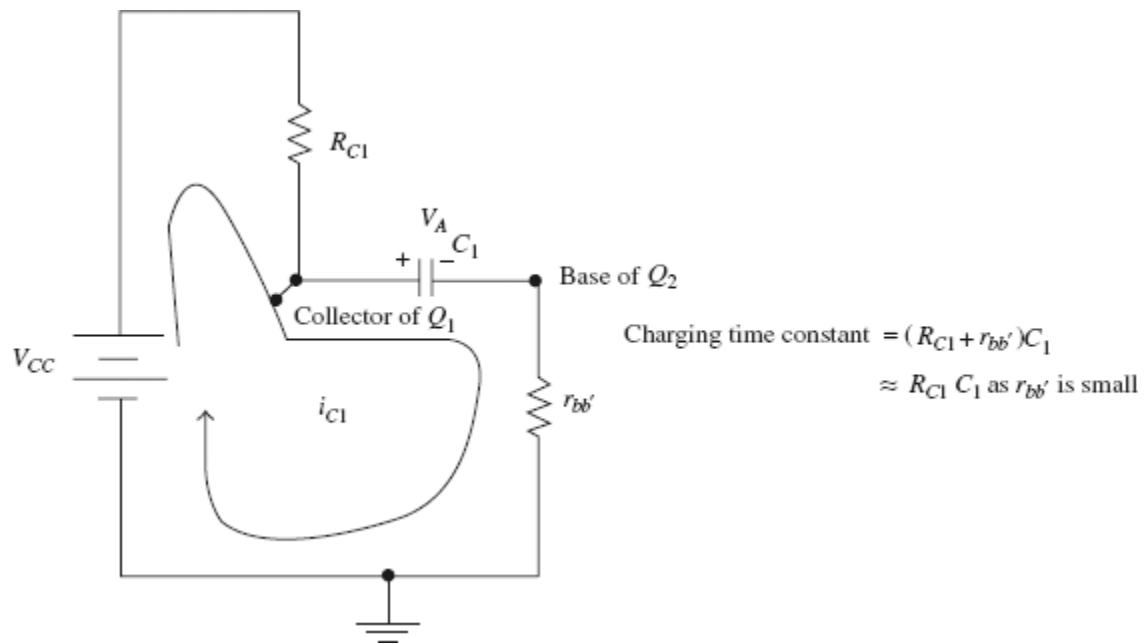
FIGURE 7.2 The charging of the capacitor C_1

Charging time constant $= (R_{C1} + r_{bb'})C_1$

$\approx R_{C1} C_1$ as $r_{bb'}$ is small
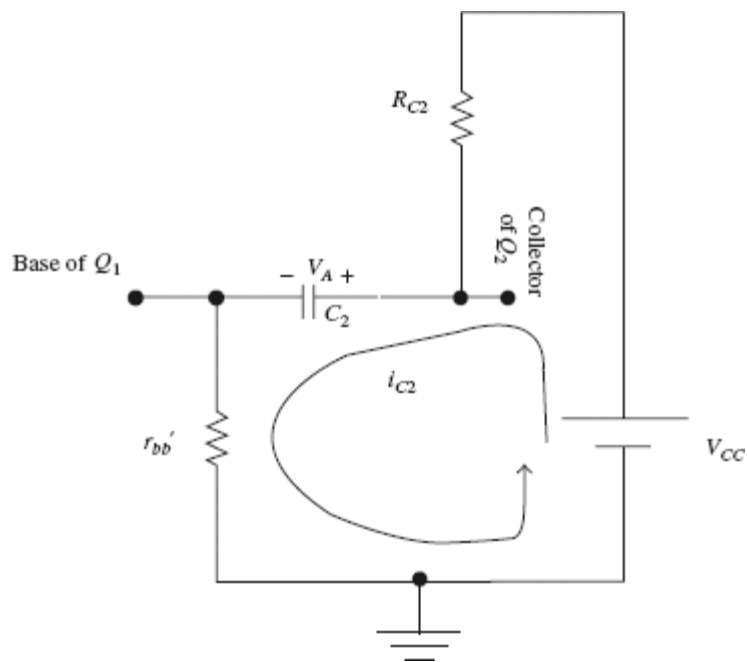
FIGURE 7.3 The charging of capacitor
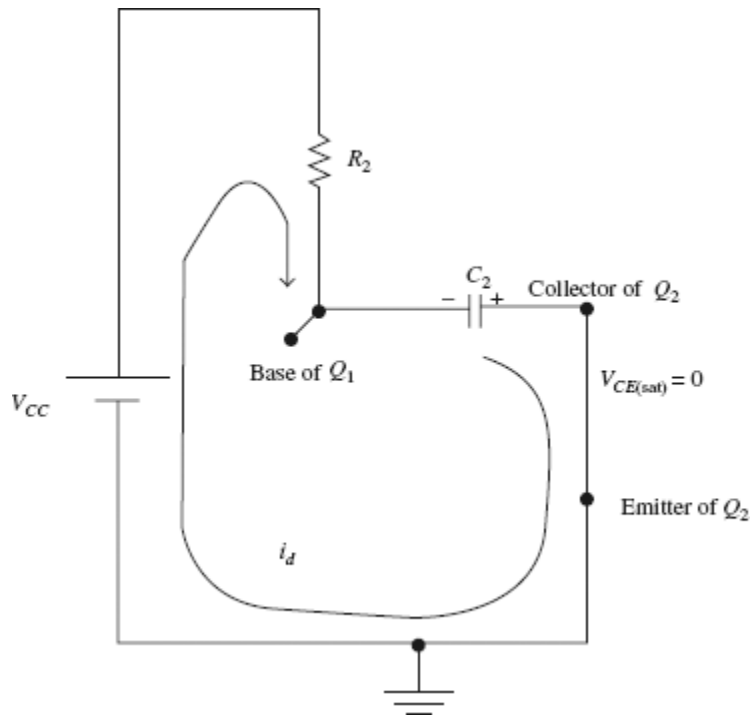
FIGURE 7.4 The discharge of C_2 through R_2

As a result, the voltage at the base of Q_1 goes on changing as a function of time. Once this voltage reaches V_γ, Q_1 starts drawing base current. Hence, there is a collector current. In turn, there is voltage drop across R_{C1} and the voltage at the collector of Q_1 falls. This voltage was earlier V_{CC} and now, it is smaller than V_{CC}. Therefore, the negative step at this collector is coupled to the base of Q_2 through C_1. As the collector of Q_1 and the base of Q_2 are connected through C_1 and the capacitor will not allow any sudden changes in the voltage, the base of Q_2 undergoes changes that are identical to those that have taken place at the first collector. As a result, the base and collector current of Q_2 drop; so, the collector voltage rises. This positive step change is coupled to the base of Q_1; and thus, its base current increases further. And the collector current increases, the voltage at the collector of Q_1 falls still further. This step change is coupled to the base Q_2 and this process is repeated. Thus, a regenerative action takes place and Q_2 switches to the OFF state and Q_1 goes into the ON state. Hence, the circuit oscillates. As long as the voltage at the base is V_o, the voltage at the collector is $V_{CE(sat)}$. Once the voltage at the base is negative, the device switches into the OFF state, giving rise to a voltage V_{CC} at its collector. The waveforms at the two bases and the two collectors are shown in Fig 7.5. When a transistor, say Q_1, switches from the ON state into the OFF state, its collector voltage is required to abruptly rise to V_{CC}. Consequently, the waveforms at the collectors should have sharp rising edges and flat tops. But when Q_1 goes into the OFF state

and Q_2 into the ON, there is a charging current of the condenser C_1 which prevents the sudden rise of the voltage from V_{C_1} to V_{CC}. Only when this charging current is zero does the collector voltage reach V_{CC}, as shown in <u>Fig. 7.6</u>. Hence, there is a rounding off of the

rising edge of the pulse.

Calculation of the Frequency of an Astable Multivibrator

To calculate the frequency (f), the two time periods T_1 and T_2 are to be calculated. Then:

$T = T_1 + T_2$ and   f=1/T
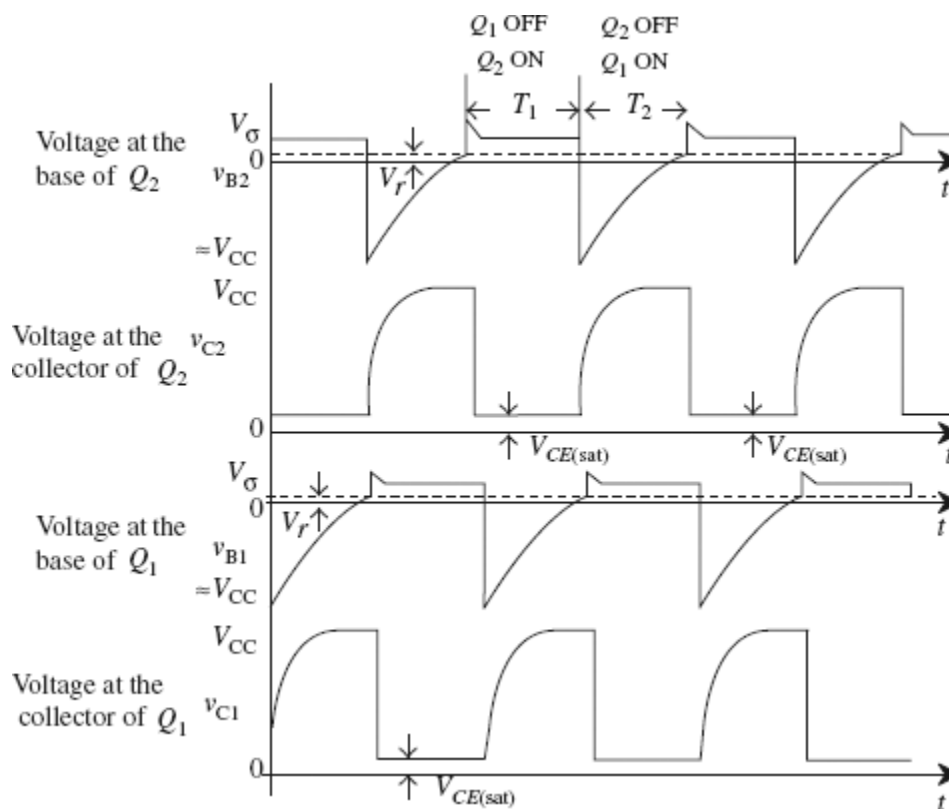
FIGURE 7.5 The waveforms of a collector-coupled astable Multivibrator

AN ASTABLE MULTIVIBRATOR AS A VOLTAGE-CONTROLLED OSCILLATOR

A voltage-controlled oscillator (VCO) is one in which the frequency of oscillations varies as a function of voltage. The same circuit is also called a voltage-to-frequency converter (VFC) because a given voltage gives rise to a specific frequency. An astable multivibrator is used as voltage-controlled oscillator [see <u>Fig. 7.13(a)</u>]. A comparison of this with the circuit shown

in Fig. 7.1 shows that here the two resistors R and R are returned to a separate source V_{BB} rather than to V_{CC}.

When Q_1 is OFF and Q_2 is ON, C_1 charges. When Q_1 is ON, the charge on C_1 decays with a time constant $\tau_1 = RC_1$ as shown in Fig. 7.13(b). As a result, the voltage at the base of Q_2, V_{B2} varies with time, [see Fig. 7.13(c)].

$$v_{B2}(t) = v_f - (v_f - v_i)e^{-t/\tau_1}$$
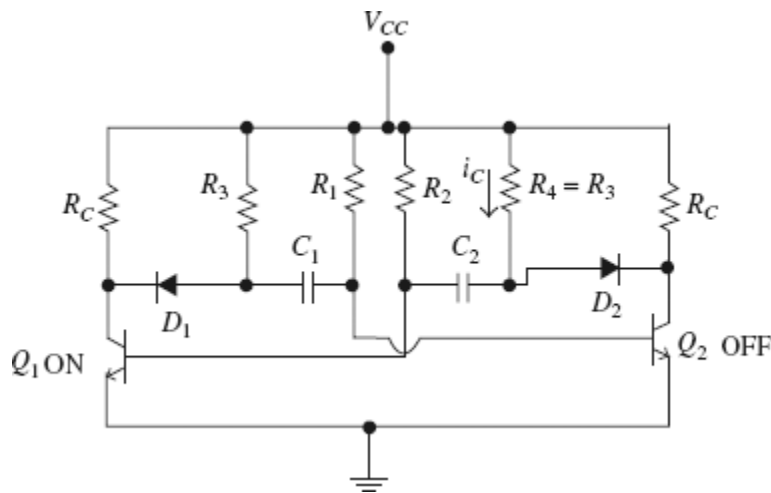
FIGURE 7.12 An astable multivibrator that generates pulses with vertical edges
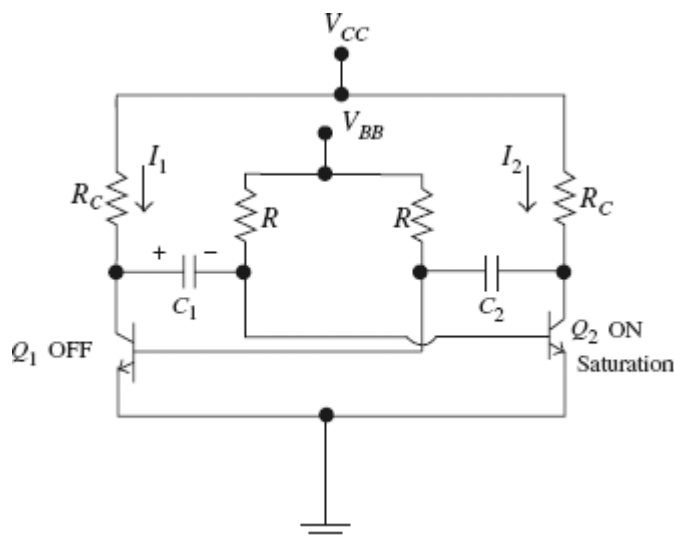
IGURE 7.13(a) A voltage-to-frequency converter

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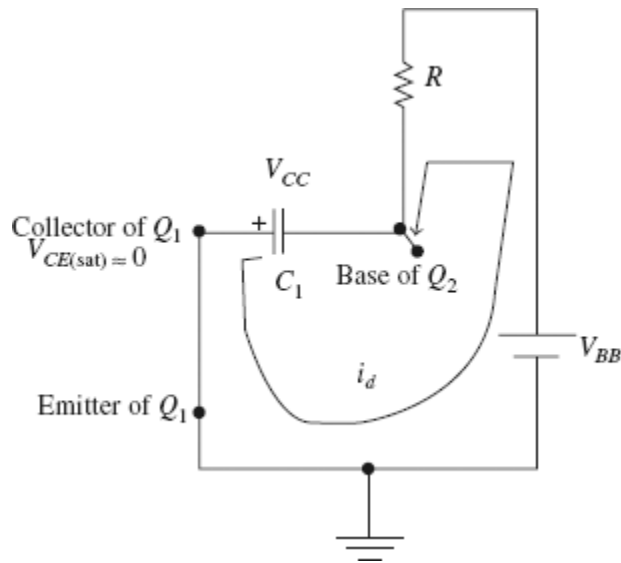
FIGURE 7.13(b) The discharge of condenser C_1 through R
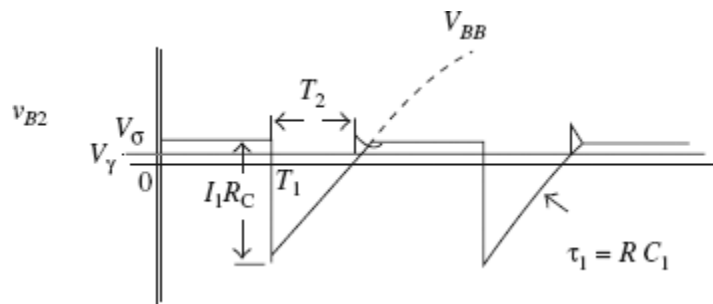
F**IGURE 7.13(c)** The voltage variation at the base of Q_2

$v_f = V_{BB}$ $v_i = V_\sigma - I_1R_C = V_\sigma - V_{CC} + V_{CE(sat)}$

Since $I_1R_C = V_{CC} - V_{CE(sat)}$;

$v_{B2} = V_{BB} - [V_{BB} - V_\sigma + V_{CC} - V_{CE(sat)}]e^{-T_2/\tau_1}$

At $t = T_2$, $v_{B2}(t) = V_\gamma$

$\therefore V_\gamma = V_{BB} - [V_{BB} - V_\sigma + V_{CC} - V_{CE(sat)}]e^{-T_2/\tau_1}$

If the junction voltages are small,

$0 = = V_{BB} - (V_{BB} + V_{CC})e^{-T_2/\tau_1}$

For a symmetric circuit, $T_1 = T_2 = T/2$ and $\tau_1 = \tau_2 = \tau$

$$T_1 = T_2 = \frac{T}{2} = \tau \ln\left(\frac{V_{BB} + V_{CC}}{V_{BB}}\right) \qquad (7.29)$$

Consequently, for a symmetric astable multivibrator:

$$T = 2\tau \ln\left(1 + \frac{V_{CC}}{V_{BB}}\right) \qquad (7.30)$$

And, $f = 1/T$. As the frequency of the multivibrator can be varied by simply varying V_{BB}, this circuit is called a voltage-controlled oscillator or voltage-to-frequency converter.

UNIT IV – b

Time Base Generators:

'Bootstrap' Ramp Generator

For many purposes, for example providing a time axis for oscilloscope displays, a voltage varying linearly with time is needed. In many instances a satisfactory approximation to such a 'ramp' is obtained by making use of a simple RC charging circuit, using just the initial part of the exponential charging response. For a time interval small compared to the RC time constant the exponential is well approximated by a tangent at the origin. Modifications of this basic procedure improve in one way or another the linearity of the approximation or, perhaps more accurately said, extend the period over which the approximation is useful. Several 'ramp' circuits are reviewed in this note.

Basic RC Ramp

A straightforward approach to generating a ramp voltage is illustrated by the circuit diagram to the right. A square wave applied to the BJT alternately switches the transistor between saturation and cutoff operation. When the transistor is cutoff the capacitor C1 charges exponentially through R2, with a time constant R2 C1. On the other hand if the transistor is turned on the capacitor discharges rapidly and the transistor saturates.

The transient response of this circuit was computed for two conditions. The data plotted immediately below is for a pulse width of 1 millesecond and a period of 30 millesecond. The period is several time
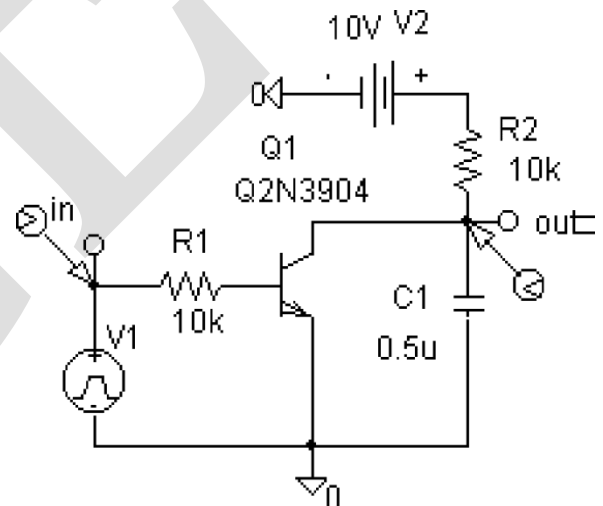
constants in width so as to make the exponential nature of the RC charging clearly evident.Only the initial part of the exponential rise, a period short compared to one time constant,, is 'linear' to any extent.In practice the pulse duration would be considerably shorter, just long enough allow for just the initial part of the charging cycle. To illustrate this the circuit response was recomputed, this time for a pulse width of 50 μseconds and a period of just 0.5 millesecond, about one tenth the time constant. The computed data is plotted below. Comparison of the computed data with expected performance is left as an exercise.

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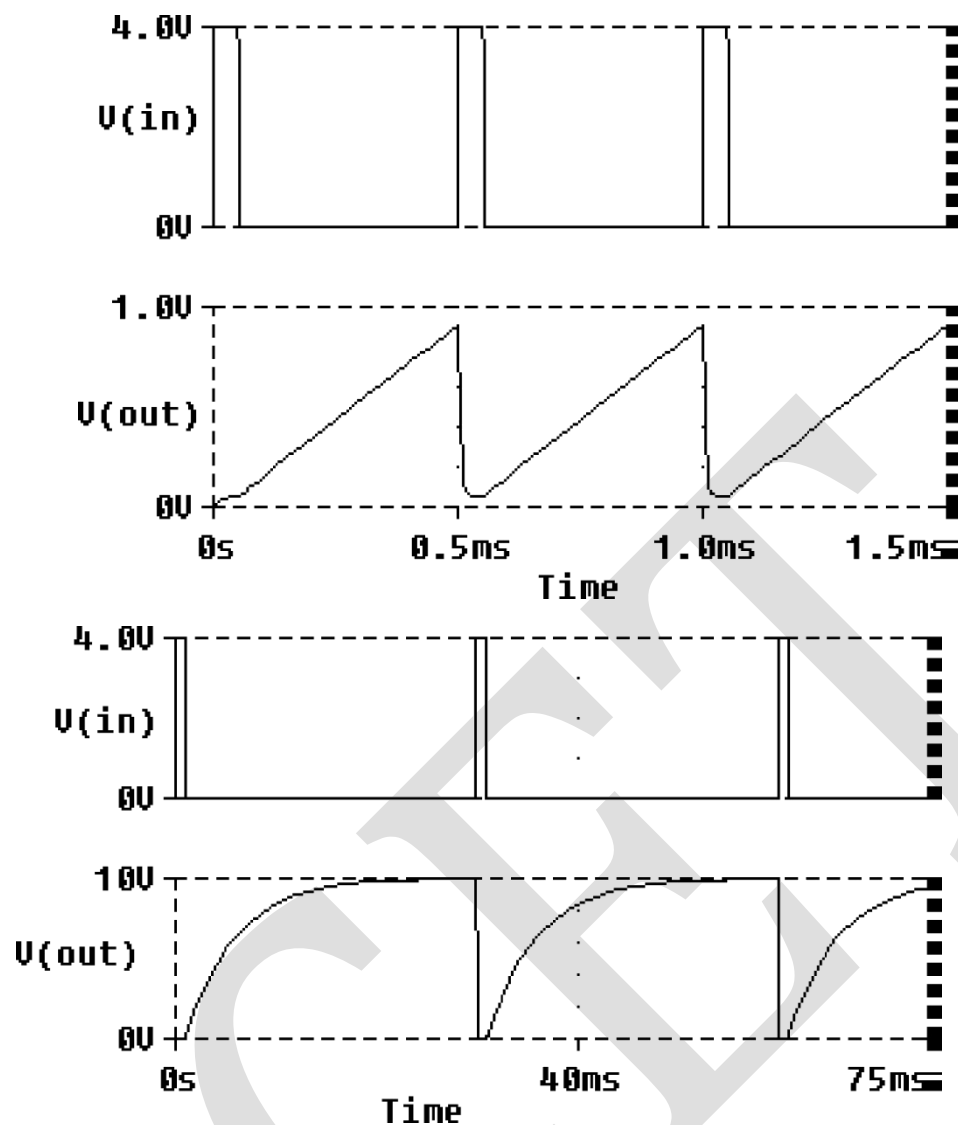
Current-Pumped Ramp

RC charging is, as was noted, fundamentally exponential rather than linear. The ramp is approximately linear only for a initial period short compared with a time constant, i.e., the initial part of the exponential rise. The difficulty with RC charging is that as the voltage across the capacitor increases the voltage difference across the charging resistor decrease, and so also does the charging current. Hence the capacitor charges at a continually decreasing rate.
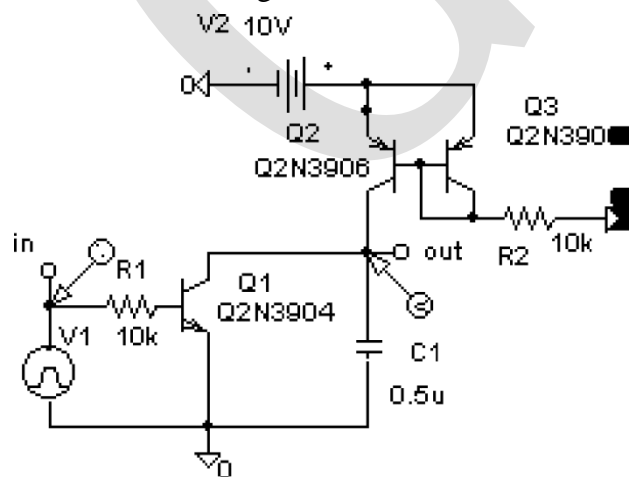
the linearity over an increased voltage range is apparent in the computed performance plotted to the right.

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One way to avoid this difficulty is to charge the capacitor with a constant current source. The circuit (left) replaces the charging resistor of the previous illustration with a (nearly) constant current source formed by the transistors Q2 and Q3. The diode-connected transistor Q3 is used to define the Q3 emitter current, and assuming a good match between Q2 and Q3, cause Q2 to carry the same emitter current. (The Q2 current is not quite constant because of the small dependence of Q2 collector current on collector voltage (Early effect).
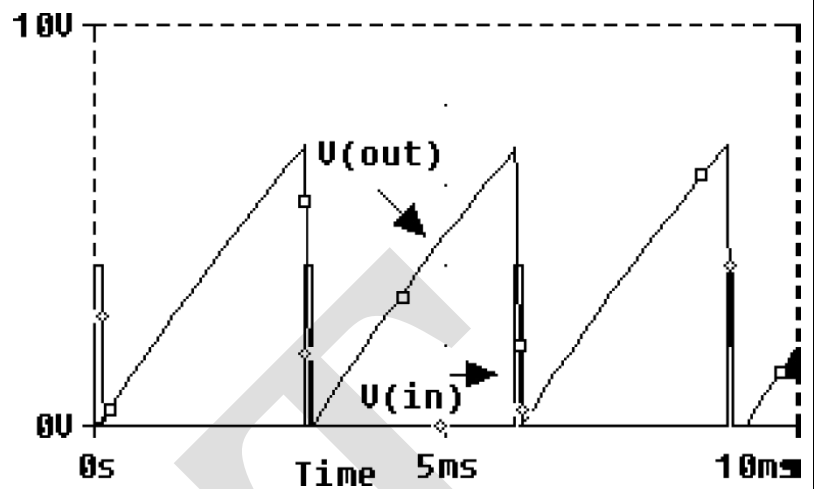
'Bootstrap' Ramp

An intriguing type of ramp generator applies positive feedback to extend the range of linear operation of an RC charging circuit. The circuit diagram on the left side of the figure below suggests a conceivable (but unworkable) approach.. R_T and C_T form a RC charging circuit with time constant $R_T C_T$. A switch periodically closes momentarily to discharge the capacitor and initiate the capacitor charging cycle. The capacitor voltage would rise linearly if the charging current were (somehow) constant. This would be so if, for example, a fixed voltage were applied across RT. But then the voltage at the upper end of RT would have to increase continuously since the voltage across CT increases as the capacitor charges. The circuit illustrated below is an ingenious method for doing just that.
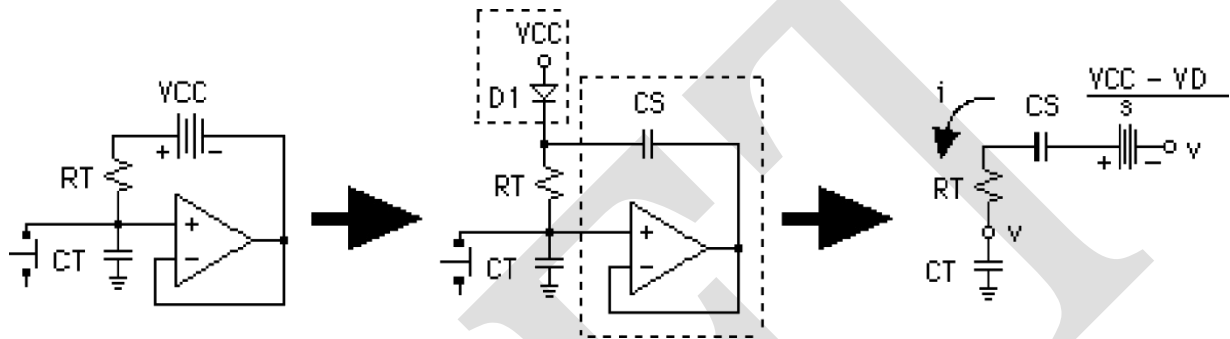
In the circuit on the left (above) a voltage follower is used to copy the voltage across CT without (ideally) loading the capacitor. The voltage across RT is VCC, and because of the voltage follow3er action remains even as the capacitor charges. Momentarily closing the switch discharges the capacitor and initiates the charging cycle.

A more practical version of this connection is illustrated in the center diagram. Instead of a battery a capacitor CS is used. If the time constant associated with CS is much greater than that associated with CT, i.e. CS >> CT, then in a given period voltage changes across CS will be much smaller than those across CT. To the extent that the voltage across CS is essentially constant this capacitor acts as a sort of temporary battery. It is of course necessary to assure that the capacitor is appropriately charged to provide the equivalent of the battery voltage. It is not feasible to connect VCC directly to CS, since the voltage at the RT-CS node is supposed to change. A buffer resistor might be used but there are conflicting requirements for its size. The resistance should be 'large' so that it does not significantly affect the timing for the charging, and it should be 'small' so that recharging CS occurs quickly. These conflicting requirements are met by use of a diode. CS charges quickly to VCC (less the diode voltage drop) through the diode. Then as the voltage across CT rises so also does the voltage at the base of the diode, and the diode becomes reverse biased.

To summarize:

A capacitor C_S is charged, and used a sort of temporary voltage source. The voltage follower provides a high resistance connection from CT that copies the capacitor voltage to one end of CS.

While C_T is being discharged (closed switch) C_S is charged through the diode by the VCC source. The diode is used to enable charging of CS by the source but prevent a converse current flow. C_S charges to somewhat less than V_{CC} because of the diode junction voltage drop. When the switch is opened C_T charges through RT, and as CT charges the rising voltage at the non-

inverting amplifier input is conveyed to CS. Provided CS >> CT, i.e., is associated with a much larger time constant, it will discharge much more slowly than CT. Hence the voltage at the other end of RT rises, and the diode becomes reverse-biased. Thereafter it is actually CS that supplies the current that charges CT. In effect

CS (and the voltage follower) is being used in a fashion as battery to produce a nearly constant current through RT.

Note that the feedback is positive, i.e. as the voltage across CT rises feedback provided through the voltage follower applies a voltage to further increase the voltage. However the process necessarily terminates itself since the opamp will saturate eventually. A connection of this sort is commonly called a 'bootstrap' connection after the tongue-in-cheek suggestion that people can lift themselves off the ground by pulling up on their own bootstraps.

When the switch is closed CS charges very quickly through the diode. The equivalent (LaPlace) circuit (idealized opamp) for the charging cycle is drawn on the right of the previous figure. It can be shown (show it) that

$$v(t) = VCC \frac{CS}{CT} \left[1 - e^{-t/RTCS} \right]$$

Note that the charging remains exponential, characteristic for a RC charging. The bootstrap effect appears in the time constant, which involves not CT but the (larger) capacitance CS. For $t \ll RTCS$ the exponential can be approximated as $1 - (t/RTCS) + \ldots$, and

$$v(t) \approx VCC(t/RTCT)$$

Note again the underlying assumption of $CS \gg CT$.

A bootstrap circuit design is illustrated to the right. The switch is provided by a transistor driven between saturation (low collector-emitter voltage approximating zero volts) and cutoff (approximating an open-circuit) by a pulse voltage input. The base resistor is used to limit the base current to safe values.. Switching is done by a 0.3 millesecond pulse with a 1.5 millesecond period.

PSpice performance computations for the circuit are drawn below. Comparison of the computations against expectations is left as exercise.
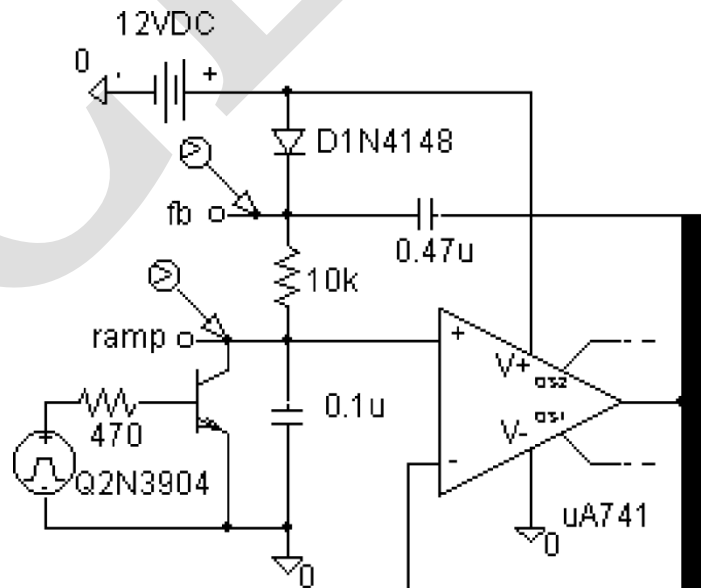
UNIT V-a
Synchronization and Frequency Division

Many types of waveform generators (sinusoidal generators, square-wave generators, sweep generators, etc) are used in pulse and digital circuits. These different waveform generators may have the same frequency. In many applications, these generators are required to run in synchronism or in step with another–which means that they should arrive at some reference point in their cycle at the same time. Alternately, it is also possible that these waveform generators may operate at different frequencies. Also, it is possible that one generator completes one cycle, whereas the other may complete an integral number of cycles (2, 3, ..., n) in the same time period. Still, it becomes necessary that these generators should run in synchronism, that is, they should arrive at some reference point in their cycles at the same time instant. Then these generators are again said to be running in synchronism, though with frequency division. In this chapter, we will discuss the methods of frequency synchronization and division using pulses and symmetric signals (sinusoidal signals) as synchronizing (sync) signals.

First, we consider the synchronization of relaxation circuits like sweep generators and multivibrators with pulses as synchronizing signals. Synchronization is possible only when the pulse amplitude is reasonably large and the repetitive frequency of the sync signal is greater than or equal to the frequency of the relaxation circuit. Also the synchronization with the division can only be achieved under certain conditions. However, when it comes to symmetric signals as sync signals, synchronization is always possible, may be with division. The various conditions under which synchronization takes place are discussed in detail.

PULSE SYNCHRONIZATION OF RELAXATION DEVICES

We are going to consider synchronization of the output of a UJT sweep generator using a pulse train. Consider a circuit where a capacitor charges during a finite time interval and the sweep is terminated abruptly by the discharge (relaxation) of the condenser. Such a circuit is called a relaxation circuit. Some relaxation circuits that we have already considered include sweep generators, blocking oscillators and multivibrators. Let us consider a UJT relaxation oscillator shown in Fig. 15.1(a).

Here, the UJT is simply used as a switch. Initially, let the capacitor be uncharged. When the switch is open the capacitor tries to charge to V_{BB}. The moment the voltage across C reaches V_P(peak voltage or the breakdown voltage of the UJT), the switch closes, allowing the charge on the capacitor C to discharge almost instantaneously. Again, when the voltage across C reaches V_V (valley voltage of the

UJT), the switch opens, once again the capacitor charges. This process is repeated, resulting in a waveform as shown in Fig. 15.1(b).
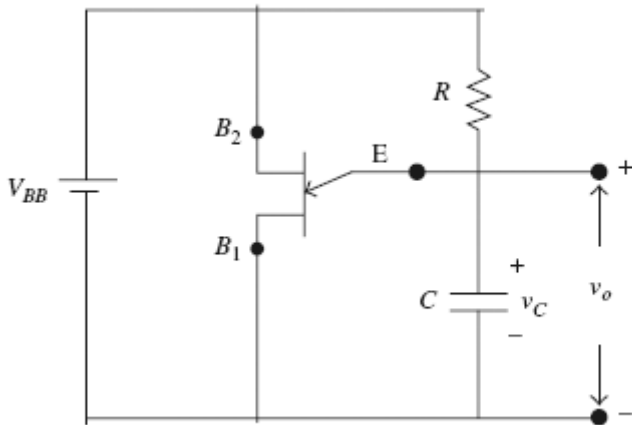
FIGURE 15.1(a) The UJT relaxation oscillator
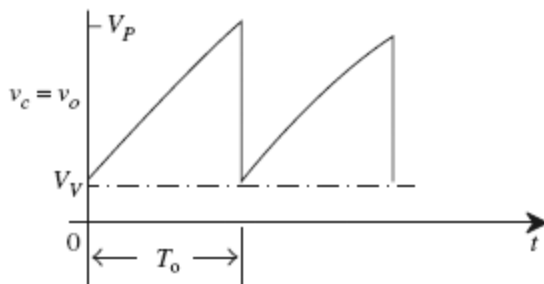
FIGURE 15.1(b) The output waveform

It is now required to synchronize the output of this relaxation oscillator with an external signal, called the sync signal. This sync signal, which is essentially a negative pulse train, is connected to the UJT circuit such that it changes its peak voltage V_P. Thus, in a UJT circuit, the sync signal (negative pulses) is applied at B_2 to lower V_P, as shown in Fig. 15.2. The resistances R_{B1} and R_{B2} are added in series with B_1 and B_2 respectively.

Let us try to visualize the situation when the synchronizing pulses are applied. As already mentioned, the effect of the sync pulses is to lower the peak or breakdown voltage of the UJT. A repetitive pulse train, having a certain amplitude is shown in Fig. 15.3(a), starting at $t = 0$. For the first few cycles the sweep generator runs at its natural frequency $f_o (= 1/T_o)$ with $V_p = V_o$ as its amplitude. The sweep signal and the pulse train run at different frequencies and no synchronization is established. At time $t = T$,

the negative pulse reduces the peak of the natural sweep and the relaxation device switches ON, thereby terminating the sweep prematurely. This results in a new sweep time of T_s, which is the same as the spacing between the successive sync pulses, T_p and has the amplitude V_s which is smaller than V_o. From now onwards, the sweep generator output and the pulse train run in synchronism, as shown in Fig. 15.3(a).

FIGURE 15.2 The synchronization of a relaxation device with external pulses
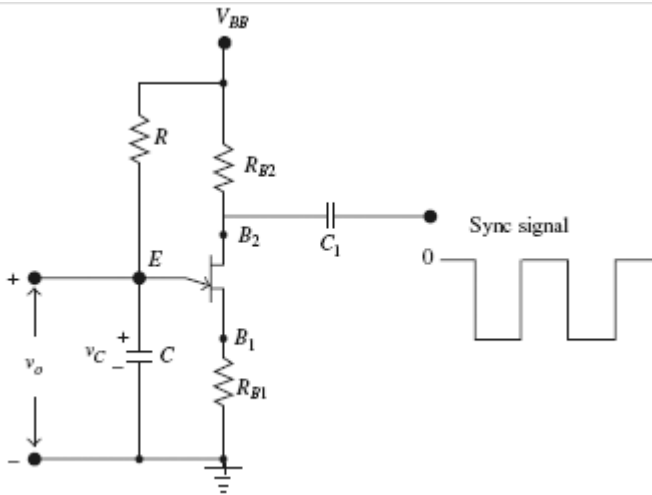
FIGURE 15.3(a) The synchronization takes place after a few cycles
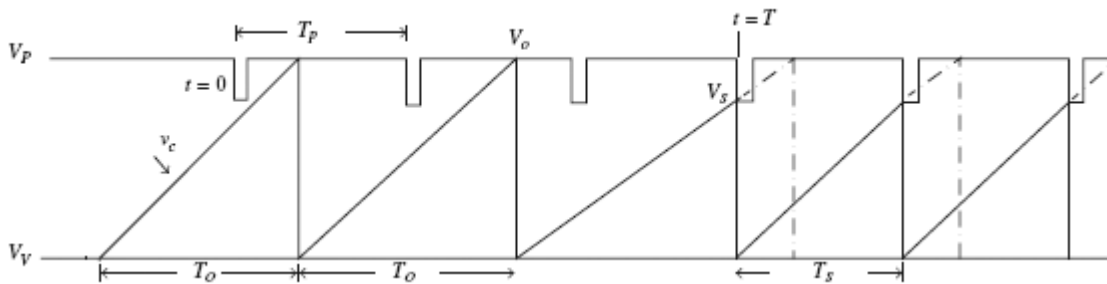
Thus, initially the two generators are not synchronized. However, the unsynchronized generators run in synchronism after a few cycles (from $t = T$ onwards). The synchronization takes place only when the sync pulses occur at the time when they would terminate the sweep cycle prematurely. This means that for synchronization to be possible, the interval between the pulses, T_p must be less than the sweep duration T_o. Once synchronization takes place the sweep duration changes to T_s and the sweep amplitude to V_s. Now consider a case where $T_p > T_o$, as shown in Fig. 15.3 (b).

Here, $T_p > T_o$ and sync pulses occur at such instants of time that they will not be able to prematurely terminate the sweep cycle. Hence, no synchronization is possible between these two waveform

generators. Obviously, synchronization cannot take place if T_p is greater than T_o. Let us consider another situation where $T_p < T_o$, but the amplitude of the sync pulses is small, as shown in <u>Fig. 15.3(c)</u>.

It is said that synchronization is possible when $T_p < T_o$. However, in the present case, as the amplitude of the sync pulses is small, they will not be able to prematurely terminate the sweep cycle. Hence, here again, no synchronization is possible. Thus, it may be inferred from this discussion that for synchronization to take place: (a) T_p must be less than or equal to T_o, and (b) the amplitude of the sync pulses should be large enough to bridge the gap between the quiescent breakdown voltage V_P and the sweep voltage v_c.

FIGURE 15.3(b) There is no synchronization for $T_p > T_o$
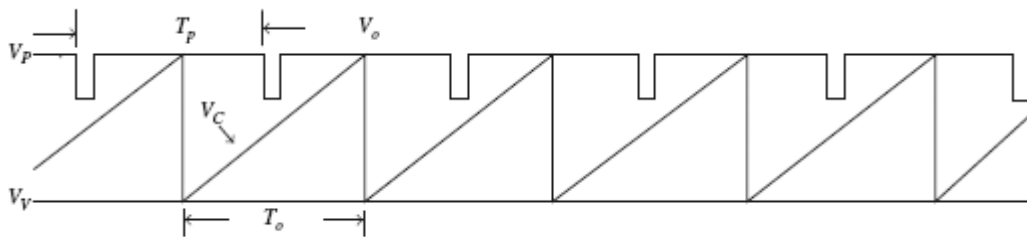
FIGURE 15.3(c) No synchronization is possible if the amplitude of the sync pulses is small
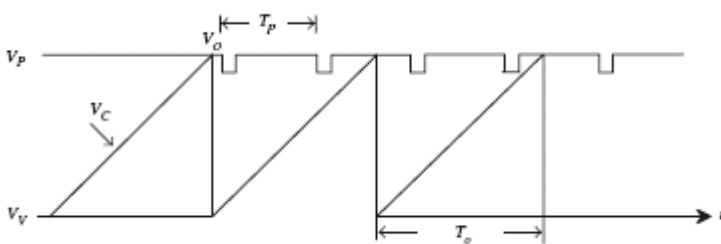
Frequency Division in a Sweep Circuit

Consider <u>Fig. 15.4(a)</u> in which $T_p < T_o$. We see that the first two pulses (marked 2 and 1) do not have sufficient amplitude so as to lower V_p and terminate the sweep cycle. Hence, there is no synchronization. However, the third pulse marked 2 though has the same amplitude as pulses marked 1, but occurs at such a time instant so as to be able to prematurely terminate the sweep cycle. The next sweep is initiated at this instant. However, the next pulse once again marked 1 may still have the same

amplitude as the rest of the pulses, but will not be able to terminate the sweep. Once again the next pulse marked 2 occurs at such an instant that its amplitude may still be sufficient enough to prematurely terminate the sweep. Thus, we see that only pulses marked 2 will be able to terminate sweep cycle and not the pulses marked 1. For every two sync pulses there is one sweep cycle and these two generators are seen to be running in synchronization. The sweep generator is now called a divider–the division being by a factor 2. There is one sweep cycle for every two sync pulses, i.e., $T_s/T_p = 2$, because $T_s = 2T_p$, where T_s is the sweep duration after synchronization and T_p is the spacing between the sync pulses.

Consider Fig. 15.4(b) where pulses marked 1 and 2 are not large enough to terminate the sweep cycle prematurely. Only when the amplitude of the pulse 1 is as large as V_1 and that for pulse 2, it is   they will be able to terminate the cycle prematurely to effect synchronization. However, pulses marked 3, though have the same amplitude, occur at such instants that they will be able to effect synchronization. Hence, for every three sync pulses the sweep generator completes one cycle. Therefore, the two generators are said to be synchronized with the frequency division being by a factor 3.
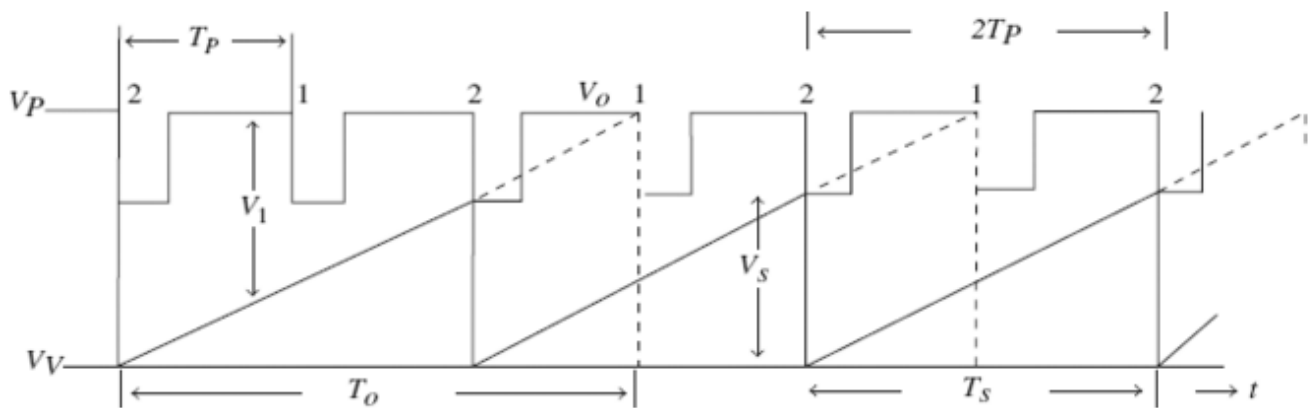
FIGURE 15.4(a) Frequency division by 2
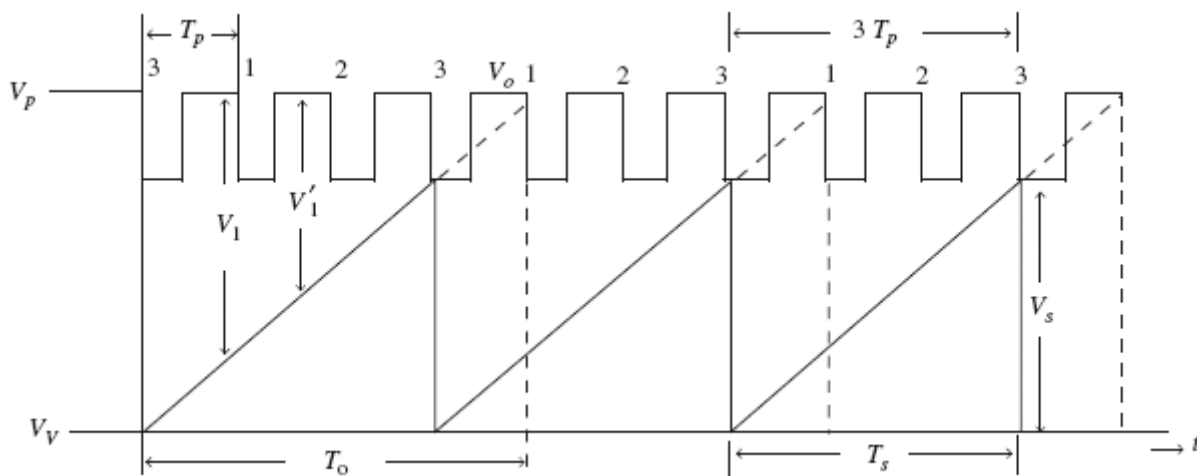
FIGURE 15.4(b) Frequency division by 3 in a sweep generator

We can infer from the previous conditions that:

(i) No synchronization is possible for pulses of smaller amplitude.

(ii) For a pulse amplitude large enough to prematurely terminate the sweep cycle, as T_p/T_s progressively decreases from 1 to 0, 1:1 synchronization holds, followed by 2:1 synchronization and then 3:1 synchronization and so on. T_S/T_p is called the counting ratio.

(iii) For a pulse amplitude that is very large, synchronization is always possible. As T_p/T_s decreases from 1 to 0, the division, however, changes from 1:1 to 2:1 to 3:1 and so on.

SYNCHRONIZATION OF OTHER RELAXATION CIRCUITS

Frequency synchronization and division is also possible using other relaxation circuits such as astable multivibrators and monostable multivibrators. We will consider the blocking oscillator circuits and conventional astable and monostable multivibators.

Synchronization of Astable Blocking Oscillators

Synchronization of the output of an astable blocking oscillator with frequency division by a factor of 5 using positive sync pulses is illustrated in Fig. 15.5(a). Q_2 acts as an inverter. The positive sync pulses that appear at the base of Q_2, after amplification and polarity inversion by the CE configuration, appear as negative pulses at the collectors of Q_1 and Q_2. Because of the polarity inversion by the pulse transformer, these negative pulses appear as positive pulses at the base Q_1 as per the chosen dot convention on the windings. Consequently, the base current of Q_1 increases, its collector current further rises, the voltage at the collector falls still further, the voltage at the base increases further and so on. A regenerative action takes place, the transistor Q_1 is quickly driven into saturation, and a pulse of duration t_p is generated. During this period of pulse generation, the capacitor C_1 charges, the voltage across the capacitor at $t = t_p$ being V_1, as shown in Fig. 15.5(b). As this voltage reverse-biases the base – emitter diode of Q_1, Q_1 now goes into the OFF state. As a result, the charge on C_1 discharges through R_1 and when the voltage across the capacitor terminals falls to $V_{BB} - V_\gamma$, then Q_1 is again ON and C_1 charges and this process is repeated. In the absence of sync pulses, a new sweep would have started at the voltage ($V_{BB} - V_\gamma$), at which voltage Q_2 would have normally gone into the ON state. The output would have a time period T_o, as shown in Fig. 15.5(b).
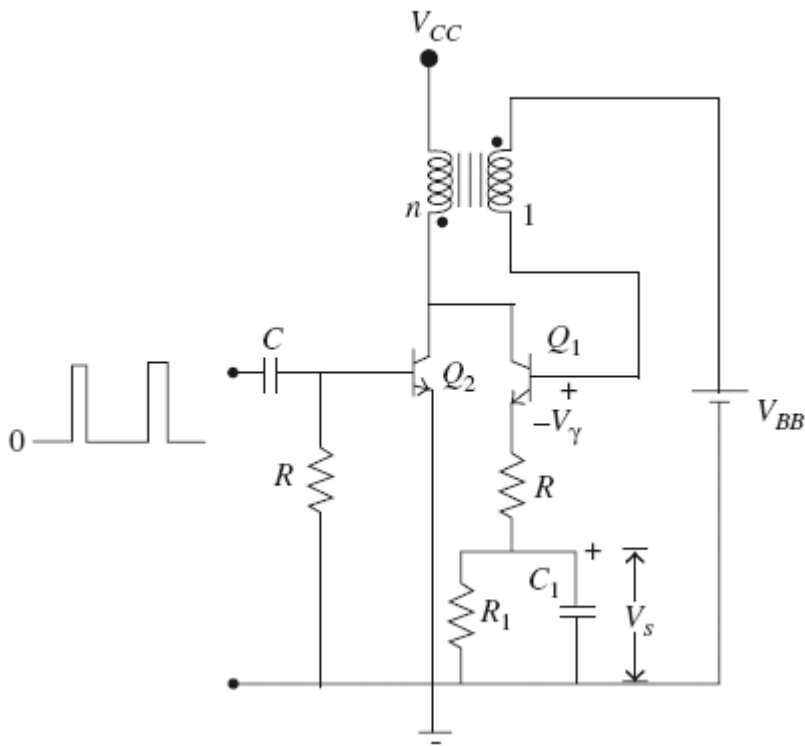
FIGURE 15.5(a) The sync signal applied to an astable blocking oscillator
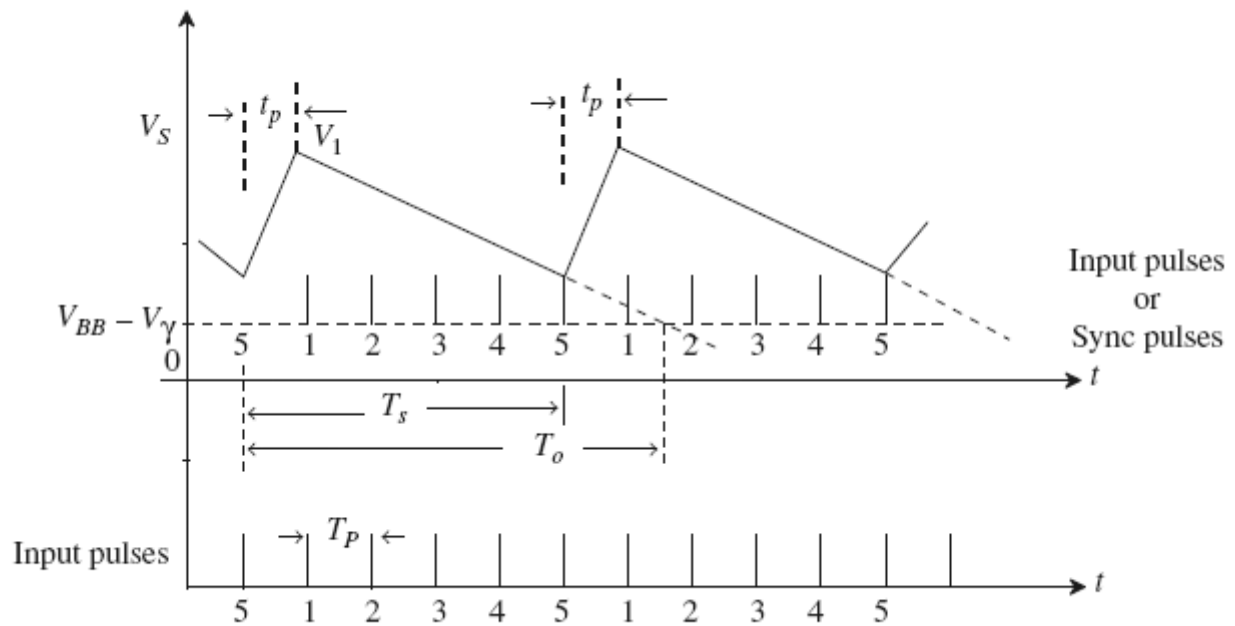
FIGURE 15.5(b) 5:1 synchronization in an astable blocking oscillator

However, the sync pulses appear as positive pulses at the base Q_1 (after polarity inversion in Q_2 and further polarity inversion in the pulse transformer). Pulses numbered 1, 2, 3 and 4 do not have sufficient amplitude to terminate the sweep prematurely. However, pulse 5 occurs at such an instant and has sufficient amplitude that it prematurely terminates the cycle as Q_2 goes into the ON state at the instant of occurrence of the 5th pulse, as regenerative action again takes place. C_1 again charges and so

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on. Thus, the cycle is prematurely terminated at T_s, and a new cycle starts. Synchronization with 5:1 division is accomplished. If, on the other hand, the amplitude of the sync pulses is increased, it could result in synchronization with 3:1 division, as shown in Fig. 15.5(c). Thus, we can say that with the proper spacing between the sync pulses (proper choice of pulse repetition frequency) and proper choice of amplitude for these pulses, it is possible to achieve synchronization with desired frequency division.

Synchronization of Transistor Astable Multivibrators

Synchronization with frequency division in a transistor astable multivibrator can be accomplished by applying either positive or negative pulses to both the transistors or to any of the transistors. Figs. 15.6 (a) and (b) depict the circuit and the waveforms to achieve synchronization with a frequency division of 6:1. Here, positive pulses are applied at the base B_1 of Q_1.

FIGURE 15.5(c) 3:1 synchronization in an astable blocking oscillator

FIGURE 15.6(a) An astable multivibrator with sync pulses applied at B_1
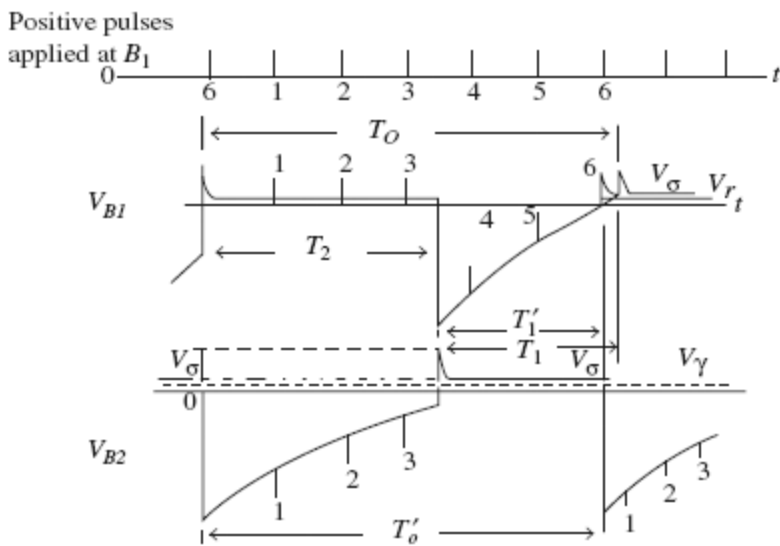
FIGURE 15.6(b) The waveforms of an astable multivibrator with positive sync pulses applied at B_1

In the absence of sync pulses, the astable must have had a time period T_o ($= T_1 + T_2$) when the cycle would have naturally terminated at V_{B1} or $V_{B2} = V_\gamma$. However, with sync pulses connected, the positive pulses applied at B_1 are amplified and inverted and appear as negative pulses at B_2. During T_2, the positive pulses at B_1 have no effect on the time period as Q_1 is already ON. Further the negative pulses 1, 2 and 3 appearing at B_2 will not be able to change T_2. Hence, T_2 remains unchanged. However, during the time period T_1, the pulses numbered 4 and 5 do not have sufficient amplitude to drive Q_1 into the ON state and terminate the time period T_1 prematurely. However, the 6th pulse has sufficient amplitude to prematurely terminate the time period T_1 as this pulse drives the base of Q_1 positive; and

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hence, Q_1 goes ON. The new time period for which Q_1 is OFF is   and the new sweep period is   . In this arrangement, the multivibrator completes one cycle for every six sync pulses. Although the complete period is synchronized, the individual time periods are not synchronized. T_2 is the same as without synchronization.

Synchronization with Division of an Astable Multivibrator by Applying Negative Pulses at both the Bases (B_1 and B_2)

If an astable multivibrator is required to be synchronized during both the time periods T_1, T_2 and also for T, then the negative pulses can be applied to both the bases B_1 and B_2 of transistors Q_1 and Q_2. Let it be assumed that both the time periods are required to be synchronized with a division of 3:1 so that the total period is synchronized with a frequency division of 6:1, as shown in Fig. 15.7.

The negative pulses applied at B_1 get amplified, inverted appear as positive pulses at the base B_2. Similarly, the negative pulses applied at B_2 get amplified and inverted and appear as positive pulses at the base B_1. Thus, the positive pulses superimposed on the exponential portion of the waveform at B_2 during T_2 are a combination of negative pulses applied directly and the inverted and amplified negative pulses from the other transistor which appear as positive pulses. The pulses marked 1 and 2 do not have sufficient amplitude. However, the pulse marked 3 has an amplitude that can terminate T_2 earlier, resulting in a new time period   . Similarly, during the period T_1 when Q_1 is OFF, pulses marked 4 and 5 will not have any influence on the time period T_1. However, the pulse numbered 6 will terminate T_1 prematurely, resulting in a new time period   . Each of these time periods are individually synchronized with a frequency division of 3:1 as the third and the sixth pulses prematurely terminate the time periods T_2 and T_1. Hence, synchronization with a division of 6:1 occurs for the entire time period T of the astable multivibrator.

15.3.4 Positive Pulses Applied to B_1 Through a Small Capacitor from a Low-impedance Source

Synchronization with the division of both the time periods of an astable multivibrator can be achieved by applying the positive pulses to only one base instead of at both the bases, say, B_1. During the period when Q_1 is ON, as its input resistance is very small, the time constant of the pulse input is also very small. This RC circuit behaves as a differentiator and the pulse is quasi-differentiated. The negative spikes in this differentiated signal at B_1 of Q_1 appear as the positive spikes during the exponential variation at B_2. Pulses 1 and 2 may not be able to drive Q_2 ON and terminate T_2 prematurely. However, the positive spike appearing at the trailing edge of the pulse numbered 3 will prematurely terminate the OFF period T_2 of Q_2. The new time period for which Q_2 is OFF is T_2'. During the exponential variation of the voltage at B_1 during T_1, the positive pulses are superimposed and at the leading edge of the pulse numbered 6, the OFF period of Q_1 is prematurely terminated. The new time period for which Q_1 is OFF is T_1. The original time period of the astable multivibrator was $T (= T_1 + T_2)$. Whereas,

the new time period after synchronization is T' $(= T_1^1 + T_2^1)$. Thus, not only the entire cycle with time period T of the astable is synchronized with a frequency division of 6:1 but the individual time periods   and   are also synchronized with a division of 3:1, as shown in <u>Fig. 15.8</u>.
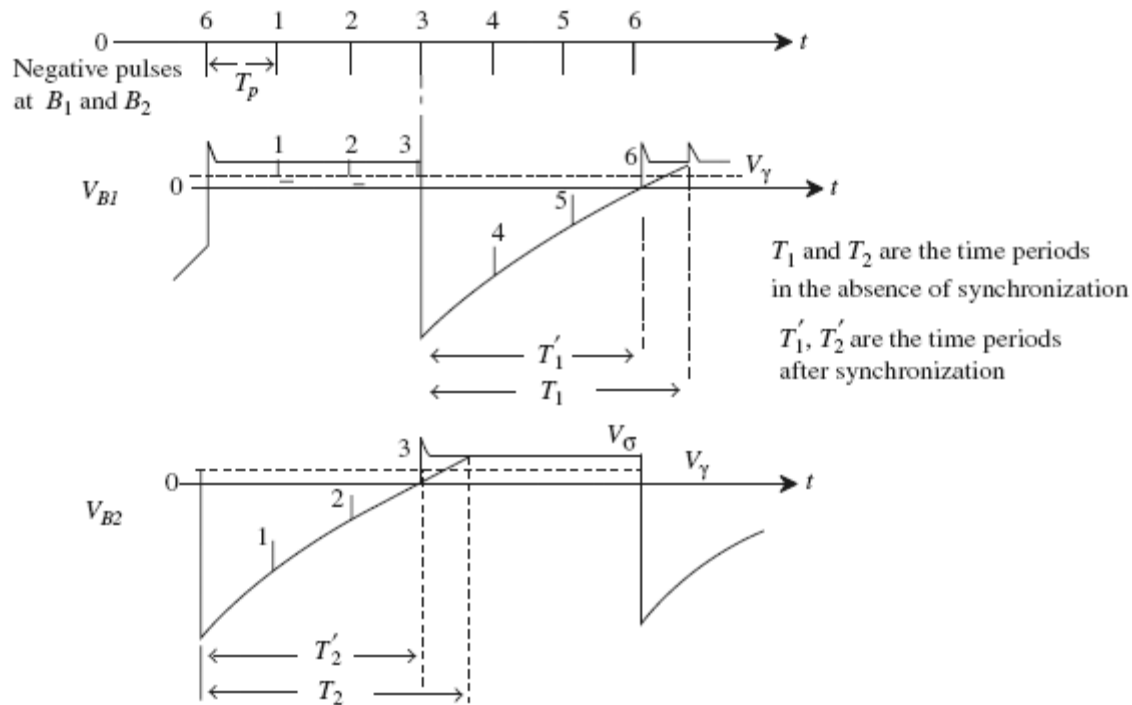
FIGURE 15.7 The synchronization of individual periods and the total period with a division of 6:1

A MONOSTABLE MULTIVIBRATOR AS A DIVIDER

A monostable multivibrator can be used for synchronization with frequency division [see <u>Fig. 15.9(a)</u>] and the waveforms are shown in <u>Fig. 15.9(b)</u>. Here, the positive pulse train is applied at B_1 through a small capacitance from a low impedance source.

The positive pulse train applied at B_1 gets quasi-differentiated as discussed earlier in the<u>Section 15.3.4</u>. The negative spikes at the trailing edge of the pulses are amplified and inverted and appear as the positive spikes at B_2. As a result, positive spikes due to the second pulse will prematurely terminate the time period resulting in synchronization with the frequency division of 2:1. On the other hand, if the amplitude of the pulses is large enough, pulse 1 may prematurely terminate the time period, thereby changing the counting ratio from 2 to 1.

A Relaxation Divider that Eliminates Phase Jitter

When a pulse train is applied to a divider, there could be a small time delay by the time it appears at the respective bases to cause a possible premature change in the state of the devices. This delay is called the phase delay. Also, as the pulse train is coupled to the divider circuit through an RC circuit, it could result in pulses having a finite rise time, Further the divider may have a certain response time which is liable to change with the frequency of the sync signals and the time constants associated with the circuit. As a result, this signal can influence the instant at which the base waveform would drive the device OFF. The phase delay could also be due to the variations in the device characteristics, supply voltages and the noise in the circuit. The phase delay that varies due to the cumulative effect of all these factors is termed as phase jitter. The frequency division without the phase jitter can be implemented using the schematic arrangement shown in Fig. 15.10.
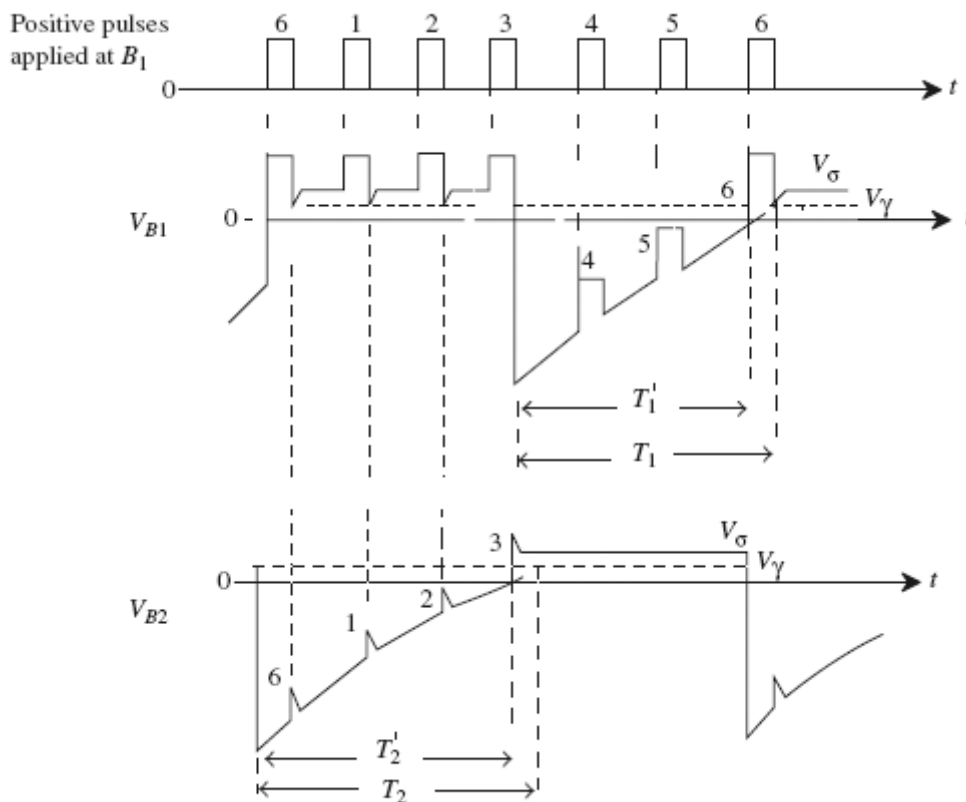
FIGURE 15.8 The synchronization of both the portions of astable multivibrators with positive pulses applied at B_1 through a small capacitor and low impedance source

The waveforms are shown in Fig. 15.11. The input to the divider is a train of pulses. The divider is an n:1 divider, i.e., for every n pulses, the nth pulse is obtained at the output of the divider. This n^{th} pulse is applied as a trigger to the monostable multivibrator which generates a gated output, that is, a pulse of duration T. This pulse of duration T controls the sampling gate. A sampling gate is one which transmits the input to its output as long the enabling signal (the gating signal) is present.

For the rest of the duration, there is no output for the sampling gate. As only the output of the divider (n^{th} pulse) triggers the monostable multivibrator, a pulse of duration T occurs only at the end of the nth pulse. Though a sequence of pulses is present at the input of the sampling gate, only the pulse marked 1 is transmitted to the output, as during the occurrence of this pulse the sampling gate is enabled. The output consists of the pulses labeled 1 only. By adjusting the pulse width of the gating signal such that $T_p < T < 2\,T_p$, we can ensure that the nth pulse does not pass to the output of the sampling gate. Thus, phase jitter can be eliminated.
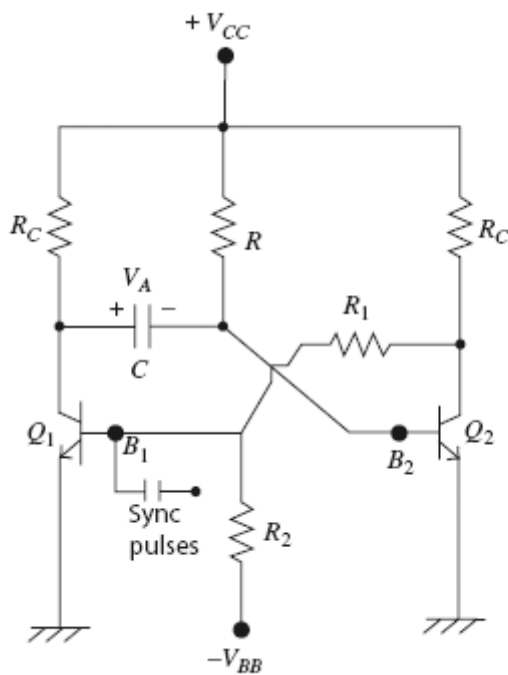
FIGURE 15.9(a) A monostable multivibrator
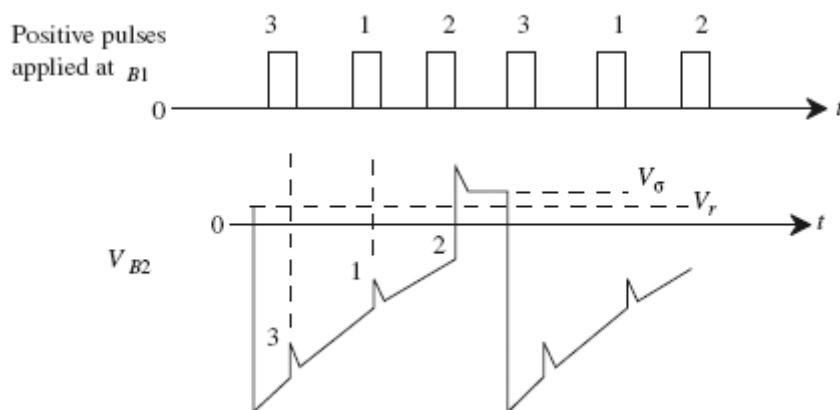
FIGURE 15.9(b) The waveform at B_2
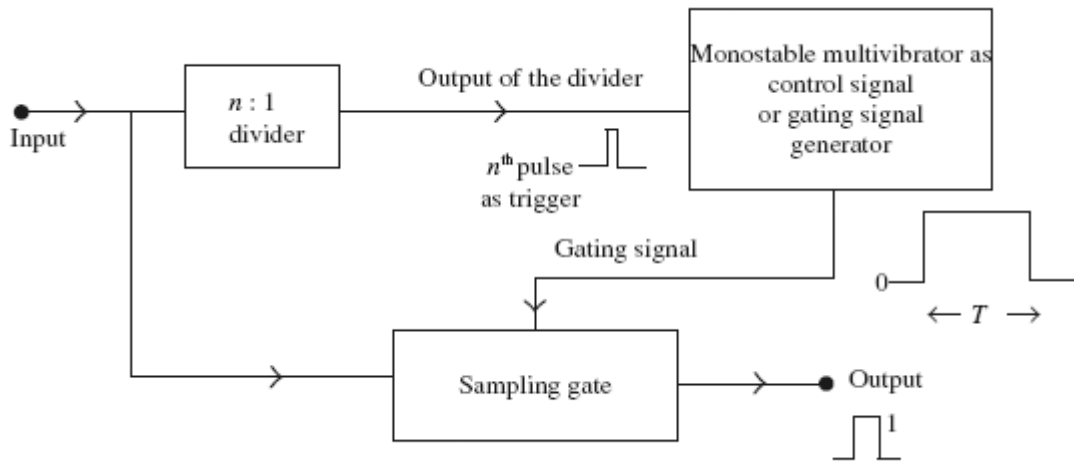
FIGURE 15.10 The frequency division without the phase jitter
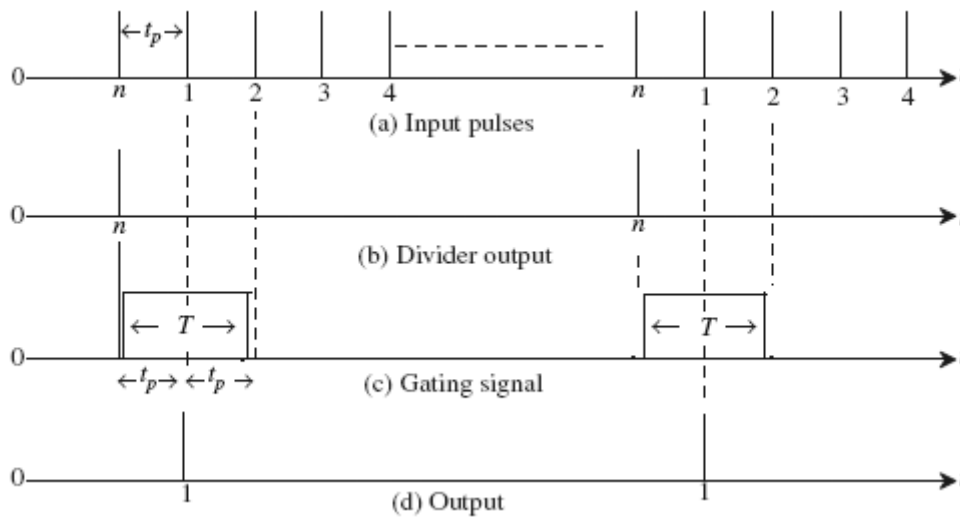
FIGURE 15.11 The waveforms of the divider that eliminates the phase jitter

Stability of the Relaxation Divider. In a frequency divider, due to phase jitter, if the nth pulse is required to prematurely terminate a sweep cycle, it is possible that either the $(n-1)^{th}$ pulse or even the $(n-2)^{nd}$ pulse may terminate a sweep cycle. This accounts for the instability of the natural timing period of the oscillator, which in turn may cause a loss of synchronization or an incorrect division ratio. The typical voltage variation at the base of an astable multivibrator is shown in <u>Fig. 15.12</u>.

In order to calculate the time period of a monostable multivibrator, we use the relation: $v_o(t) = v_f - (v_f - v_i)e^{-t/\tau}$ where, v_i is the initial voltage from which the charge on the capacitor discharges and v_f is the final voltage to which the capacitor would discharge, if allowed to discharge, as $t \to \infty$. Assuming that τ remains fairly constant, it is the changes in v_i and v_f and $v_C(= V_\gamma)$ that could be responsible for the instability of the natural period. Let us consider the influence of these factors on the natural time period of the monostable multivibrator:

(i) The parameters of the transistor are likely to change due to temperature variations. Also, if the existing transistor is replaced by another for some reason the transistor parameters may be affected. This could influence v_i and v_C, the voltage at which the period terminates. v_C can be the cut in the voltage of a transistor (V_γ) and v_f can change due to loading. Normally, a regulated power supply with sufficient current rating is used for v_f. Hence, the instability of the time period T_o due to the variation of v_f can be minimized or eliminated. The time period T_o can now mainly change due to the variations in v_i and v_C. However, the choice of v_f may influence the natural time period.

ii) Let us consider the case when v_f is a large value, say, v_{f1} (curve 1). Then the variation between v_i and v_C can be approximately linear. Consequently, the change in T_o due to variation in v_C can be minimized to some extent. However, in curve 1, if v_i changes by a larger amount than v_C (with the same τ), then choosing a larger value of v_f may again give rise to instability of the time period.

iii) On the contrary, if v_f is reduced to v_{f2}, the variation of the voltage between v_i and v_C is exponential in nature and hence, non-linear. Now if v_i varies, then a given percentage change in ($v_C - v_i$) could cause a lesser percentage change in T_o (curve 2).
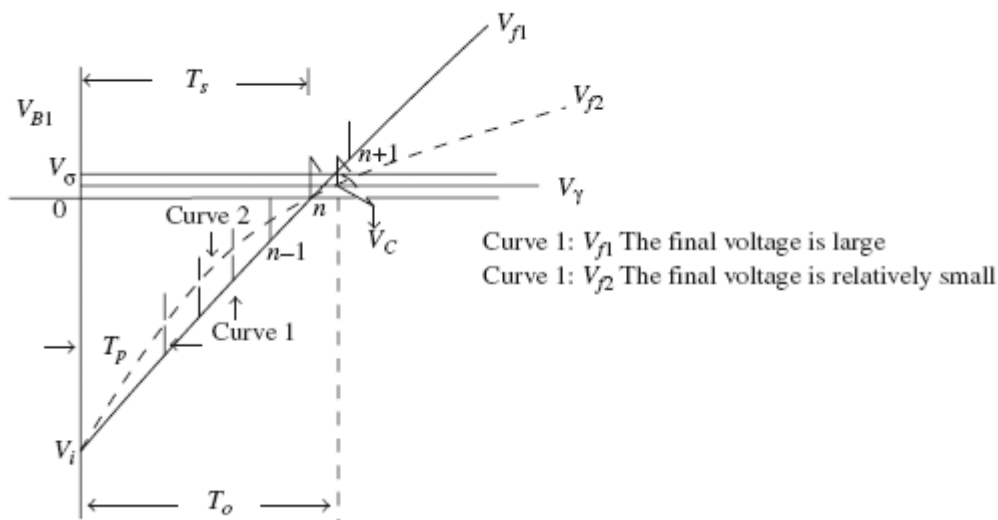
FIGURE 15.12 The factors that account for the instability of a relaxation divider

Hence, the variation in T_o i.e., instability of the time period, can be minimized by the proper choice of v_f, depending on whether the instability has occurred either due to the variation in v_C or v_i.

SYNCHRONIZATION OF A SWEEP CIRCUIT WITH SYMMETRICAL SIGNALS

So far, we have considered the synchronization of relaxation circuits with external sync signals that are essentially pulses only. However, we can also synchronize a relaxation circuit such as a sweep generator with sync signals that could as well be gradually varying signals like sinusoidal signals. Let us consider the output of a UJT sweep generator that is to be synchronized with a slowly varying sinusoidal signal, as shown in Fig. 15.13(a).

Let it be assumed that the breakdown voltage of the UJT varies sinusoidally in the presence of the sync signal. Here, V_{po} is the quiescent breakdown voltage of the UJT and V_p is the breakdown voltage in the presence of the sync signal. It is possible that synchronization can be effected with $T = T_o$. If this happens, then the period of the sweep is not altered by the sync signal and the sweep amplitude is also unaffected. The sweep cycle, as a result, terminates at V_{po}, which means that the sweep terminates on its own at points labeled 'o' in Fig. 15.13(a).

Earlier, when synchronization was achieved using a pulse train as sync signals, it was observed that for synchronization to take place it was imperative that the spacing between pulses (T_p) should be less than or equal to the natural time period (T_o) of the relaxation circuit. It was also observed that a pulse could prematurely and reliably terminate a sweep cycle (reduce the sweep duration) but will not be able to extend the sweep duration. However, when it is a case of synchronization with symmetric signals, synchronization is always possible whether T (T_p in the case of a pulse train) is less than or equal to T_o or T is greater than T_o.
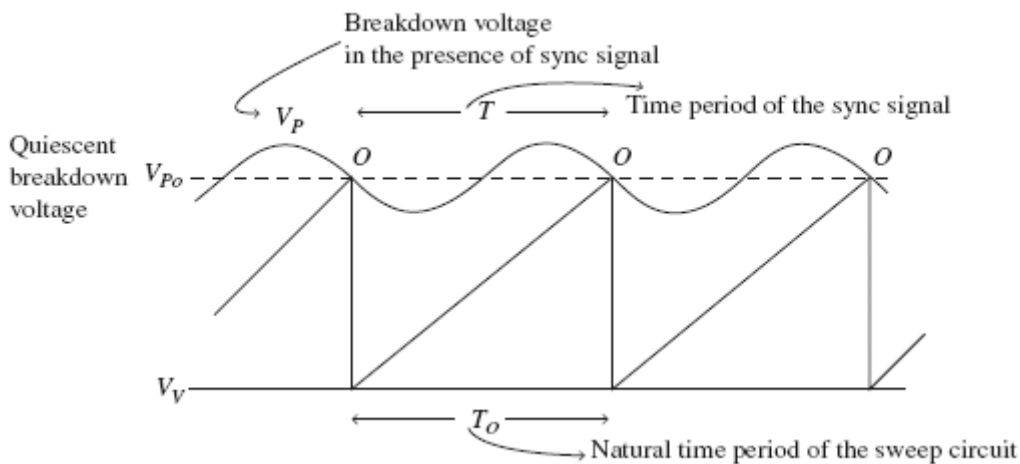
FIGURE 15.13(a) The synchronization of a sweep generator with sinusoidal sync signal

It is seen from Fig. 15.13(b) that if the sweep voltage meets the V_P curve at a point above V_{po} for $T > T_o$, say X, then the duration of the sweep is lengthened ($> T_o$). On the other hand, if the sweep voltage meets the V_P curve at a point below V_{po} for $T < T_o$, the duration of the sweep is shortened ($< T_o$).

(i) When $T = T_o$

(ii) When $T > T_o$

(iii) When $T < T_o$
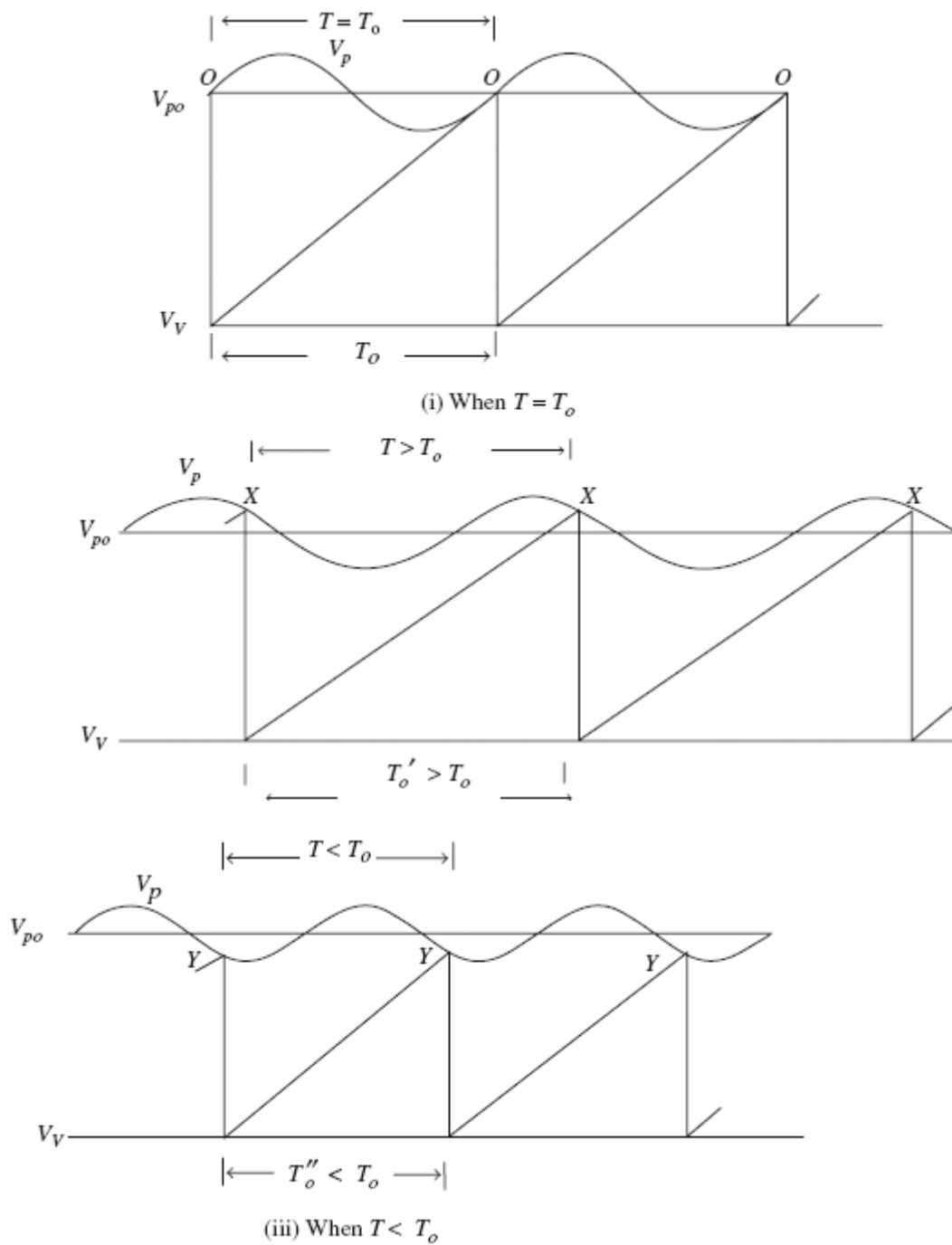
FIGURE 15.13(b) The timing relationship between the sweep voltage and the time-varying breakdown voltage when (i) $T = T_o$, (ii) $T > T_o$, then $\quad > T_o$ and (iii) $T < T_o$, then $\quad < T_o$

Let us summarize this with the help of Fig. 15.13(c):

1. When $T = T_o$, the sweep is terminated at 'o' on the V_{po} line, leaving the period and the amplitude of the sweep unaltered.

2. When $T > T_o$, if the sweep terminates at a point say, X that lies between 'o' and positive maximum, at A, then the sweep is lengthened and its duration $\quad$ is greater than T_o. This lengthening is maximum when the sweep terminates at A.

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3. When $T < T_o$, if the sweep terminates at a point, say Y, that lies between 'o' and the negative maximum at B, then the sweep is shortened and its duration   is smaller than T_o. This shortening is maximum when the sweep terminates at B. To calculate the range of synchronization let us consider an example.
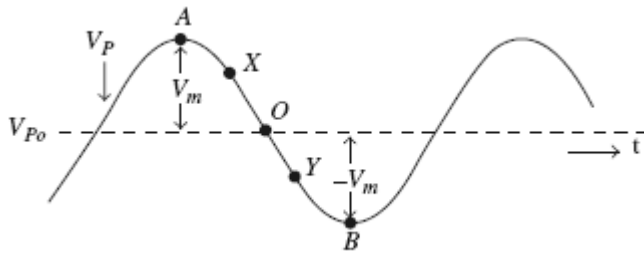
FIGURE 15.13(c) The synchronization when $T \neq To$

EXAMPLE

Example 15.1: A UJT sweep operates with a valley voltage of 4 V and peak voltage of 16 V. A sinusoidal synchronizing voltage of 3 V peak is applied as a sync signal. $\eta = 0.5$. If the natural frequency of the sweep is 1 kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronization with the sync signal.

Solution:

The quiescent breakdown voltage, $V_{po} = 16$ V.

Peak-to-peak amplitude of the synchronizing signal = 3 V

In the absence of the sync signal, the peak-to-peak swing of the sweep = $V_{po} - V_V = 16 - 4 = 12$ V

In the presence of the sync signal, the sweep amplitude must therefore lie in the range

$(12 - 1.5) = 10.5$ V and $(12 + 1.5) = 13.5$ V.

Time period of the sync signal,

Amplitude of the natural sweep signal = $16 - 4 = 12$ V.

And this sweep amplitude is generated in 1ms. Therefore, the time required to generate a sweep of, 10.5 V is

and the corresponding frequency is,

The time required to generate a sweep of 13.5 V is

and the corresponding frequency is

It is seen from the above calculations that the sweep generator remains synchronized as the frequency of the sync signal varies from 889 c/s to 1143 c/s.

Frequency Division with Symmetric Sync Signals

Let us now consider the operation of a sweep circuit as a frequency divider using sinusoidal signal as sync signal, as shown in <u>Fig. 15.14(a)</u>. The solid lines represent the sweep with a time period T_o and the sync signal with a time period T. The natural sweep terminates on V_{po} line. In the presence of the sinusoidal sync signal, if the sweep meets the sync signal above the V_{po} line at X, the new time period of the sweep is T_s. Thus, the sweep period T_o changes to T_s as a result of the sync signal. The sync signal completes three cycles during the period T_s, resulting in the division by a factor 3 as $T_s = 3T$ (counting ratio of 3).

If now the amplitude of the sync signal is increased (dashed line), keeping the time period the same as T, as shown in <u>Fig. 15.14(b)</u>, the sweep meets the sync signal at Y between O and B. The duration of the sweep is shortened (dashed line) resulting in a 2:1 synchronization (a counting ratio of 2). If the amplitude of the sync signals further increases, it could result in a counting ratio of 1. Hence, this circuit can operate as a counter.

Increasing the amplitude of the sync signal, in principle, can cause 1:1 synchronization. The sweep is terminated prematurely when it meets the sync signal below the V_{po} line. Beyond this point once again the sweep voltage increases and this time it will terminate on the sync signal above the V_{po} line. Therefore, the actual sweep waveform consists of the alternate sweeps of short and long durations. The

suggestion therefore is that if this sweep is used to cause deflection of the electron beam along the X-axis in a CRO, it is preferable to use a sync signal of smaller amplitude, as shown in Fig. 15.14(c).
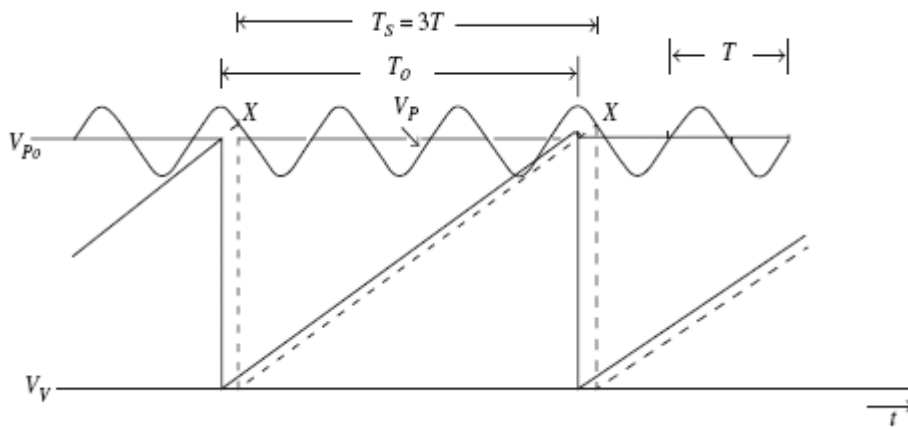
FIGURE 15.14(a) 3:1 synchronization of the sweep with symmetric sync signal
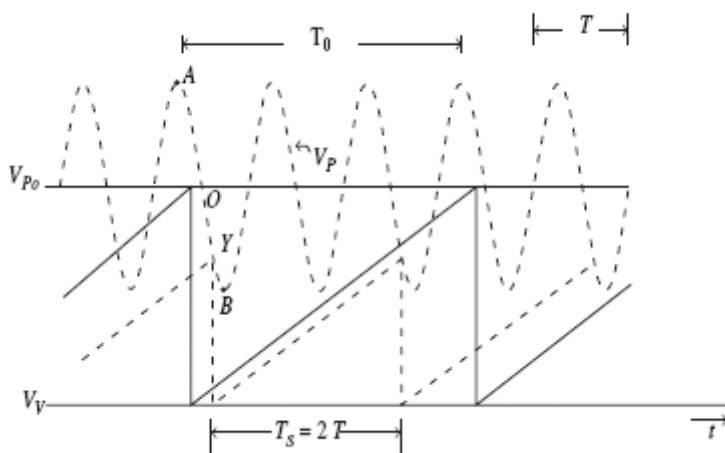
FIGURE 15.14(b) 2:1 Synchronization of the sweep with a symmetric sync signal
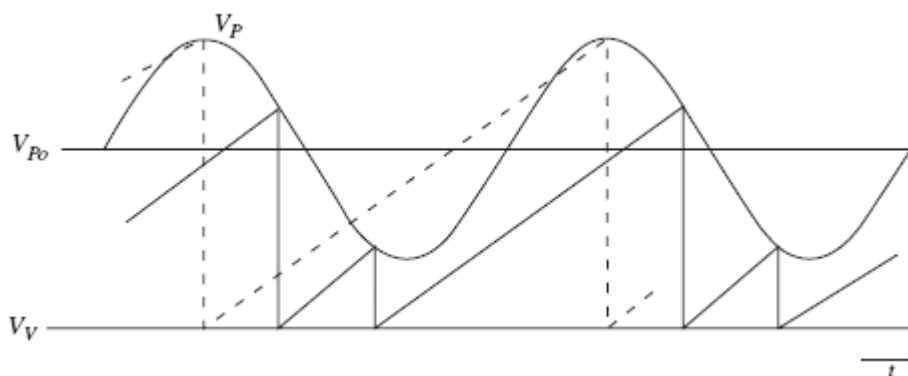
FIGURE 15.14(c) The excessive amplitude of the sync signal in a sweep resulting in sweeps of long and short durations

UNIT V - b
Realization of logic gates using diodes & transistor

INTRODUCTION

In digital applications, data is in the form of binary bits—0s and 1s. A logic gate is a digital circuit that gives a specific discrete output (0 or 1) depending on the input conditions. These logic gates can be wired using discrete components such as resistors, diodes, transistors, FETs, and their combinations. The simplest logic gate, say a two-input AND / OR gate (diode–resistance logic gate), may be constructed using two diodes, a resistance and a dc source. The important logic families are diode–transistor logic (DTL), transistor–transistor logic (TTL), p-channel and n-channel MOSFET logic (PMOS and NMOS) and complementary MOSFET logic (CMOS). The TTL family is further subdivided into open-collector TTL, emitter-coupled logic (ECL) or integrated injection logic (I^2L). TTL and CMOS are the two most important logic families. TTL gates are preferred where there is a need for faster switching speed and CMOS gates are used where the requirement is lower power dissipation per gate. The suitability of a logic gate, for a specific application, is evaluated in terms of the number of requirements. This chapter presents the relative performance of these gates. Also, sometimes, it becomes necessary to connect the output of one type of gate (say, a TTL gate which operates with a 5 V supply) to the input of another gate (say, a CMOS gate that operates with a 30 V supply). In such cases, the output requirements of the driving gate should be compatible with the input requirements of the driven gate. Hence, interfacing methods are also discussed. Normally, designing and constructing logic gates using discrete components is meaningful only for small circuits. As the complexity increases, these circuits are best fabricated on a chip called the digital integrated circuit. Depending on the level of integration, these are classified as under:

1. Small-scale integration (SSI): 1 to 20 gates or transistors per package
2. Medium-scale integration (MSI): 20 to 200 gates or transistors per package
3. Large-scale integration (LSI): 200 to 200,000 gates or transistors per package
4. Very large-scale integration (VLSI): More than 1 million gates or transistors
5. Ultra large-scale integration (ULSI): 1 billion gates or transistors

LOGIC GATES

A logic gate is a circuit that gives either '0' (LOW) level or '1' (HIGH) level at the output, depending on the input conditions. The basic logic gates can be wired using discrete components

such as resistors, diodes, transistors and FETs. The wiring of a complex gate circuit is unthinkable using discrete components. When the complexity of the gate circuit increases, it is preferable to wire the logic gate in an integrated circuit form. In this section, we basically describe the different types of logic gates using discrete components only, in order to understand the principle of operation of logic circuits of different logic families.

Simple Diode Gates

AND and OR are the two basic gates from which NAND and NOR gates can be derived. Here, we describe two types of diode gates—diode AND gates and diode OR gates.

Diode AND Gates. An AND gate is a digital circuit which gives a high output only when all the inputs are simultaneously high (1), otherwise the output is low (0). Consider a simple two-input AND gate using diodes (See Fig. 10.1).

Assuming D_1 and D_2 to be ideal diodes, the following cases are possible:

1.   Both the inputs are zero, the diodes are ON and $V_o = 0$.
   2. $V_1 = 0$, $V_2 = 1$, D_1 is ON, D_2 is OFF, $V_o = 0$.
   3. $V_1 = 1$, $V_2 = 0$, D_1 is OFF, D_2 is ON, $V_o = 0$.
   4. $V_1 = 1$, $V_2 = 1$, D_1 and D_2 are OFF, $V_o = 1$.

The truth table for the gate is given in Table 10.1. The schematic representation of the AND gate is shown in Fig 10.2(a).

The timing diagram for the two-input AND gate is shown in Fig 10.2(b). As mentioned in the preceding section, in an AND gate, the output is 1 only when all the inputs are 1 and, 0 if any one of the inputs is 0. Hence, in Fig. 10.2(b), at the instant T_0, when both the inputs V_1 and V_2 are 0, the output $V_o = 0$. At T_1, $V_1 = 0$ and $V_2 = 1$. Since one of the inputs is zero, the output $V_o = 0$. At the instant T_3, $V_1 = 1$ and $V_2 = 1$. Since both the inputs are 1, the output $V_o = 1$ and so on. In general, there can be a large number of inputs to a gate. A NOT gate, also called an inverter in digital circuits, is schematically represented as in Fig. 10.2(c). Figure 10.2(d) shows the timing diagram for a NOT gate.

TABLE 10.1 The truth table for the AND gate

V1	V2	V_o
0	0	0
0	1	0
1	0	0
1	1	1
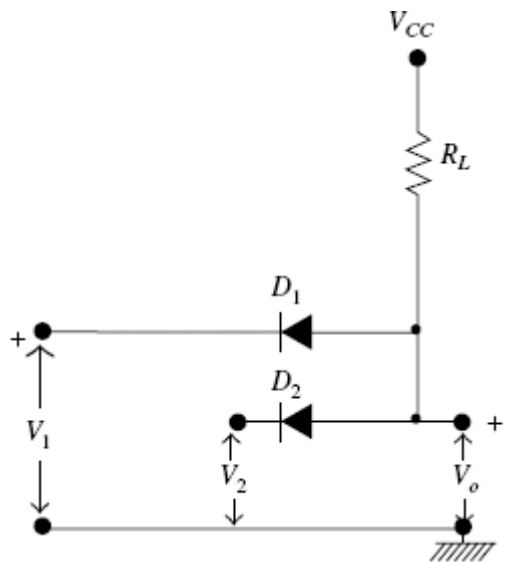
FIGURE 10.1 A two-input AND gate
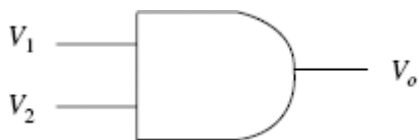
FIGURE 10.2(a) The schematic diagram for the two-input AND gate
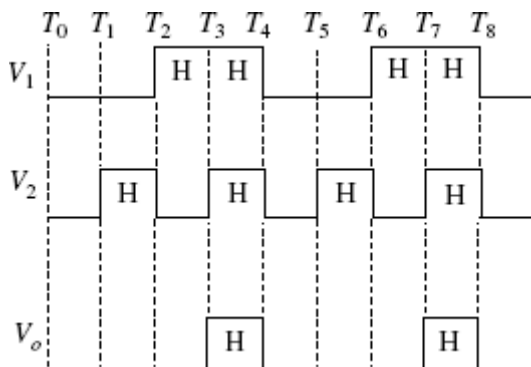
FIGURE 10.2(b) The timing diagram for two-input AND gate
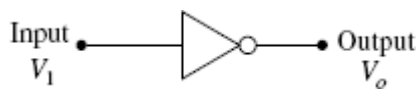
FIGURE 10.2(c) A NOT gate
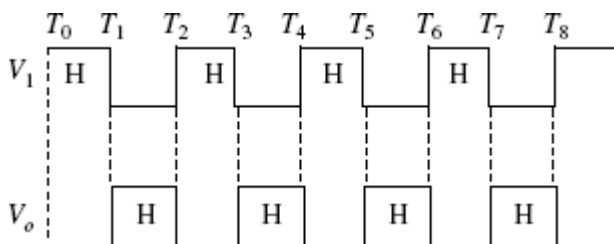
FIGURE 10.2(d) The timing diagram for a NOT gate
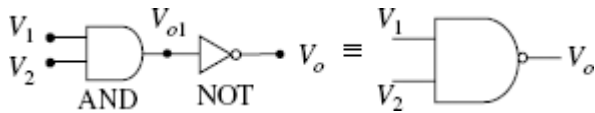
FIGURE 10.3(a) A NAND gate

In a NOT gate, the output is the complement of the input. This means, that if the input is 1, the output is 0; and if the input is 0, the output is 1. At T_o, the input $V_1 = 1$; therefore, the output $V_o = 0$. At T_1, the input $V_1 = 0$ and output $V_o = 1$ and so on.

An AND gate cascaded with a NOT gate is called a NAND gate. Figures 10.3(a) and (b) show the schematic representation and the timing diagram of a NAND gate, respectively.

In a NAND gate, the output is 0 only when all the inputs are 1. If any one of the inputs is 0, the output is 1. As shown in Fig. 10.3(b), at the instant T_o, both the inputs V_1 and V_2 are 0 and therefore, the output V_o is 1. At T_1, $V_1 = 0$ and $V_2 = 1$. Since one of the inputs is 0, the output V_o is 1. At T_3 both the inputs V_1 and V_2 are equal to 1 and therefore the output $V_o = 0$.

Diode OR Gates. An OR gate is a digital circuit which gives a high output when either one or all the inputs are high (1). In other words, the output is low (0) only when both the inputs are low. A two-input diode OR gate is shown in Fig. 10.4. Here too, we assume the diodes to be ideal. The following cases are possible:
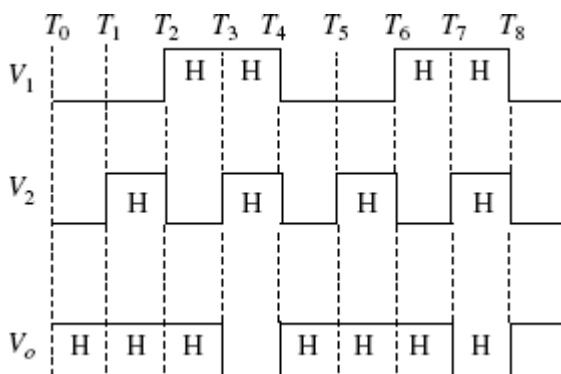
FIGURE 10.3(b) The timing diagram for a NAND gate

1. $V_1 = V_2 = 0$, D_1 and D_2 are OFF, $V_o = 0$
2. $V_1 = 0$, $V_2 = 1$, D_1 is OFF, D_2 is ON, $V_o = 1$
3. $V_1 = 1$, $V_2 = 0$, D_1 is ON, D_2 is OFF, $V_o = 1$
4. $V_1 = 1$, $V_2 = 1$, D_1 and D_2 are ON and $V_o = 1$

The truth table for an OR gate is shown in Table 10.2. An OR gate is schematically represented as in Fig. 10.5(a).
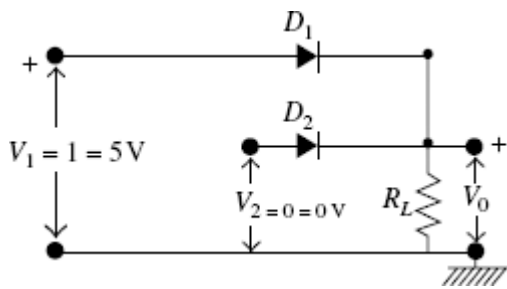
FIGURE 10.4 The two-input diode OR gate

The timing diagram for a two-input OR gate is shown in Fig. 10.5(b). In an OR gate, when any one of the inputs is 1, the output is 1. It is 0 only if all the inputs are 0. Hence, in Fig. 10.5(b), at the instant T_0, both the inputs V_1 and V_2 are 0; therefore, the output V_o is 0. At T_1, V_1 is 0 whereas $V_2 = 1$. Since one of the inputs is 1, the output $V_o = 1$. At the instant T_3, V_1 is 1 and V_2 is 1. Since both the inputs are 1, the output $V_o = 1$. An OR gate cascaded with a NOT gate is called a NOR gate, as represented in Fig. 10.6(a). Its timing diagram is shown in Fig. 10.6(b).

The output of a NOR gate is 1 when all the inputs are 0. When any one of the inputs is 1, the output is 0. Therefore, in Fig. 10.5(b), at the instant T_0, when both the inputs V_1 and V_2 are 0, the output of the NOR gate is $V_o = 1$. At T_1, $V_1 = 0$ and $V_2 = 1$; since one of the inputs is 1, the output V_o is 0. At T_3, both the inputs V_1 and V_2 are equal to 1; therefore, the output V_o is 0.

TABLE 10.2 The truth table for an OR gate

V1	V2	Vo
0	0	0
0	1	1
1	0	1
1	1	1

FIGURE 10.5(a) An OR gate
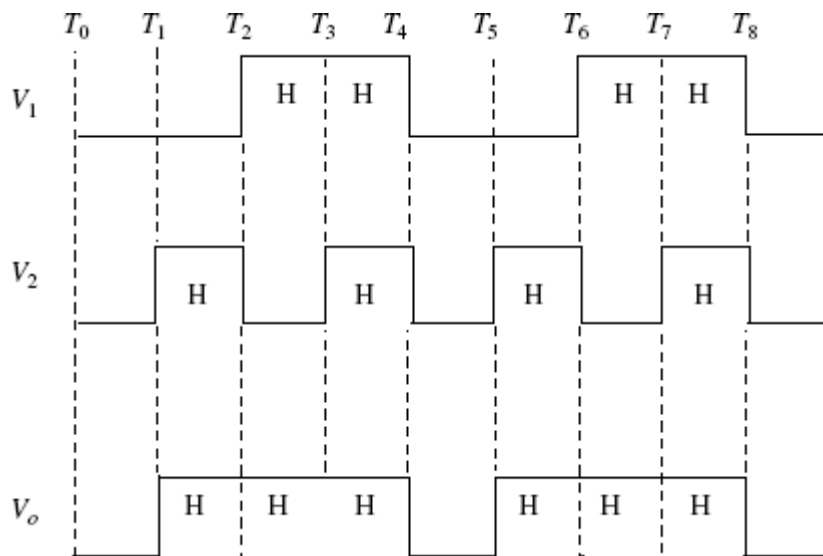
FIGURE 10.5(b) The timing diagram for a two-input OR gate
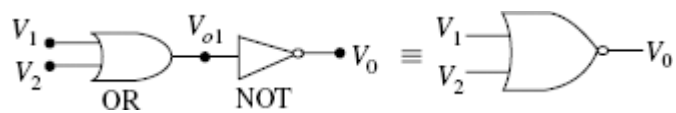
FIGURE 10.6(a) A NOR gate
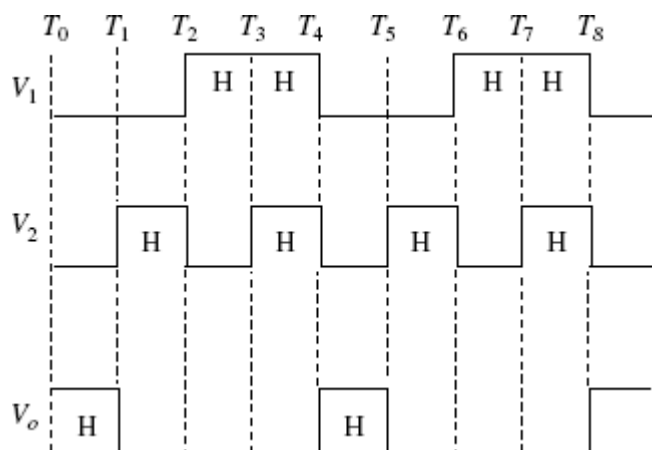
FIGURE 10.6(b) The timing diagram for a NOR gate
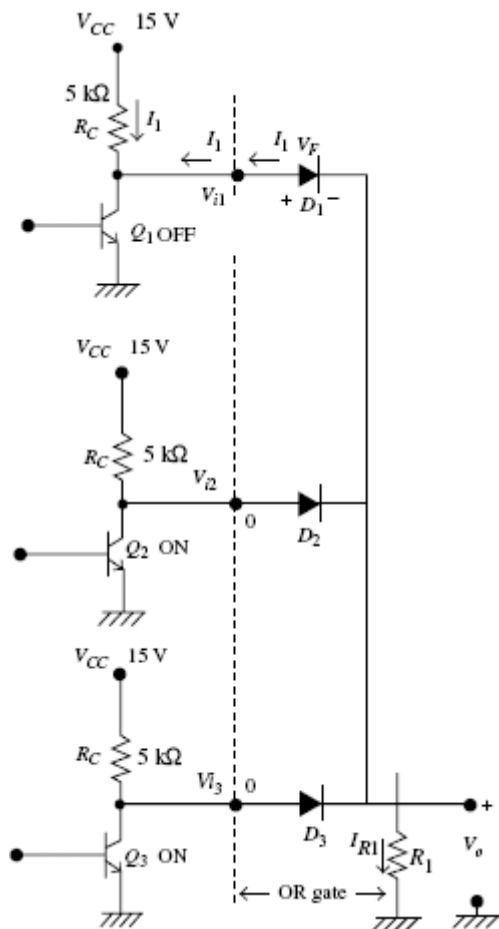
FIGURE 10.8(a) The three-input OR gate

Let the inputs be 1, 0 and 0 for D_1, D_2 and D_3, respectively. This means Q_1 is OFF and Q_2 and Q_3 are ON. Then D_1 is ON and D_2 and D_3 are OFF, as shown in Fig. 10.8(b).

$$V_{CC} = I_1 R_C + V_F + V_o \qquad I_1 R_C = V_{CC} - V_F - V_o$$
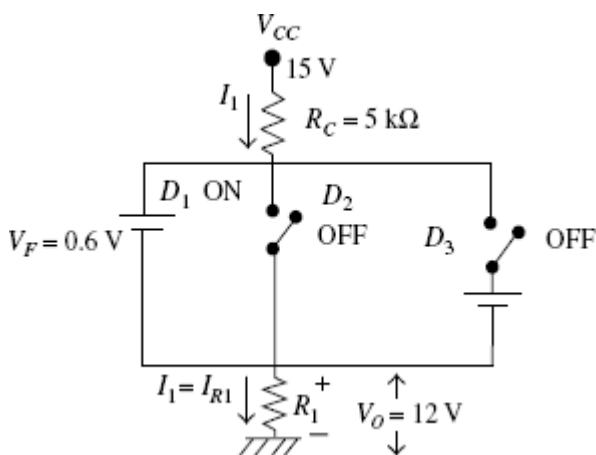
FIGURE 10.8(b) The circuit of Fig. 10.8(a) when Q_1 is OFF Q_2 and Q_3 are ON

V_o for 1 level required to be 12V.

Therefore,

$$I_1 = \frac{15 - 0.6 - 12}{R_C} = \frac{2.4\,\text{V}}{5\,\text{k}\Omega} \qquad I_1 = I_{R1} = 0.48\,\text{mA}$$

Therefore

$$V_o = I_{R1}R_1 \qquad R_1 = \frac{12}{0.48\,\text{mA}} = 25\,\text{k}\Omega$$

10.2.2 Resistor–Transistor Logic Gates

An RTL gate uses the resistances and transistors for its operation. Figure 10.9 shows a resistor–transistor logic (RTL) NOR gate. If both the inputs V_1 and V_2 are 0, Q_1 and Q_2 are OFF and $V_o = V_{CC}$ (1 level). If any or both the inputs are 1, $V_o = V_{CE(sat)}$ (0 level). Hence, this is a NOR gate.
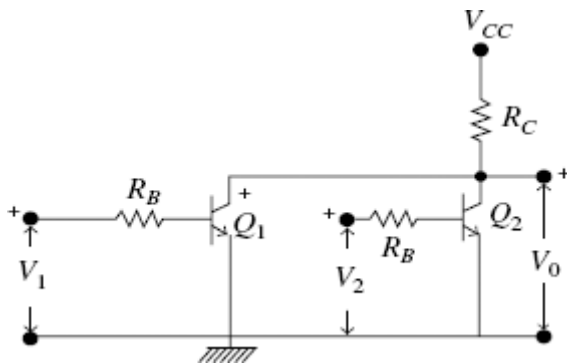
FIGURE 10.9 An RTL NOR Gate

TABLE 10.3 The truth table for a NOR gate

V1	V2	Vo
0	0	1
0	1	0
1	0	0
1	1	0

10.2.3 Diode–Transistor Logic Gates

In the diode–transistor logic family (DTL), diodes and transistors are used as the basic building blocks. In this family, we consider the two basic gates—NAND and NOR.

DTL NAND Gates. A diode AND gate followed by a transistor inverter is a DTL NAND gate, as shown in Fig. 10.11 Here, we assume that the input at 1 is grounded. Diode D_1 conducts. Then the voltage at A, $V_A = V_F$, the diode forward voltage. With this voltage (approximately equal to 0.7 V), diodes D_3 and D_4 will not conduct as they require a minimum voltage of 1.4 V to conduct. Hence, Q is OFF. Thus, if any one of the inputs to the NAND gate is zero, Q is OFF and $V_o = V_{CC}$ (1 level).

If, on the other hand, both the inputs are 1, then diodes D_1 and D_2 are reverse-biased and behave as open circuits. Diodes D_3 and D_4 then conduct and the voltage at the base of Q can drive it into saturation. Therefore, the output $V_o = V_{CE(sat)}$ (0 level). This gate produces a 0 output level when all the inputs are 1 and the 1 level at the output if any of the inputs is 0 (NAND gate). D_3 and D_4 are provided to derive noise immunity. In the NAND gate shown in Fig. 10.11, when D_3 is replaced by a Zener diode (anode and cathode reversed) with a break-down voltage of 3.8 V, this gate gives an even better noise immunity. However, this requires high supply voltages. Such a gate is called a high-threshold logic (HTL) NAND gate. HTL is also sometimes referred to as HNIL (high noise immunity logic).
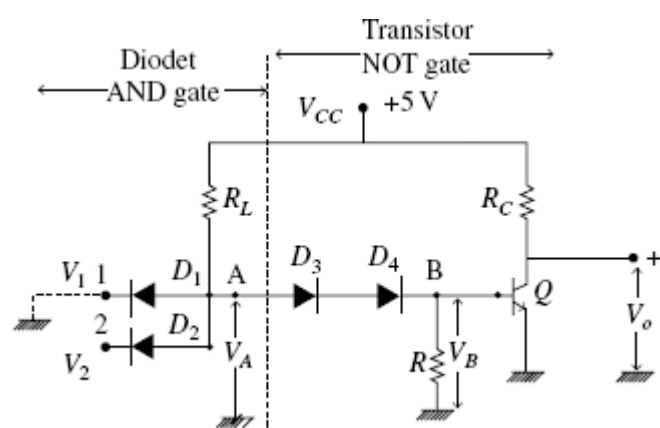
FIGURE 10.11 A DTL NAND gate
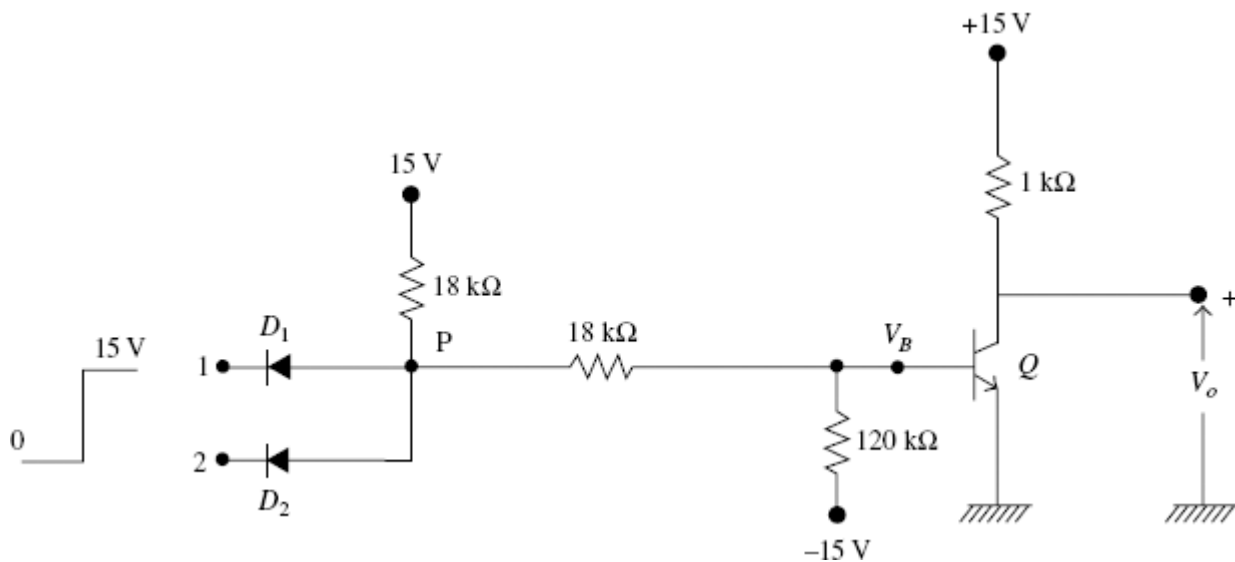
FIGURE 10.12(a) A DTL NAND gate
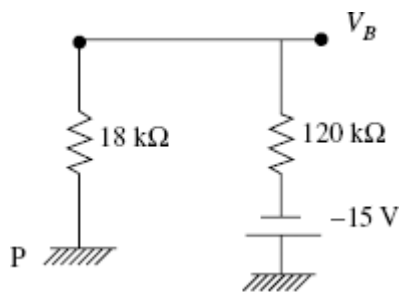
FIGURE 10.12(b) The resultant circuit of Fig. 10.12(a) when the input 1 is 0 and the other is 1
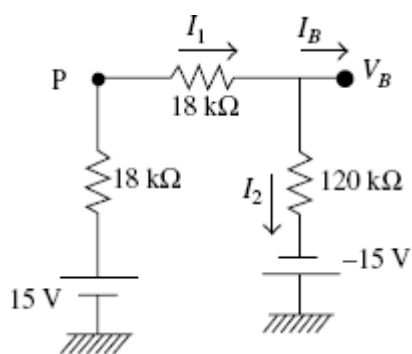
FIGURE 10.12(c) The resultant circuit of Fig. 10.12(a) when both the inputs are 1

To verify that the circuit shown in Fig. 10.12(a) is a NAND gate, let us assume that input1 is 0 V and input 2 is at level 1, i.e., 15 V. Then D_1 conducts as the voltage at the anode of D_2 is V_F ($\approx$ 0 V) and that at the cathode is 15 V, D_2 is OFF and is open circuited. The voltage at P is 0 V, as shown in Fig. 10.12(b).

$$V_B = \frac{-15 \times 18}{18 + 120} = -1.96 \text{ V}$$

TABLE 10.4 The truth table for a NAND gate

280

V1	V2	Vo
0	0	1
0	1	1
1	0	1
1	1	0

As V_B reverse-biases the emitter diode, Q is OFF and $V_o = 15$ V (1 level). If all the inputs are 15 V (1 level), both the diodes are OFF.

$$V_B = \frac{15 \times 120}{120 + 36} + (-15) \times \frac{36}{120 + 36} = 11.54 - 3.46 = 8.08 \text{ V}$$

Hence, Q is in saturation. Consequently, $V_o = 0$ V (0 level). The truth table for this is shown in Table 10.4. Hence, the circuit is a NAND gate.

(ii) Calculating the minimum value of h_{FE} to keep Q in saturation

Consider the equivalent circuit of Fig. 10.12(a). When Q is in saturation, $V_{CE(sat)} = 0$, $V_{BE(sat)} = 0$ when compared to the supply voltages of 15 V, as shown in Fig. 10.12(d).

$$I_1 = I_2 + I_B \quad I_B = I_1 - I_2$$

$$I_B = \frac{15 \text{ V}}{36 \text{ k}\Omega} - \frac{15 \text{ V}}{120 \text{ k}\Omega} = 0.42 - 0.125 = 0.295 \text{ mA}$$

$$I_C = \frac{15 \text{V}}{1 \text{k}\Omega} = 15 \text{ mA}$$
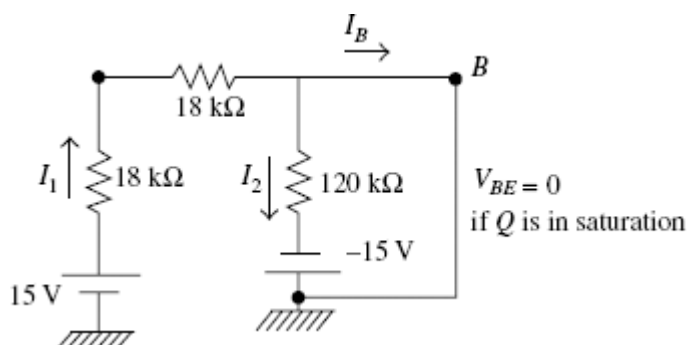
FIGURE 10.12(d) The resultant circuit of <u>Fig. 10.12(a)</u> when Q is in saturation

And

$$h_{FE}(\text{min}) = \frac{I_C}{I_B} = \frac{15}{0.295} = 50$$
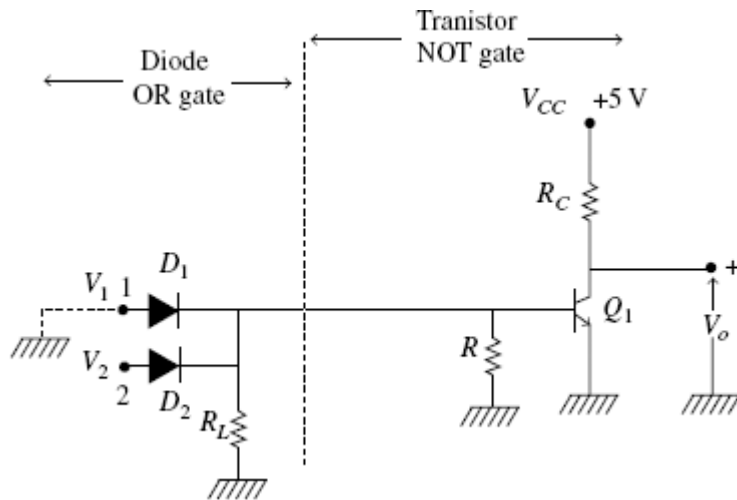
FIGURE 10.13 A DTL NOR gate
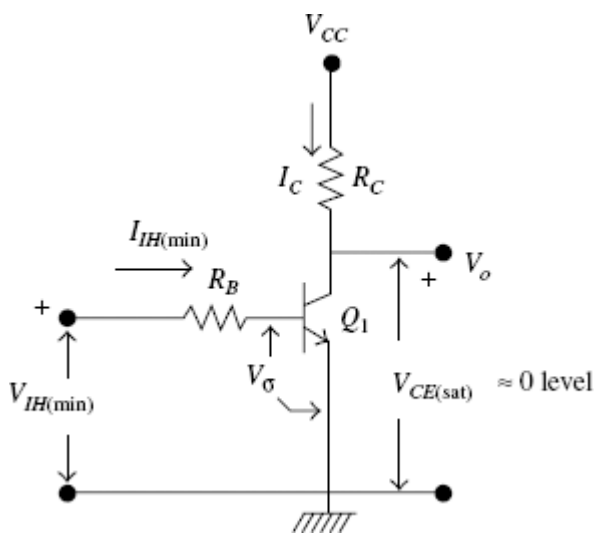
FIGURE 10.14 A transistor inverter with an output low

DTL NOR Gates. A DTL NOR gate comprises a diode OR gate followed by a transistor inverter, as shown in <u>Fig. 10.13</u>. When both the inputs V_1 and V_2 are 0, Q_1 is OFF and $V_o = V_{CC}$(1 level). If any input, say V_1 is 1, D_1 is ON and the voltage at the base of Q_1 is 5 V. Consequently, Q_1 is in saturation and $V_o = V_{CE(sat)}$ (0 lev

In a diode AND gate, the output voltage is high if all the input voltages are high. The output voltage is low if at least one of the input voltage is low.

To realize the basic idea, the diodes are *reverse connected* and *forward biased* by an additional voltage source $+V$ (a power supply) through the pull-up resistor R1. The input voltage sources are connected in opposite direction to the supplying voltage source (traveling along the loop +V - R1 - D - Vin). To invert the output voltage and to get a grounded output, the complementary voltage drop $(+V - V_{R1})$ between the output and ground is taken as an output instead the floating voltage drop V_{R1} across the resistor.

Input logical ones. When all the input voltages are high, they "neutralize" the biasing supply voltage $+V$. The voltage drops across the diodes are zero and these diode switches are open. The output voltage is high (output logical *1*) since no current flows through the resistor and there is no voltage drop across it. The output resistance is R1. Hence, the behavior of the diode switches is reversed - whereas in diode OR logic gates diodes act as *normally open switches*, in diode AND logic gates diodes act as *normally closed switches*.

Input logical zero. If the voltage of some input voltage source is low (input logical *0*), the power supply passes current through the resistor, diode and the input source. The diode is forward biased (the diode switch is closed) and the output voltage drop across the diode is low (output logical *0*). The output resistance is low and is determined by the input source. The rest of diodes connected to high input voltages (input logical *1s*) are backward biased and their input sources are disconnected from the output Node 1.

If two diode AND logic gates are cascaded, they behave as *current-sinking* logic gates: if the first gate produces high output voltage, the second gate does not consume current from the first one; if the first gate produces low output voltage, the second gate injects current into the output of the first one. A diode AND gate uses its own power supply to drive the load through the pull-up resistor.

Properties

Non-restoring logic
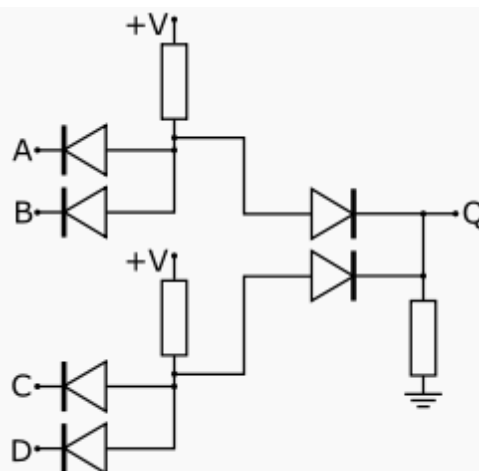
In cascaded AND-OR diode gates, the high voltage level is decreased more than two times.

Digital logic implemented by active elements is characterized by signal restoration. *True* and *false* or *1* and *0* are represented by two specific voltage levels. If the inputs to a digital logic gate is close to their respective levels, the output will be closer or exactly equal to its desired level. Active logic gates may be integrated in large numbers because each gate tends to remove noise at its input. Diode logic gates are implemented by passive elements; so, they have two restoration problems.

Forward voltage drop. The first restoration problem of diode logic is that there is a voltage drop V_F about 0.6 V across the forward-biased diode. This voltage is added to or subtracted from the input of every gate so that it accumulates when identical diode gates are cascaded. In an OR gate, V_F decreases the high voltage level (the logical *1*) while in an AND gate, it increases the low voltage level (the logical *0*). The feasible number of logic stages thus depends on the difference between the high and low voltages.

Source resistance. Another problem of diode logic is the internal resistance of the input voltage sources. Together with the gate resistor, it constitutes a voltage divider that worsens the voltage levels. In an OR gate, the source resistance decreases the high voltage level (the logical *1*) while in an AND gate, it increases the low voltage level (the logical *0*). In the cascaded AND-OR diode gates in the picture on the right, the AND high output voltages are decreased because of the internal voltage drops across the AND pull-up resistances.

Non-inverting logic

Diode logic is non-inverting in both the OR and AND configurations: a diode OR gate is *true non-inverting* ($Y = X$ in the case of one-input OR gate) while a diode AND gate is non-inverting since it is *double inverting* ($Y = $ NOT (NOT (X)) = X in the case of one-input AND gate - see the considerations above). Diode AND gate would be inverting if the voltage drop across the resistor is taken as an output but the load would be not grounded in this case.

Applications

Diode logic gates are used to build diode–transistor logic (DTL) gates as integrated circuits.

The outputs of conventional ICs (with complementary output stages) must never be directly connected together since they act as voltage sources. However, diodes can be used to combine two or more digital (high/low) outputs from an IC such as a counter. This wired logic connection can be a useful way of producing simple logic functions without using additional logic gates.

Monolithic integrated circuit logic families compared

The following logic families would either have been used to build up systems from functional blocks such as flip-flops, counters, and gates, or else would be used as "glue" logic to interconnect very-large scale integration devices such as memory and processors. Not shown are some early obscure logic families from the early 1960s such as DCTL (direct-coupled transistor logic), which did not become widely available.

Propagation delay is the time taken for a two-input NAND gate to produce a result after a change of state at its inputs. Toggle speed represents the fastest speed at which a J-K flip flop could operate. Power per gate is for an individual 2-input NAND gate; usually there would be more than one gate per IC package. Values are very typical and would vary slightly depending on application conditions, manufacturer, temperature, and particular type of logic circuit. Introduction year is when at least some of the devices of the family were available in volume for civilian uses. Some military applications pre-dated civilian use.[5][6]

Family	Description	Propagation delay (ns)	Toggle speed (MHz)	Power per gate_@1 MHz (mW)	Typical supply voltage V (range)	Introduction year	Remarks
RTL	Resistor–transistor logic		4	10	3.3	1963	the first CPU built from integrated circuits (the Apollo Guidance Computer) used RTL.
DTL	Diode–transistor logic			10	5	1962	Introduced by Signetics, Fairchild 930 line became industry standard in 1964
CMOS	AC/ACT	3	125	0.5	3.3 or 5 (2-6 or 4.5-5.5)	1985	ACT has TTL Compatible levels
CMOS	HC/HCT	9	50	0.5	5 (2-6 or 4.5-5.5)	1982	HCT has TTL compatible levels
CMOS	4000B/74C	30	5	1.2	10V (3-18)	1970	Approximately half speed and power at 5 volts
TTL	Original series	10	25	10	5 (4.75-5.25)	1964	Several manufacturers
TTL	L	33	3	1	5 (4.75-5.25)	1964	Low power
TTL	H	6	43	22	5 (4.75-5.25)	1964	High speed
TTL	S	3	100	19	5 (4.75-5.25)	1969	Schottky high speed
TTL	LS	10	40	2	5 (4.75-5.25)	1976	Low power Schottky high speed
TTL	ALS	4	50	1.3	5 (4.5-5.5)	1976	Advanced Low power Schottky
TTL	F	3.5	100	5.4	5 (4.75-5.25)	1979	Fast
TTL	AS	2	105	8	5 (4.5-5.5)	1980	Advanced Schottky
TTL	G	1.5	1125 (1.125 GHz)		1.65 - 3.6	2004	First GHz 7400 series logic
ECL	ECL III	1	500	60	-5.2(-5.19 - -5.21)	1968	Improved ECL
ECL	MECL I	8		31	-5.2	1962	first integrated logic circuit commercially produced
ECL	ECL 10K	2	125	25	-5.2(-5.19 - -5.21)	1971	Motorola
ECL	ECL 100K	0.75	350	40	-4.5(-4.2 - -5.2)	1981	
ECL	ECL 100KH	1	250	25	-5.2(-4.9 - -5.5)	1981	

15. Additional Topics

1. CMOS logic family
2. Bi-CMOS logic family
3. CRO operation and CRO probe

CMOS Logic Family

The CMOS (Complementary Metal Oxide Semiconductor) logic family uses both N-type and P-type MOSFETs (enhancement MOSFETs, to be more precise) to realize different logic functions. The two types of MOSFET are designed to have matching characteristics. That is, they exhibit identical characteristics in switch-OFF and switch-ON conditions. The main advantage of the CMOS logic family over bipolar logic families discussed so far lies in its extremely low power dissipation, which is near-zero in static conditions. In fact, CMOS devices draw power only when they are switching. This allows integration of a much larger number of CMOS gates on a chip than would have been possible with bipolar or NMOS (to be discussed later) technology. CMOS technology today is the dominant semiconductor technology used for making microprocessors, memory devices and application-specific integrated circuits (ASICs). The CMOS logic family, like TTL, has a large number of subfamilies. The prominent members of CMOS logic were listed in an earlier part of the chapter. The basic difference between different CMOS logic subfamilies such as 4000A, 4000B, 4000UB, 74C, 74HC, 74HCT, 74AC and 74ACT is in the fabrication process used and not in the design of the circuits employed to implement the intended logic function. We will firstly look at the circuit implementation of various logic functions in CMOS and then follow this up with a brief description of different subfamilies of CMOS logic.

Circuit Implementation of Logic Functions

In the following paragraphs, we will briefly describe the internal schematics of basic logic functions when implemented in CMOS logic. These include inverter, NAND, NOR, AND, OR, EX-OR, EX-NOR and AND-OR-INVERT functions.

CMOS Inverter

The inverter is the most fundamental building block of CMOS logic. It consists of a pair of N-channel and P-channel MOSFETs connected in cascade configuration as shown in Fig. 5.34. The circuit functions as follows. When the input is in the HIGH state (logic '1'), P-channel MOSFET Q_1 is in the cut-off state while the N-channel MOSFET Q_2 is conducting. The conducting MOSFET provides a path from ground to output and the output is LOW (logic '0'). When the input is in the LOW state (logic '0'), Q_1 is in conduction while Q_2 is in cut-off. The conducting P-channel device provides a path for V_{DD} to appear at the output, so that the output is in HIGH or

logic '1' state. A floating input could lead to conduction of both MOSFETs and a short-circuit condition. It should therefore be avoided. It is also evident from Fig. 5.34 that there is no conduction path between V_{DD} and ground in either of the input conditions, that is, when input is in logic '1' and '0' states. That is why there is practically zero power dissipation in static conditions. There is only dynamic power dissipation, which occurs during switching operations as the MOSFET gate capacitance is charged and discharged. The power dissipated is directly proportional to the switching frequency.
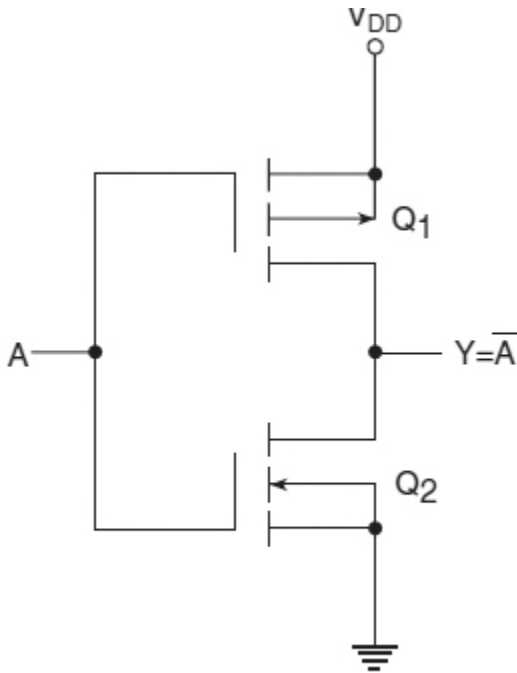
Fig.1 CMOS inverter.

NAND Gate

Below shows the basic circuit implementation of a two-input NAND. As shown in the figure, two P-channel MOSFETs (Q_1 and Q_2) are connected in parallel between V_{DD} and the output terminal, and two N-channel MOSFETs (Q_3 and Q_4) are connected in series between ground and output terminal. The circuit operates as follows. For the output to be in a logic '0' state, it is essential that both the series-connected N-channel devices conduct and both the parallel-connected P-channel devices remain in the cut-off state. This is possible only when both the inputs are in a logic '1' state. This verifies one of the entries of the NAND gate truth table. When both the inputs are in a logic '0' state, both the N-channel devices are nonconducting and both the P-channel devices are conducting, which produces a logic '1' at the output. This verifies another entry of the NAND truth table. For the remaining two input combinations, either of the two N-channel devices will be nonconducting and either of the two parallel-connected P-channel devices will be conducting. We have either Q_3 OFF and Q_2 ON or Q_4 OFF and Q_1 ON. The output in both cases is a logic '1', which verifies the remaining entries of the truth table.
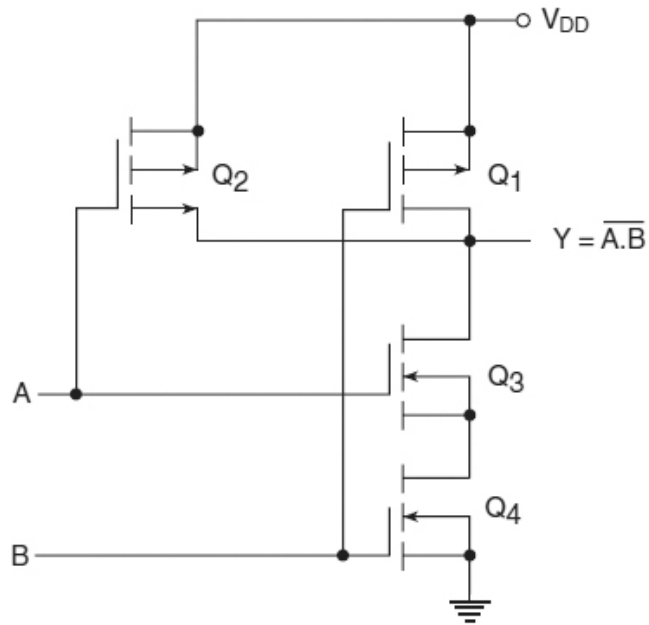
Fig.2 CMOS 2-i/p NAND gate
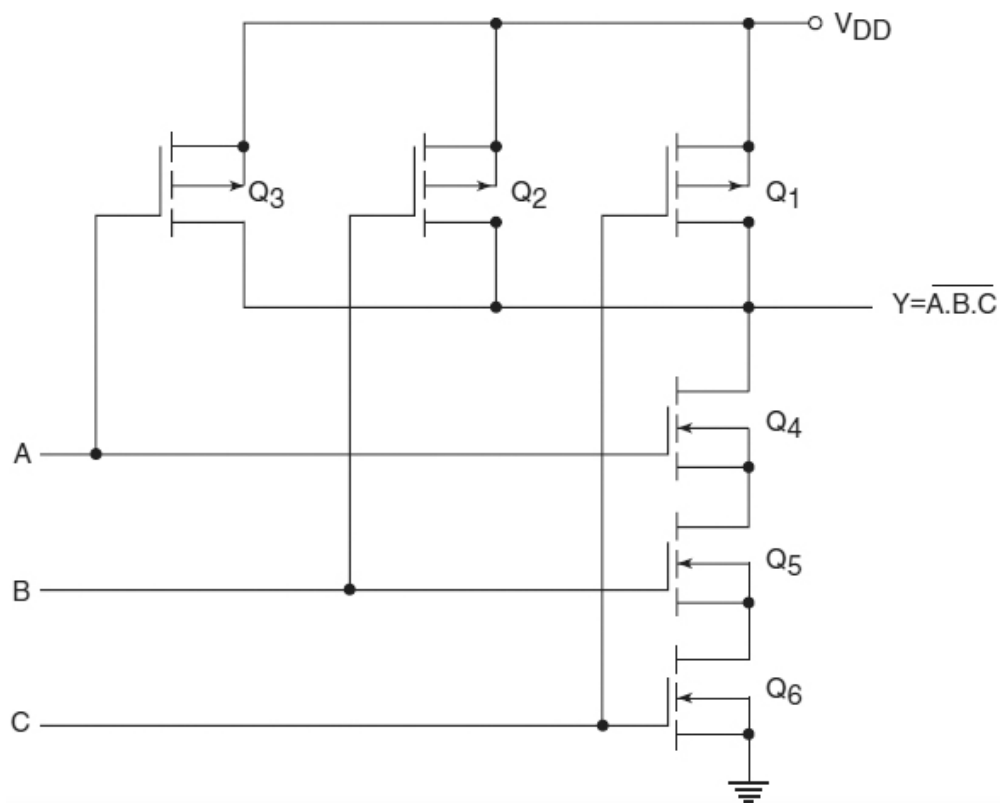
Fig.3 CMOS 3-i/p NAND gate

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From the circuit schematic of <u>Fig.</u> 2 we can visualize that under no possible input combination of logic states is there a direct conduction path between V_{DD} and ground. This further confirms that there is near-zero power dissipation in CMOS gates under static conditions. Figure 3 shows how the circuit of Fig. 2 can be extended to build a three-input NAND gate. Operation of this circuit can be explained on similar lines. It may be mentioned here that series connection of MOSFETs adds to the propagation delay, which is greater in the case of P-channel devices than it is in the case of N-channel devices. As a result, the concept of extending the number of inputs as shown in Fig. 3 is usually limited to four inputs in the case of NAND and to three inputs in the case of NOR. The number is one less in the case of NOR because it uses series-connected P-channel devices. NAND and NOR gates with larger inputs are realized as a combination of simpler gates.

NOR Gate

Figure 4 shows the basic circuit implementation of a two-input NOR. As shown in the figure, two P-channel MOSFETs (Q_1 and Q_2) are connected in series between V_{DD} and the output terminal, and two N-channel MOSFETs (Q_3 and Q_4) are connected in parallel between ground and output terminal. The circuit operates as follows. For the output to be in a logic '1' state, it is essential that both the series-connected P-channel devices conduct and both the parallel-connected N-channel devices remain in the cut-off state. This is possible only when both the inputs are in a logic '0' state. This verifies one of the entries of the NOR gate truth table. When both the inputs are in a logic '1' state, both the N-channel devices are conducting and both the P-channel devices are nonconducting, which produces a logic '0' at the output. This verifies another entry of the NOR truth table. For the remaining two input combinations, either of the two parallel N-channel devices will be conducting and either of the two series-connected P-channel devices will be nonconducting. We have either Q_1 OFF and Q_3 ON or Q_2 OFF and Q_4 ON. The output in both cases is logic '0', which verifies the remaining entries of the truth table.
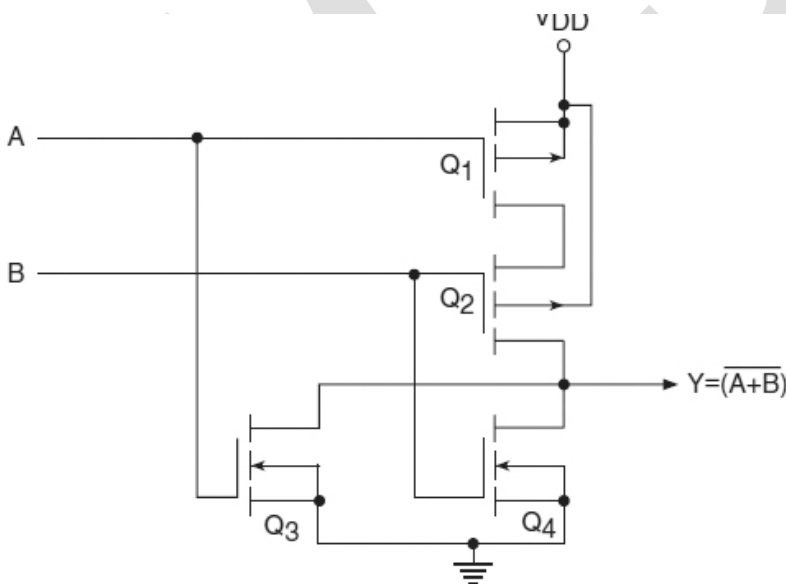
Fig.4 CMOS 2-i/p NOR gate

EXCLUSIVE-OR Gate

An EXCLUSIVE-OR gate is implemented using the logic diagram of Fig. 5. As is evident from the figure, the output of this logic arrangement can be expressed by

Exclusive-OR (XOR)

$$- \; a \oplus b = \overline{a} \cdot b + a \cdot \overline{b}$$
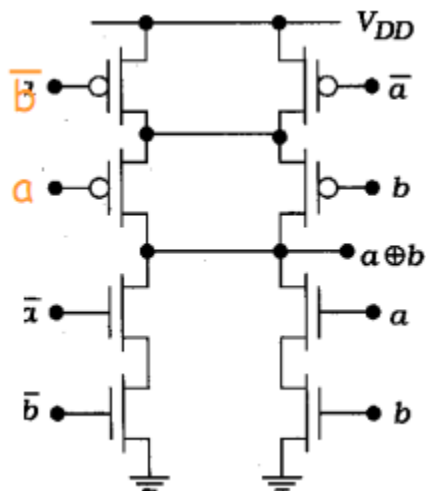
Fig.5 XOR gate

An EXCLUSIVE-NOR gate is implemented using the logic diagram of Fig. 6. As is evident from the figure, the output of this logic arrangement can be expressed by

Exclusive-NOR

$$- \; \overline{a \oplus b} = a \cdot b + \overline{a} \cdot \overline{b}$$
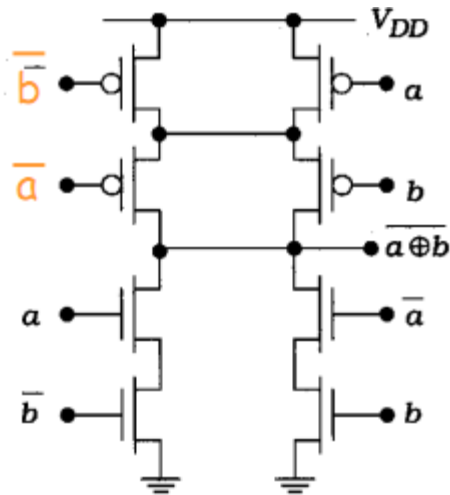
Fig.6 XOR gate

Bi-CMOS logic family

The BiCMOS logic family integrates bipolar and CMOS devices on a single chip with the objective of deriving the advantages individually present in bipolar and CMOS logic families. While bipolar logic families such as TTL and ECL have the advantages of faster switching speed and larger output drive current capability, CMOS logic scores over bipolar counterparts when it comes to lower power dissipation, higher noise margin and larger packing density. BiCMOS logic attempts to get the best of both worlds. Two major categories of BiCMOS logic devices have emerged over the years since its introduction in 1985. In one type of device, moderate-speed bipolar circuits are combined with high-performance CMOS circuits. Here, CMOS circuitry continues to provide low power dissipation and larger packing density. Selective use of bipolar circuits gives improved performance. In the other category, the bipolar component is optimized to produce high-performance circuitry. In the following paragraphs, we will briefly describe the basic BiCMOS inverter and NAND circuits.

5.6.1 BiCMOS Inverter

Figure 5.55 shows the internal schematic of a basic BiCMOS inverter. When the input is LOW, N-channel MOSFETs Q_2 and Q_3 are OFF. P-channel MOSFET Q_1 and N-channel MOSFET Q_4 are ON. This leads transistors Q_5 and Q_6 to be in the ON and OFF states respectively. Transistor Q_6 is OFF because it does not get the required forward-biased base-emitter voltage owing to a conducting Q_4. Conducting Q_5 drives the output to a HIGH state, sourcing a large drive current to the load. The HIGH-state output voltage is given by the equation

$$V_{OH} = V_{DD} - V_{BE}(Q_5)$$

When the input is driven to a HIGH state, Q_2 and Q_3 turn ON. Initially, Q_4 is also ON and the output discharges through Q_3 and Q_4. When Q_4 turns OFF owing to its gate-source voltage falling below the required threshold voltage, the output continues to discharge until the output voltage equals the forward-biased base-emitter voltage drop of Q_6 in the active region. The LOW-state output voltage is given by the equation

$$V_{\mathrm{OL}} = V_{\mathrm{BE}}(Q_6 \text{ in active mode}) = 0.7V$$

BiCMOS NAND

Figure 7 shows the internal schematic of a two-input NAND in BiCMOS logic. The operation of this circuit can be explained on similar lines to the case of an inverter. Note that MOSFETs Q_1– Q_4 constitute a two-input NAND in CMOS.. The HIGH-state and LOW-state output voltage levels of this circuit are given by the equations
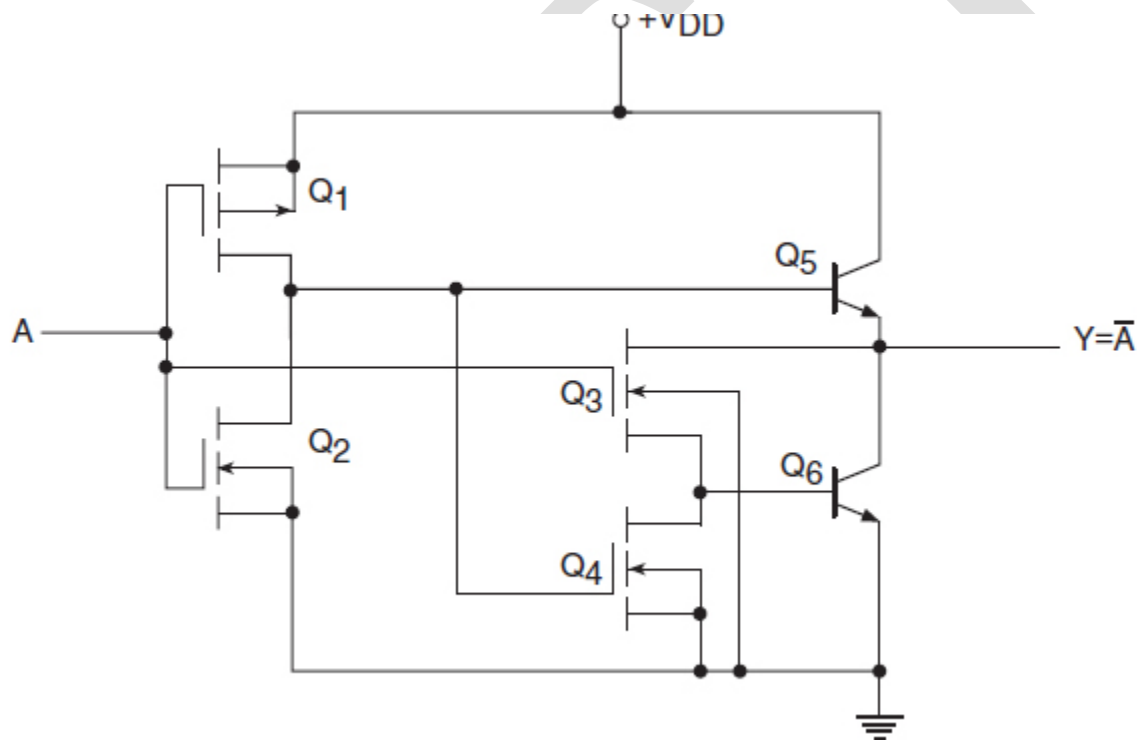
Figure 7 BiCMOS inverter.
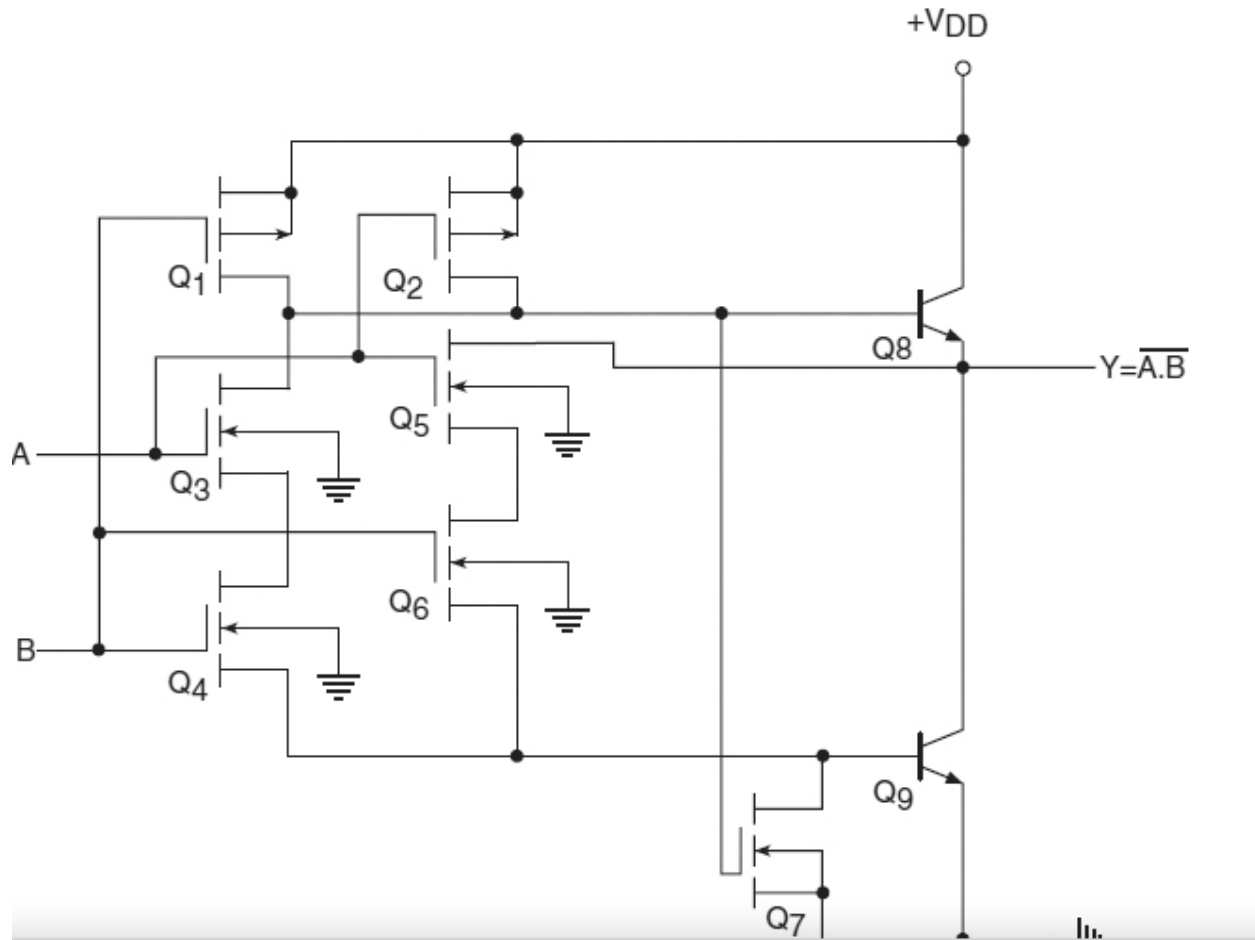
Figure 8 BiCMOS NAND

$$V_{OH} = (V_{DD} - 0.7)$$

$$V_{OL} = 0.7$$

CRO

Oscilloscopes are also used very widely in electronic measurements and instrumentation systems. Unlike other measuring instruments, the signal being measured can be visually seen on the screen. The characteristics of the signals, like amplitude, frequency, phase, time period, duty cycle, etc. can be measured using oscilloscopes. The amplitude of the signals can vary from μV to even a few hundred volts. The frequency can range from very low (even DC) to MHzs.

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Because of the phosphorescence effect, the electrical signal is converted to a visible form and the shape of the signal can be seen.

In this chapter, the constructional blocks of CRO, various controls associated with CRO instruments, the principle of working, triggered sweep and dual beam CRO, and measurement of amplitude and frequency using CRO are explained. The student is expected to understand all these aspects connected with CRO.

The Cathode Ray Oscilloscope (CRO) is a very useful, general-purpose electronic instrument for testing and developing electronic circuits, systems, and instruments. Using a CRO, the shape, amplitude, and frequency of AC signals can be measured. CRO is also useful in determining the amplitude of DC signals. The versatility of CRO lies in the fact that time variation of the given electronic signal or electrical input can be studied. A part of the input signal can be expanded in the time scale, and the distortion, rise time, fall time, or any other characteristic feature of the signal can be studied. The electron beam generated in the CRO is deflected by the given electrical signal and when the deflected electron beam strikes the screen of the CRO, because of the phosphorescence effect, a visible trace is produced exactly in the same shape as the given electrical signal. Similar to the conventional graph that is plotted, the deflection of the electron beam in the X-direction on the screen is a measure of time, and the deflection in the conventional Y-direction is a measure of amplitude of the signal. The other types of recording devices such as an $X–Y$ recorder and a strip-chart recorder are mechanical devices that are slow in response. CRO is capable of displaying events that take place over periods of microseconds and nanoseconds. Though a hard copy of the waveform seen on the screen is not obtained from CRO directly, the waveform can be photographed or stored as in the case of storage CRO. By incorporating microprocessor-based computing circuitry, CROs can directly display the characteristics of the signal on the screen such as amplitude, frequency, phase, rise time, and fall time on the screen itself along with the signal, without measurement and computation by the operator.

BLOCK DIAGRAM OF A CRO

The heart of a CRO is the cathode ray tube (CRT). Here, the electron beam is generated, accelerated, and deflected in accordance with the input signal, and a visible trace is produced on the phosphor screen. For the illumination on the screen to be bright, the velocity of the electron beam impinging on the screen and the kinetic energy (KE) must be high. Therefore, the beam must be accelerated by a high potential. Hence, a power supply circuit to generate the required high voltage also forms another part of the CRO. If the input signal amplitude is very small, it needs to be amplified. Hence, amplifier circuits also form a part of the system. In order to get a true time variation of the input signal, the electron beam must also be deflected along the X-axis linearly. Hence, a saw-tooth waveform or time base generator is to be incorporated. In addition, there will be delay lines, trigger circuits, and synchronisation circuits also in a CRO in addition to the all-important CRT. The block schematic of a CRO is shown

Vertical amplifier: This is also called a *Y*-amplifier. The electron beam deflection in the *Y*-direction or the vertical direction is proportional to the signal amplitude given to the *Y*-input or vertical plates. Hence, this is called a *Y*-amplifier.

The gain can be varied externally with the help of amplitude control. The bandwidth of this amplifier puts a limit to the maximum frequency of the input signal that can be measured using the CRO. If the magnitude of the external signal is large, it can also be attenuated in the potential divider attenuator section.
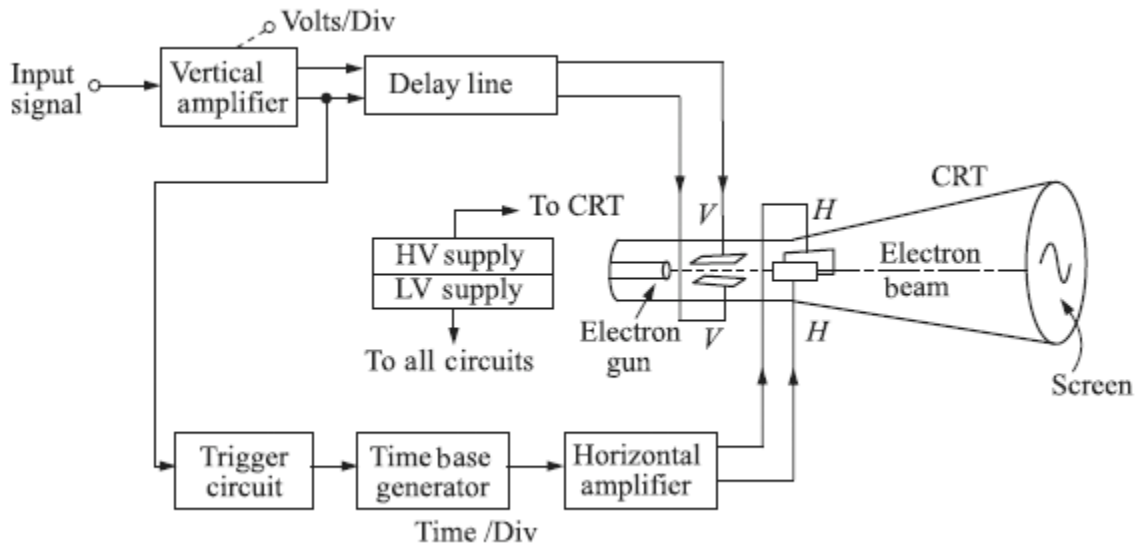
Fig.9 Block diagram of CRO

Delay line: The electron beam is deflected in the *X*-direction by a saw-tooth waveform called the *time base signal*. When the set magnitude of the saw-tooth waveform is reached, it is to be reset and started again in order to get a true time variation of the given signal. The attenuators, amplifiers, pulse shapers, and circuit wiring introduce a certain amount of time delay. To allow the operator to observe the leading edge of the signal waveform, the signal drive for the vertical CRT plates must be delayed by at least the same amount. This is achieved by the vertical delay lines.

HV and LV supplies: To accelerate, deflect, and sweep the electron beam, a large voltage in kilovolts is required. This is generated by the high-voltage power supply circuits. *Vcc* and other low voltages required are generated in the low-voltage power supply circuits.

CRT: A CRT is the heart of a CRO. Here the electron beam is generated, accelerated, deflected, post-accelerated, and made to strike the fluorescent screen to give the visual display of the electrical input signal given to the vertical or the *Y*-plates.

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Trigger circuit: To get a true representation of the input signal, the time base signal or the *X*-input and the *Y*-signal must be initiated at the same time. The time base signal must be initiated by the vertical signal itself for proper triggering. This is achieved by the trigger circuit.

Time base generator: This is a saw-tooth waveform generator circuit used to deflect the electron beam linearly in *X*-direction. Usually, a constant current, Miller sweep circuit is employed to generate the saw-tooth waveform.

Horizontal amplifier: The purpose of this circuit is to amplify an externally applied signal to the horizontal or *X*-plates. This also helps in adjusting the magnitude of the internal saw-tooth waveform being generated. If the internal time base waveform is not being used, an electron beam can be deflected horizontally by means of an external signal, which is applied to this circuit. This externally applied *X*-signal can be amplified by adjusting the gain.

16. University Question papers of previous years

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

R13

B.Tech II Year II Semester Examinations, May - 2015

PULSE AND DIGITAL CIRCUITS

(Common to ECE, BME)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

Part- A

(25 Marks)

1.a) Define rise time. [2M]
  b) Draw and briefly explain the RC differentiator circuit. [3M]
  c) What is meant by clipping in wave shaping? [2M]
  d) Explain Clipping at two independent levels with circuit. [3M]
  e) Compare unidirectional and bi-directional Sampling Gates. [2M]
  f) Draw the Piecewise Linear Diode Characteristics. [3M]
  g) Write a basic principle of time base generator. [2M]
  h) Write the Methods of Generating Time Base Waveform. [3M]
  i) Define positive and negative logic systems. [2M]
  j) List out the applications of sweep circuits. [3M]

Part-B

(50 Marks)

2. Draw the output of the low pass RC circuit for different time constant to
   a) Pulse input.
   b) Step voltage input. [5+5]

OR

3.a) Prove that for any periodic input waveform the average level of the steady state output signal from RC high pass circuit is always zero.
  b) Draw and explain the response of RLC circuit for step input. [5+5]

4. Classify different types of clipper circuits. Draw their circuits and explain their operation and also transfer characteristics. [10]

OR

5.a) State and prove clamping circuit theorem.
  b) Explain negative peak clipper with and without reference voltage. [5+5]

6.a) Explain the operation of linear bidirectional sampling gate using transistors.
  b) Explain in detail the junction diode switching times. [5+5]

OR

7.a) Explain about basic operation principles of sampling gates.
  b) Write the advantages and disadvantages of unidirectional diode gate. [5+5]

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8. Explain with neat diagram the following methods of linearizing a voltage sweep.
    a) Miller Sweep
    b) Bootstrap weep.
    Compare their merits and limitations.   [5+5]

OR

9. Draw and explain the working principle of bistable multivibrator circuit and also explain the merits and limitations of it.   [10]

10.a) Explain about DTL NAND gate.
   b) Distinguish between voltage and current sweep circuit.   [4+6]

OR

11. Draw the circuit of a linear current sweep and explain its operation with wave forms. Explain the necessity of generating trapezoidal wave form.   [10]

--ooOoo--

Code No: R05210203

Set No. 1

II B.Tech I Semester Supplimentary Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering, Electronics &
Communication Engineering, Electronics & Instrumentation Engineering
and Electronics & Telematics)

Time: 3 hours   Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Derive the expression for rise time of integrating circuit and prove that it is proportional to time constant and inversely proportional to upper 3 dB frequency.

   (b) Explain the operation of RC low pass circuit for exponential input is applied.
   [8+8]

2. (a) T=1000 μ sec
   V= 10 V
   Duty cycle = 0.2

   i. Sketch waveform with voltage levels at steady state figure 2(a)iii
   ii. Forward and reverse direction tilt
   iii. A_f / A_r
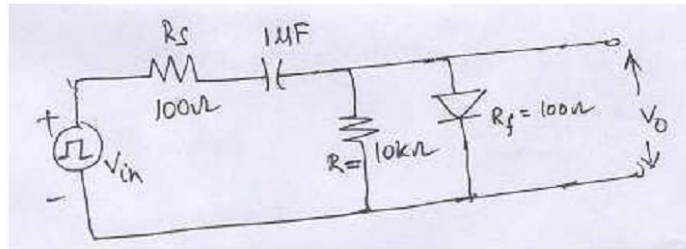
Figure 2(a)iii

   (b) Write a short note on non- linear wave shaping.   [12+4]

3. (a) Explain the behaviour of a BJT as a switch in electronic circuits. Give an example.

   (b) Write a short note on the switching times of transistor.   [8+8]

4. What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a monostable multi, and derive an expression for pulse width. Draw the wave forms at collector and Bases of both transistors. [16]

5. (a) With the help of a neat circuit diagram and waveforms explain the working of a transistor Miller time base generator.

(b) Find the component values of a bootstrap sweep generator, given Vcc=18V, Ic(sat) = 2mA and hfe(min)=30.   [8+8]

6. (a) Explain the factors which influence the stability of a relaxation divider with the help of a neat waveforms.

(b) A UJT sweep operates with Vv = 3V, Vp=16V and η=0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronism with the sync signal?   [8+8]

7. (a) What is sampling gate? Explain how it differ from Logic gates?

(b) What is pedestal? How it effects the output of a sampling gates?

(c) What are the drawbacks of two diode sampling gate?   [6+6+4]

8. (a) With the help of circuit diagram explain the purpose of clamping diode in a positive diode AND gate.

(b) Explain the effect of and diode capacitance on the output pulse of diode AND gate.   [8+8]

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Code No: R05210203

Set No. 2

II B.Tech I Semester Supplimentary Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering, Electronics &
Communication Engineering, Electronics & Instrumentation Engineering
and Electronics & Telematics)

Time: 3 hours   Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) A square wave whose peak-to-peak value is 1V, extends $\pm 0.5V$ with reference
   to ground. The half period is 0.1 sec This voltage impressed upon an R.C.
   differentiating circuit whose time constant is 0.2 sec. Determine the maximum
   and minimum values of the output voltage in the steady state.

   (b) Draw the response of high pass circuit for square wave and derive the expres-
   sion for percentage tilt.   [8+8]

2. (a) For the circuit shown in figure 2a V_S is a sinusoidal voltage of peak 75 volts.
   Assuming ideal diodes. Sketch one cycle of output voltage. Determine the
   maximum diode currents.
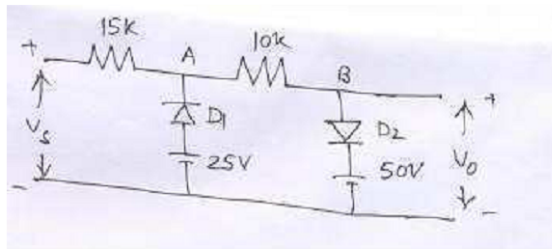
Figure 2a

   (b) What are the uses of clipper circuits.   [12+4]

3. (a) Explain the terms pertaining to transistor switching characteristics.

      i. Rise time.
      ii. Delay time.
      iii. Turn-on time.
      iv. Storage time.
      v. Fall time.
      vi. Turn-off time.

   (b) Give the expression for risetime and falltime in terms of transistor parameters
   and operating currents.   [6+10]

4. Draw and explain about the response of Schmitt circuit for the following.

   (a) for loop gain ≤ 1

(b) loop gain >1. [16]

5. (a) How are linearly varying current waveforms generated?

(b) In the boot strap circuit shown in figure5 V_{cc} = 25 V, V_{EE} = -15 V, R = 10 K ohms, R_B = 150 K ohms, C = 0.05 μF. The gating waveform has a duration of 300 μs. The transistor parameters are h_{ie} = 1.1Kohms, h_{re} = 2.5 x 10^{-4} K ohmsh_{fe} =50 h_{oe} = 1/40K ohms.

   i. Draw the waveform of IC1 and Vo , labeling all current and voltage levels,
   ii. What is the slope error of the sweep?
   iii. What is the sweep speed and the maximum value of the sweep voltage?
   iv. What is the retrace time Tr for C to discharge completely?
   v. Calculate the recovery time T1 for C1 to recharge completely. [6+10]
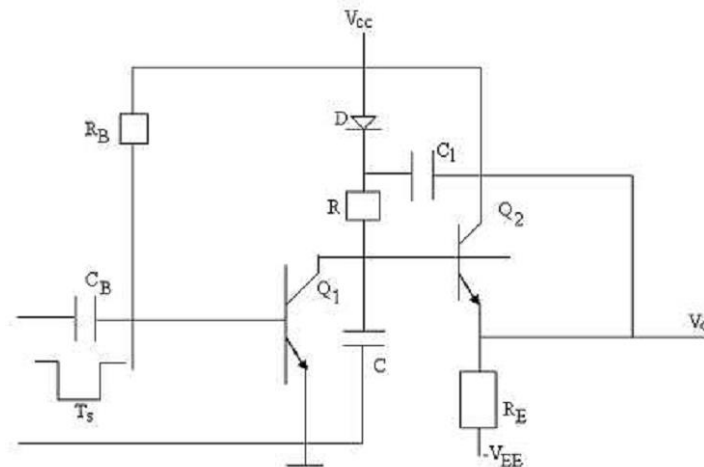
Figure 5

6. (a) What do you mean by synchronization ?

(b) What is the condition to be met for pulse synchronization?

(c) Compare sine wave synchronization with pulse synchronization? [4+6+6]

7. (a) Explain the balance conditions in a bi-directional diode gate.

(b) Explain the utility of sampling gate in a sampling scope. [8+8]

8. (a) What are the basic logic gates which perform almost all the operations in Digital communication systems.

(b) Give some applications of logic gates.

(c) Define a positive and negative logic systems.

(d) Draw a pulse train representing a 11010111 in a synchronous positive logic digital system. [4+4+4+4]

⋆ ⋆ ⋆ ⋆ ⋆

II B.Tech I Semester Supplimentary Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering, Electronics &
Communication Engineering, Electronics & Instrumentation Engineering
and Electronics & Telematics)

Time: 3 hours   Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. Wtite short note on the following:

   (a) Attenuators

   (b) RC Double differentiator.

   (c) RLC ringing circuit.   [5+6+5]

2. (a) A symmetrical 10 kHz square wave whose peak -to-peak excursion are $\pm 10V$
   with respect to ground is impressed upon the diode clamping circuit shown in
   figure 2a. The Diodes has $R_f = 100\ \Omega$, $R_r = \alpha$ and $V_\gamma = 0$. Sketch the steady
   state output waveform Indicating clearly the voltage levels.
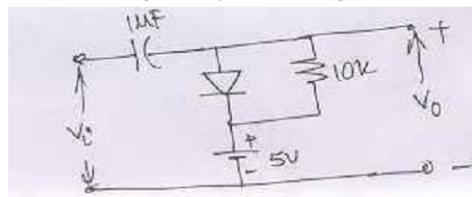
   Figure 2a

   (b) Explain positive peak voltage limiters above and below reference level. [8+8]

3. (a) Sketch neatly the waveforms of current & voltages for a transistor switch with
   capacitance loading circuit.

   (b) What are catching diodes?   [12+4]

4. (a) Draw the circuit of a bistable multivibrator with symmetrical collector trig-
   gering.

   (b) Design a monostable circuit that produces a pulse width of 10msec. (Assume
   the required date)   [8+8]

5. (a) With the help of a neat circuit diagram and waveforms explain the working
   of a transistor Miller time base generator.

   (b) Find the component values of a bootstrap sweep generator, given Vcc=18V,
   Ic(sat) = 2mA and hfe(min)=30.   [8+8]

6. (a) What is relaxation oscillator? Explain how it is used for synchronization?
   Name some negative resistance devices used as relaxation oscillators.

(b) Explain how Astable multivibrator is used for frequency division?   [8+8]

7. (a) Draw and explain a sampling diode whose response is not sensitive to the upper level of the control voltage.

(b) Draw and explain a unidirectional gate which delivers an output only at a coincidence of a number of control voltages.   [8+8]

8. (a) What are the basic logic gates which perform almost all the operations in Digital communication systems.

(b) Give some applications of logic gates.

(c) Define a positive and negative logic systems.

(d) Draw a pulse train representing a 11010111 in a synchronous positive logic digital system.   [4+4+4+4]

⋆ ⋆ ⋆ ⋆ ⋆

II B.Tech I Semester Supplimentary Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering, Electronics &
Communication Engineering, Electronics & Instrumentation Engineering
and Electronics & Telematics)

Time: 3 hours
Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Prove that an RC circuit behaves as a reasonably good integrator if RC > 15T,
   Where T is the period of an input '$E_m \sin \omega t$'.

   (b) What is the ratio of the rise time of the three sections in cascade to the rise
   time of Single section of low pass RC circuit. [8+8]

2. (a) For the circuit shown in figure 2a an input voltage V_i linearly from 0 to 150V
   is applied. Sketch the output waveform V_0 to the same time scale. Assume
   ideal diodes.
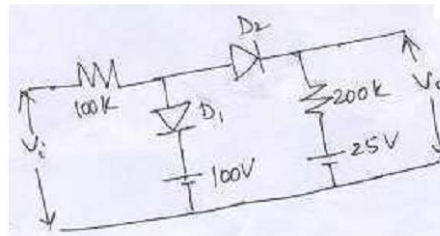
Figure 2a

   (b) What in meant by a d.c restoration circuit and explain? [12+4]

3. Write Short notes on:

   (a) Diode switching times

   (b) Switching characteristics of transistors

   (c) FET as a switch. [4+8+4]

4. In the monostable circuit of the given figure 4 the resistor R is connected to
   an auxiliary supply V_1 instead of V_{YY}. If A2 is in saturation or clamp and
   if A1 is OFF in the stable state, verify that the gate time T is given by Eq.
   $T = \tau \ln(V_{YY} + I_1 R_Y - V\sigma)/(V_{YY} - V\gamma)$ with V_{YY} replaced by V_1. [16]
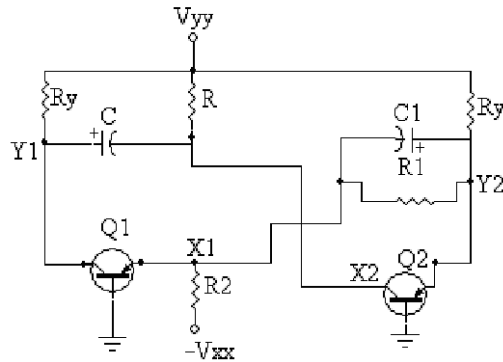
Figure 4

5. (a) Compare the principle of operation of Miller sweep circuit and Bootstrap sweep circuit

   (b) Explain how linearity is obtained by adjusting the driving waveform of current sweep circuit. [8+8]

6. (a) Draw the circuit diagram of an astable multivibrator to obtain frequency division by 5. Explain its working with waveforms.

   (b) What is phase jitter? Discuss the significance of it in a frequency divider. [8+8]

7. (a) What is sampling gate? Explain how it differ from Logic gates?

   (b) What is pedestal? How it effects the output of a sampling gates?

   (c) What are the drawbacks of two diode sampling gate? [6+6+4]

8. (a) What are the basic logic gates which perform almost all the operations in Digital communication systems.

   (b) Give some applications of logic gates.

   (c) Define a positive and negative logic systems.

   (d) Draw a pulse train representing a 11010111 in a synchronous positive logic digital system. [4+4+4+4]

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Set No. 1

II B.Tech I Semester Regular Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering and Electronics &
Instrumentation Engineering)
Time: 3 hours
Max Marks: 80
Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain the response of RC low pass circuit for exponestial input signal
   (b) Derive the expression for percentage till for a square wave output of Rc high
   pass circuit. [8+8]

2. (a) Design a diode clamper to restore a d.c level of +3 Volts to an input sinusoidal
   signal of peak value 10Volts. Assume drop across diode is 0.6 volts as shown
   in the figure 2a.
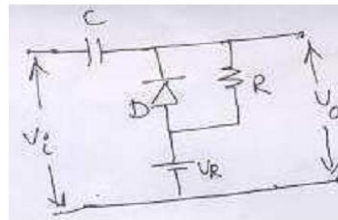
Figure 2a

   (b) Compare series diode clipper and shunt diode clipper. [8+8]

3. (a) Explain the phenomenon of latching in a transistor
   (b) Define the following for a transistor switch
       i. Rise time
       ii. Fall time
       iii. Storage time
       iv. Delay time. [8+8]

4. (a) Explain different triggering methods of binary circuits.
   (b) A collector coupled Fixed bias binary uses NPN transistors with $h_{FE} = 100$.
   The circuit parameters are $V_{CC} = 12v$, V_{BB} = -3v, $R_C = 1k\ \Omega$, $R_1 = 5k\ \Omega$,
   and $R_2 = 10\ k\ \Omega$. Verify that when one transistor is cut-off the other is in
   saturation. Find the stable state currents and voltages for the circuit. Assume
   for transistors $V_{CE(sat)} = 0.3V$ and $V_{BE(sat)} = 0.7V$. [8+8]

5. (a) In a current sweep circuit, explain how linearity correction is made through
   adjustment of driving waveform.
   (b) Write the basic mechanism of transistor television sweep circuit. [16]

6. (a) What is the condition to be met for pulse synchronization?

Set No. 1

(b) Describe synchronization with 2:1 frequency division with neat waveforms.

(c) Define the terms phase delay and phase jitter.   [4+8+4]

7. (a) What is a sampling gate.

(b) Illustrate the principle of sampling gates with series and parallel switches and compare them.

(c) Draw the circuit diagram of unidirectional diode gate and explain its operation.
   [16]

8. (a) Draw the circuit diagram of diode - resistor logic AND gate and explain its operation.

(b) Design a transistor inverter circuit (NOT gate) with the following specifications. $V_{CC} = V_{BB} = 10V$, $i_{csat} = 10mA$; $h_{femin} = 30$; the input is varying between 0 and 10V. Assume typical junction voltages of npn silicon transistor.
   [16]

$\star\star\star\star\star$

II B.Tech I Semester Regular Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering and Electronics &
Instrumentation Engineering)
Time: 3 hours   Max Marks: 80
Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) A symmetrical square wave whose peak-to-peak amptitude id 2V and whose average value is zero as applied to on Rc integrating circuit. The time constant is equals to half -period of th esquare wave find the peak to peak value of the output amplitude

   (b) Describe the relationship between rise time and RCtime constant of a low pass RC circuit.   [8+8]

2. (a) Determine V_o for the network shown in fugure 2a for the given waveform .Assume ideal diodes.
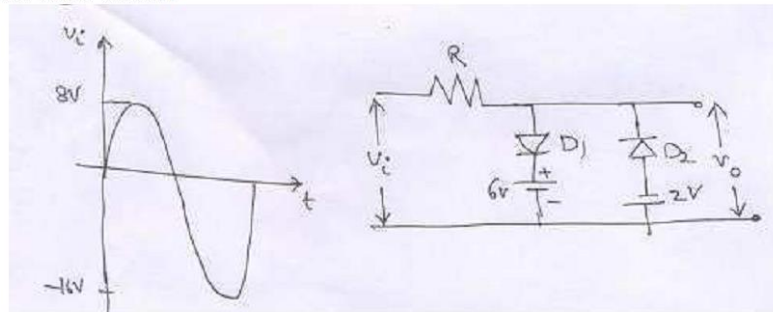
Figure 2a

   (b) Explain negative peak clipper with and without reference voltage.   [8+8]

3. (a) For a common emitter circuit $V_{cc} = 10V$, $RC = 1k\Omega$ I_B=0.2A. Determine

      i. The valve of $h_{FE}(\min)$ for saturation to occor

      ii. If R_c is changed to 220Ω, will the transistor be saturated

   (b) Explain the phenomenon of latching in a transistor.   [8+8]

4. Draw the circuit diagram for Schmitt trigger and explain its operation. What are the applications of the above circuit? Derive the expressions for UTP and LTP.
                                                                              [16]

5. Explain the basic principal of Miller and Bootstrap time base generators and also derive the equations for sweep speed error.   [16]

6. (a) With the help of a circuit diagram and waveforms explain frequency division of an a stable multivibrator with pulse signals.

(b) Explain with the help of block diagram and waveforms for acheiving division of relaxation devices without phase jitter. [8+8]

7. (a) Distinguish between sampling gates and logic gates?

(b) Explain the operation of a chopper amplifier with neat block diagram and waveforms.

(c) Distinguish between unidirectional and bidirectional gates. [4+8+4]

8. (a) Draw the circuit diagram of diode-transistor logic NOR gate and explain its operation.

(b) Draw the output waveform X for the given inputs figure 8b

Figure 8b

⋆ ⋆ ⋆ ⋆ ⋆
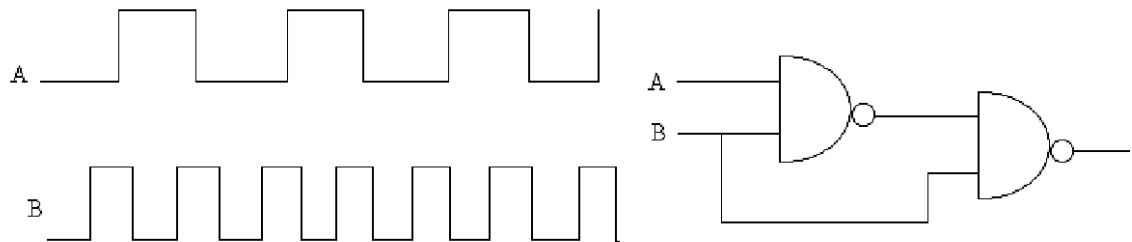
Set No. 3

II B.Tech I Semester Regular Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering and Electronics &
Instrumentation Engineering)
Time: 3 hours   Max Marks: 80
Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain about RLC Ringing Circuit

   (b) Explain RC double differentiator circuit.   [8+8]

2. (a) T=1000 μ sec
      V= 10 V
      Duty cycle = 0.2

        i. Sketch waveform with voltage levels at steady state figure 2(a)iii
        ii. Forward and reverse direction tilt
        iii. A_f / A_r
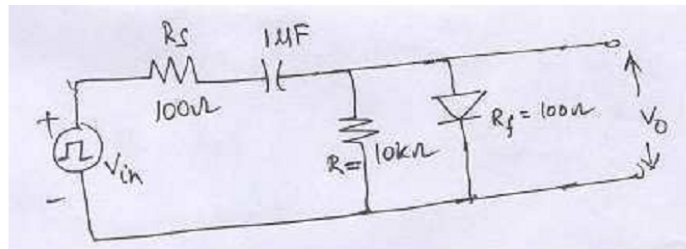
Figure 2(a)iii

   (b) Write a short note on non- linear wave shaping.   [12+4]

3. Explain the following

   (a) Storage and transition times of the diode as a switch

   (b) Switching times of the transistor.   [8+8]

4. What is a monostable multivibrator? Explain with the help of a neat circuit di-
   agram the principle of operation of a monostable multivibrator, and derive an
   expression for pulse width. Draw the wave forms at collector and Bases of both
   transistors.   [16]

5. (a) Define sweep time and restoration time of a voltage time base waveform. What
      is the difference between sweep and sawtooth waveforms?

   (b) In the transistor bootstrap circuit, V_{cc} = 25V, V_{EE} = − 15V, R = 10kΩ, R_E
      = 15kΩ, R_B = 150 kΩ, C= 0.05 μF, C_1 = 100 μF. The gating waveform has
      a duration T_G =300 μSec. The transistor parameters are h_{ie} = 1.1 kΩ, h_{re} =
      2.5×10^{-4}kΩ, h_{fe} = 50, h_{oe} = 1/40

i. Draw the waveforms of i_c, and v_o, labeling all current and voltage levels.

ii. What is the slope error of the sweep?

iii. What is the sweep speed and the maximum value of the sweep voltage?

iv. What is the retrace time T_r for C to discharge completely?

v. Calculate the recovery time T_1 for C_1 to recharge completely. [16]

6. (a) With the help of a circuit diagram and waveforms, explain frequency division of an astable multivibrator with pulse signals.

(b) The relaxation oscillator, when running freely, generates an output signal of peak - to - peak amplitude 100V and frequency 1 kHz. Synchronizing pulses are applied of such amplitude that at each pulse the breakdown voltage is lowered by 20V. Over what frequency range may the sync pulse frequency be varied if 1 : 1 synchronization is to result? If 5 : 1 synchronization is to be obtained ($f_P/f_S = 5$), over what range of frequency may the pulse source be varied? [16]

7. (a) Explain the operation of a six - diode gate.

(b) Write the applications of sampling gates.

(c) Briefly describe the chopper amplifier and sampling scope. [16]

8. (a) Compare the Resistor Transistor logic and Diode Transistor logic families

(b) Explain the wired AND logic with the help of circuit diagram.

[8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Set No. 4

II B.Tech I Semester Regular Examinations, November 2008
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering and Electronics &
Instrumentation Engineering)
Time: 3 hours   Max Marks: 80
Answer any FIVE Questions
All Questions carry equal marks
⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Obtain the response of RC high pass cirucit for an exponential i/p lignal

    (b) A square wave whose peak-to-peak valve is IV, exterds I 0.5V w.r.t. to ground.
        The half period is O.iSec this voltage impressed upon an RC differentating
        circuit whose time constant is 0.2 sec. Determine the maximum and minimum
        valves of the l/p voltages int eh steady state.   [8+8]

2. (a) The input voltage v_i to the two level clipper shown in figure 2a varies linearly
        from 0 to 75 V. Sketch the output voltage v_o to the same time scale as the
        input voltage. Assume Ideal diodes.
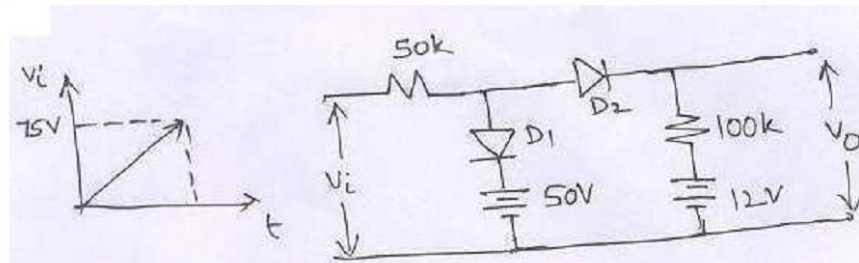
Figure 2a

    (b) Explain positive peak voltage limiters below reference level.   [12+4]

3. (a) Explain with relevant diagram the various transistor switching times

    (b) Explain the storage and transition times of the diode as a switch.   [8+8]

4. Explain about various switching conditions of Schmitt trigger.   [16]

5. (a) What are the methods of generating a time base waveform? Explain each
        method.

    (b) Derive the expression Mathematical relationship between sweep speed error,
        Displacement error and transmission error for an exponential sweep circuit.
                                                                                [16]

6. (a) Describe frequency division employing a transistor a stable multivibrator with
        waveforms.

    (b) Describe frequency division employing a transistor monostable multivibrator
        with waveforms.   [8+8]

7. (a) Describe the working of a four diode gate with necessary diagrams and equations.

   (b) For the four diode gate, $R_L = R_C = 100k \Omega$ and that $R_2 = 2k\Omega$, $R_F = 50\Omega$. For $V_s = 25V$, compute gain A, V_{min} and $(V_c)_{min}$. Compute $(V_n)_{min}$ for V $= V_{min}$.

   [16]

8. (a) Define positive and negative logic system

   (b) Define fan-In, fan-out

   (c) Draw and explain the circuit diagram of a diode OR gate for positive logic.

   [4+4+8]

$\star\star\star\star\star$

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
PULSE AND DIGITAL CIRCUITS
(COMMON TO ELECTRONICS AND COMMUNICATION ENGINEERING,
ELECTRONICS AND TELEMATICS)

Time: 3hours   Max. Marks: 75

Answer any FIVE questions
All Questions Carry Equal Marks
- - -

1.a) The output of a high pass RC circuit for a symmetrical square wave input is shown in Figure.1. Derive the expression for percentage tilt in the output.
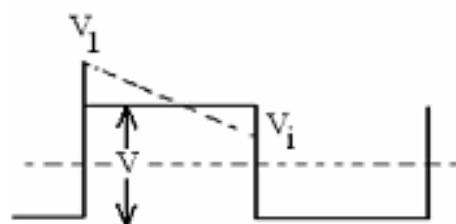
Figure.1

b) An oscilloscope displays a 5Hz square wave with 6% tilt. The signal input has no tilt and is coupled to the oscilloscope via a 4.7μF capacitor. Calculate the input resistance of the oscilloscope.   [10+5]

2.a) Draw the circuit diagram of an Emitter-Coupled clipping circuit. Explain its operation with its transfer characteristic and necessary expressions

b) State and prove clamping circuit theorem.   [8+7]

3.a) A silicon transistor has h_{FE} = 75, I_{CO} = 0.1μA and cut-in voltage V_{γ} = 0.5V. The parameter "n" of avalanche multiplication is 4 and BV_{CBO} = 50V.
i) Calculate BV_{CEO}
ii) Calculate BV_{CER} if R_B = 1.M Ω
iii) Calculate BV_{CEX} assuming V_{BB} = 10V and R_B = 10K.

b) Write about diode switching times.   [10+5]

4.a) What are transpose capacitors? Explain how the commutating capacitors will increase the speed of a fixed-bias binary.

b) For the circuit shown in figure.4, Vcc = 18V, V_{BB} = 6V, V = 6V, Rc = 1.5K, R_1= 5K, R_2 = 25K and h_{FE}(min) of each transistor is 40. Neglect the drop across the forward biased junctions. Indicate all the circuit voltages in the quiescent state and indicate also the voltages immediately after a 5V positive step is applied.   [5+10]

Figure.4

5.a) Draw the circuit of a Boot strap sweep generator and explain its operation. Derive an expression for its sweep time.

  b) Explain with a circuit the working of a UJT sweep circuit and obtain the expressions for the intrinsic standoff ratio (η). [8+7]

6.a) Illustrate with neat circuit diagram, the operation of unidirectional sampling gate for multiple inputs.

  b) Explain with circuit diagram the operation of a two input sampling gate which does not have any loading effect on control signal. [7+8]

7.a) With neat waveforms explain sine wave synchronization and compare it with pulse synchronization.

  b) The relaxation oscillator when running freely, generates an output sweep amplitude of 100V and frequency 1kHz. Synchronizing pulses are applied such that at each pulse the breakdown voltage is lowered by 20V. Over what frequency range the synchronizing pulse frequency may be varied if 1:1 synchronization is to result? [8+7]

8.a) Realize two-input AND & OR gates using diodes and explain their operation with the help of truth-tables.

  b) Realize a three-input NOR gate using Resistor Transistor Logic and explain its operation with the help of truth-table. [8+7]

****

Time: 3hours   Max. Marks: 75

Answer any FIVE questions
All Questions Carry Equal Marks
- - -

1.a)   Prove that an RC circuit behaves as a reasonably good integrator if $RC > 15T$, Where T is the period of an input '$E_m \sin \omega t$'.

 b)   What is the ratio of the rise time of the three sections in cascade to the rise-time of Single section of low pass RC circuit?   [8+7]

2.a)   A square wave input of period T = 1000 µ sec, Vpeak = 10V and Duty cycle = 0.2 is applied to the circuit shown in figure.2. Given, $R_S = 100\Omega$, C = 1µF, R = 10K & Diode forward resistance, $R_f = 100\Omega$.
   i) Sketch the output waveform with voltage levels at steady state.
   ii) Forward and reverse direction tilt
   iii) A_f / A_r
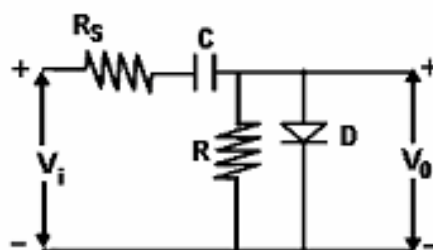
figure.2

 b)   Write a short note on voltage comparators.   [12+3]

3.a)   Explain the terms pertaining to transistor switching characteristics.
   i) Rise time.   ii) Delay time.   iii) Turn-ON time.
   iv) Storage time.   v) Fall time.   vi) Turn-OFF time.

 b)   Calculate the maximum operating frequency of a diode with storage time of 1ns and transition time of 8ns.   [12+3]

4.a)   What do you mean by collector catching diodes? Explain the need of these diodes in a bistable multivibrator.

 b)   For the given circuit shown in figure. 4, find UTP & LTP. What is this circuit called? Data given $h_{fe}(min)$ = 40, $V_{CE}(sat)$ = 0.1 V, $V_{BE}(sat)$=0.7 V, V_γ = 0.5V, $V_{BE}(active)$ = 0.6V.

                                                                                        [5+10]
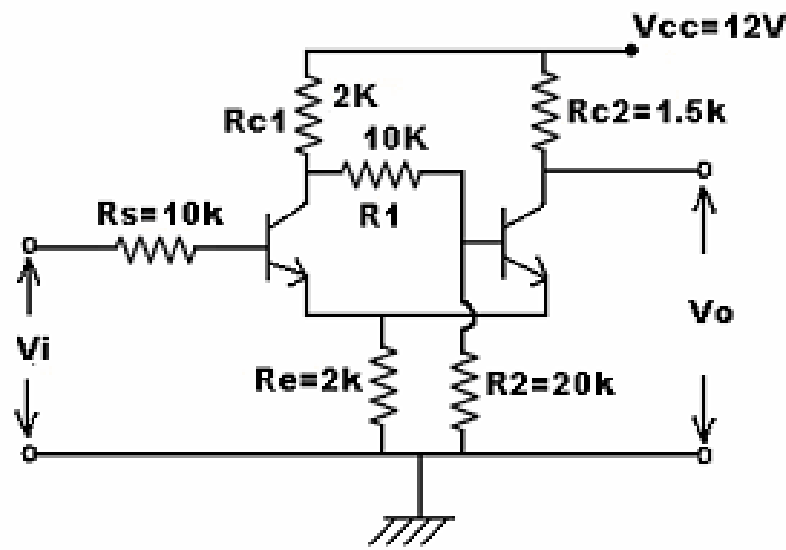
figure.4

5.a) Define the three errors that occur in a sweep circuit and obtain an expression for these errors for an exponential sweep circuit.

b) In the UJT sweep circuit, V_{BB} = 20V, V_{yy} = 50V, R = 5k, C = 0.01 micro F. UJT has η= 0.5. Calculate
i) Amplitude of sweep signal
ii) Slope and displacement errors and
iii) Estimated recovery time. [8+7]

6.a) With the help of a neat diagram, explain the working of two-diode sampling gate.

b) Derive expressions for gain and minimum control voltages of a bi-directional two- diode sampling gate. [7+8]

7.a) Explain how monostable multivibrator is used as frequency divider?

b) Write short notes on
   i)   Phase delay
   ii)   Phase jitters [7+8]

8.a) What is logical noise in a diode AND gate? Explain how it can be reduced by connecting a clamping diode in the circuit?

b) Realize NAND & NOR gates using CMOS Logic and explain their operation with the help of truth-tables. [7+8]

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
PULSE AND DIGITAL CIRCUITS
(COMMON TO ELECTRONICS AND COMMUNICATION ENGINEERING,
ELECTRONICS AND TELEMATICS)

Time: 3hours   Max. Marks: 75

Answer any FIVE questions
All Questions Carry Equal Marks
- - -

1.a) What are the drawbacks of uncompensated attenuators? Prove that the condition to prevent input signal from distortion is $R_1C_1 = R_2C_2$, in an adequately compensated attenuator.

  b) An RC differentiator circuit is driven from a 500Hz symmetrical square wave of 10V Peak-to peak. Calculate the output voltage levels under steady state if RC = 1msec.[10+5]

2.a) Draw the basic circuit diagram of negative peak clamper and explain its operation.
  b) For the circuit shown in figure.2, an input voltage V_i linearly varies from 0 to 150V is applied. Sketch the output voltage V_O and transfer characteristics. Assume ideal diodes.

[5+10]
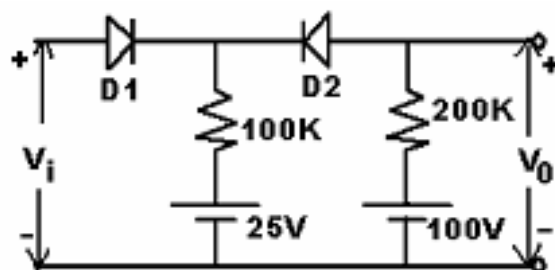
figure.2

3.a) Consider the transistor switch in CE configuration shown in figure.3, operated with $V_{CC} = 12V$ and Vbb = 0V. It is given that $R_2 = 2R_1 = 68K\Omega$, $R_C = 2.2K\Omega$. Determine
   i) The values of I_B and I_C of the transistor.
   ii) The minimum value of h_{FE} required for the transistor to operate in saturation when it is in ON state?
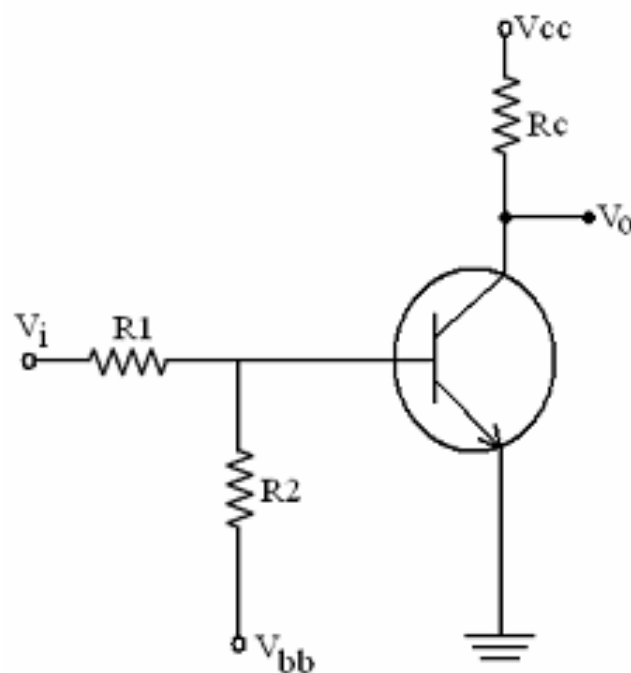
figure.3

b)   Explain Zener & Avalanche breakdown mechanisms in diodes.   [10+5]

4.   Draw and explain the circuit of Astable Multivibrator with necessary waveforms and also derive the expression for its frequency of oscillations.   [15]

5.a)   What are the essential requirements of TV horizontal sweep circuit? How do you achieve them using a current sweep?
  b)   With neat sketches and necessary expressions, explain the transistor Miller time-base generator.   [7+8]

6.a)   Draw the circuit of an emitter-coupled bidirectional sampling gate and explain.
  b)   What is Pedestal? How pedestal can be reduced in a sampling gate circuit?   [7+8]

7.a)   Explain the principle of "synchronization" and 'synchronization with frequency division'.
  b)   Explain the method of pulse synchronization of relaxation devices, with examples. [7+8]

8.a)   Realize a two-input NAND gate using Diode Transistor Logic and explain its operation with the help of truth-table.
  b)   Explain the terms:
      i) Wired- AND connection   ii) Current Source – Sink logic   iii) Tri-state logic [6+9]

****

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
PULSE AND DIGITAL CIRCUITS
(COMMON TO ELECTRONICS AND COMMUNICATION ENGINEERING,
ELECTRONICS AND TELEMATICS)

Time: 3hours   Max. Marks: 75

Answer any FIVE questions
All Questions Carry Equal Marks
- - -

1.a) Prove that for any periodic input waveform the average level of the steady state output signal from the RC high pass circuit is always Zero.

  b) Draw the RC low pass circuit. With necessary waveforms and expressions explain its working for a step voltage input.   [8+7]

2.a) Explain negative peak clipper with and without reference voltage.

  b) Sketch the steady state output voltage for the clamper circuit shown in figure.2 and locate the output d.c level and the zero level. The diode used has R_f = 1KΩ, R_r = 600 KΩ, V_γ = 0. C = 0.1μF and R = 20 KΩ. The input is a $\pm$ 20 Volts square wave with 50% duty cycle.   [5+10]
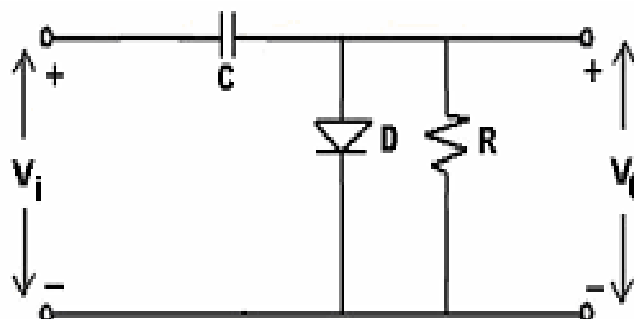
figure.2

3.a) The circuit shown in figure.3 uses a silicon transistor with h_{FE} = 100 and V_{BE} = 0.7V. Find the value of R_B which saturates the transistor, when input voltage is +5V. Given R_C = 1K & V_{CC} = +5V.
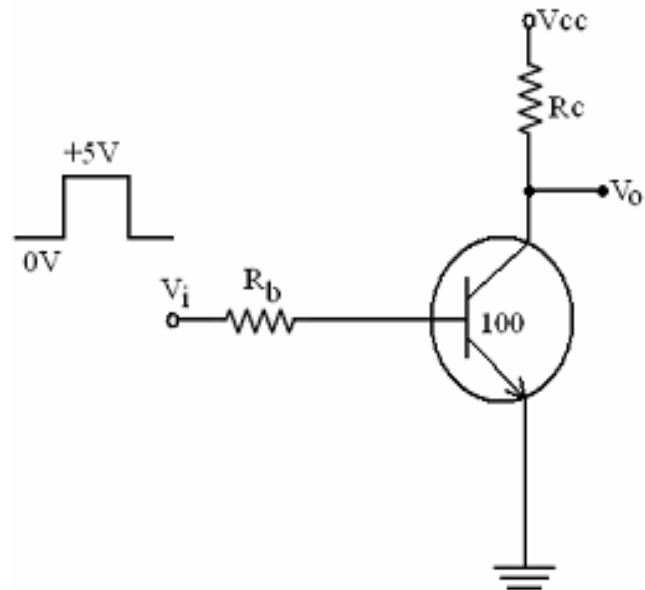
figure.3

b) Write about diode switching times. [10+5]

4. What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a monostable multi, and derive an expression for pulse width. Draw the wave forms at collector and Bases of both transistors. [15]

5. A UJT is used as a switch across a sweep capacitor C which charges through R. A single voltage supply V_{BB} is used in the circuit. If V_V&V_P are the valley and peak voltages respectively,
a) Prove that the sweep duration is exactly given by $T_s = RC \ln (V_{BB} - V_V)/(V_{BB} - V_P)$
b) Prove that if $V_{BB} >> V_V$, then $T_s \approx RC \ln [1/(1-\eta)]$ [8+7]

6.a) Draw the circuit of FOUR-DIODE sampling gate. Derive expressions for its gain(A) and V_{min}.
b) Explain the application of sampling gate in a sampling scope. [10+5]

7.a) With neat sketches and necessary waveforms explain how an astable multivibrator can be synchronized?
b) A symmetrical astable multivibrator using transistor operates from 10V supply has a period of 1msec. Triggering pulses of spacing 750 µsec are applied to one base through a small capacitor from a high-impedance source. Find the minimum triggering pulse amplitude required to achieve 1:1 synchronization. [8+7]

8.a) Realize a three-input NAND GATE using Transistor Transistor Logic. Explain its operation with Totem-pole load.

B.Tech II Year - II Semester Examinations, April-May, 2012
PULSE AND DIGITAL CIRCUITS
(Common to BME, ECE, ETM)

Time: 3 hours   Max. Marks: 75

Answer any five questions
All questions carry equal marks
- - -

1.a) Explain perfect compensation, over compensation and under compensation with respect to attenuator circuits?

b) Explain why the initial voltage distribution in an attenuator is determined by the capacitors?

c) Explain why the final voltage distribution in an attenuator is determined by the resistors?

d) Why does a resistive attenuator need to be compensated?   [6+3+3+3]

2.a) The ideal transfer characteristic of particular clipper circuit is shown in Figure.1. Design the circuit using ideal diodes and draw the input-output waveforms with proper explanation, if $V_i = 10 \sin \omega t$.
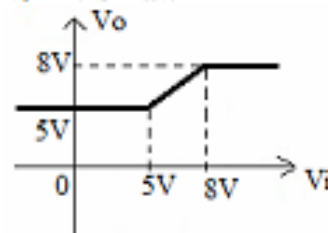
Figure.1

b) With neat diagrams, explain the use of clamper circuit in television receivers as DC restorer?   [10+5]

3.a) Design a common-emitter transistor switch shown in Figure.2, operated with Vcc = 18V and -Vbb = -12V. The transistor is expected to operate at $I_C = 8mA$, $I_B = 0.75mA$. Assume $h_{FE} = 25$, $V_{BE}(sat) = V_{CE}(sat) = 0V$ and $R_2 = 6 R_1$.
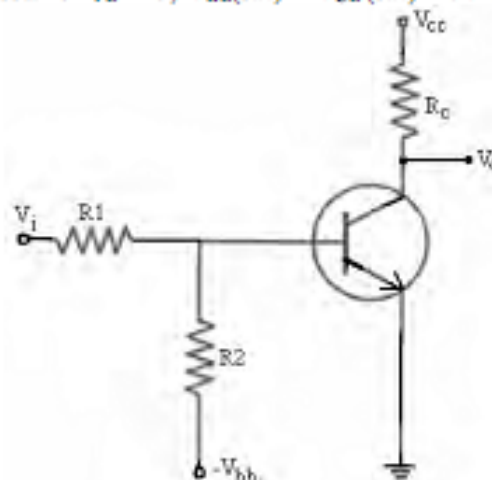
Figure.2

b) Define storage and transition times with respect to diodes?   [12+3]

4. A self-biased binary uses n-p-n transistors have maximum values of $V_{CE}(sat)=0.4V$ and $V_{BE}(sat) = 0.8V$ and V_{BE} cutoff = 0V. The circuit parameters are $V_{CC}= 15V$, $R_C = 1K\Omega$, $R_1 = 6K\Omega$, $R_2 = 15K\Omega$ and $R_E = 500\Omega$.
a) Find the stable-state currents and voltages.
b) Find the minimum value of h_{FE} required for BJT to provide the above stable state values.
c) Also determine $I_{CBO}(max)$ to which I_{CBO} raises as temperature rises where neither BJT is off. [15]

5.a) Draw the circuit of simple current time-base generator and explain its operation with the help of neat waveforms and necessary equations. Also derive expression for sweep speed error(e_s), by considering the effect of internal resistance of inductor (R_L) and collector saturation resistance (R_{CS}) of the transistor.
b) Explain why an operational integrator is used in transistorized Miller sweep circuit? [12+3]

6.a) Draw and explain the circuit diagram of a six-diode sampling gate. Derive expressions for V_{Cmin}
b) For the four diode gate with a divider resistance $R=100\Omega$, $V_S=25V$, $R_f =20$, $R_L = R_C = 200K\Omega$. Find V_{Cmin} and V_{min}? [10+5]

7.a) What type of synchronization is used when the interval between pulses is less than or equal to the natural period of the wave form generator? Explain it briefly.
b) With the help of neat diagram and wave forms explain the use of a monostable relaxation circuit as a frequency divider? [7+8]

8.a) Draw the circuit of a 2-input TTL totem-pole output NAND gate with the help of four transistors. Explain why the output of this gate cannot be wire-ANDed?
b) Explain the function of multi emitter transistor used in the above circuit. What is the disadvantage of using back to back diodes in place of multi emitter transistor?
c) Explain why this logic circuit is faster than open collector logic circuit? [6+6+3]

B.Tech II Year - II Semester Examinations, April-May, 2012
PULSE AND DIGITAL CIRCUITS
(Common to BME, ECE, ETM)

Time: 3 hours　　　　　　　　　　　　　　　　　　　　Max. Marks: 75

Answer any five questions
All questions carry equal marks
- - -

1.a) Obtain an expression for the input impedance of RC differentiating circuit. Compare it with that of RL differentiating circuit.

b) A pulse of 5V amplitude and width of 0.5 msec. is applied to high pass RC circuit consisting of R = 22 KΩ and C = 0.47μF. Estimate the output voltage levels and sketch the waveform. Also determine the percentage tilt in the output? [5+10]

2.a) A voltage signal of $10 \sin \omega t$ is applied to the circuit with ideal diodes shown in Figure.1. Estimate the maximum & minimum values of output waveform and maximum current through each diode. Also draw the input-output waveforms with proper explanation.
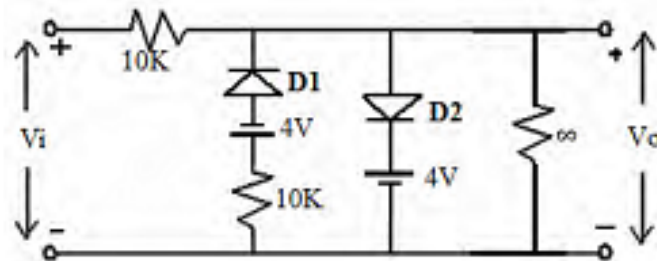
Figure.1

b) A square wave input is applied to the clamper circuit shown in Figure.2. By taking the effect of source resistance, R_s, the diode forward dynamic resistance, R_f and the diode reverse dynamic resistance, R_r into account, draw the equivalent circuits for the following cases:
i) When the diode is conducting　　　　ii) When the diode is not conducting. [9+6]

Figure.2

326
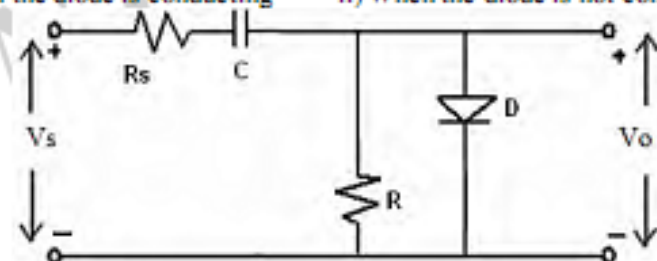
3.a) A simple diode-switch circuit and the input signal applied to it are shown in Figure.3. Draw and explain the waveforms representing the variation in minority carrier concentration, diode current I, and diode voltage V_D with respect to input signal variations.
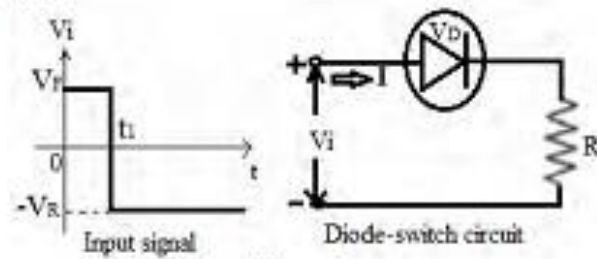
Figure.3

b) Derive an expression for collector-to-emitter breakdown voltage, with open-circuited base, BV_{CEO} in terms of collector-to-base breakdown voltage, with open-circuited emitter, BV_{CBO}. [8+7]

4. What for the circuit shown in Figure.4 is used? Discuss the role of the diodes, D1 and D2 in the circuit. With neat waveforms and necessary equations, explain the operation of the circuit, without D1, D2, R3 and $R3^1$. [15]
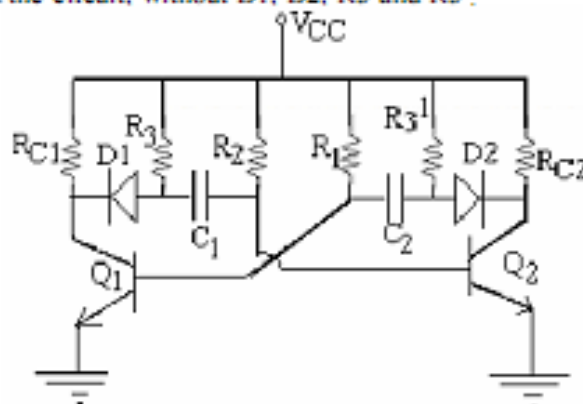
Figure.4

5.a) Draw and explain the operation of transistorized Miller sweep generator. Show that the sweep speed for Miller circuits is same as in the case where the capacitor, C charges through a resistor, R directly from the source, V.

b) A transistor bootstrap ramp generator is to produce a 15V, 5ms output to a 2KΩ load resistor. The ramp is to be linear within 2%. Design a suitable circuit using Vcc = 22V, -VEE = -22V and transistor with $h_{fe(min)}$ = 25, h_{ie} = 1.1KΩ, h_{re}=2.5x10^{-4}, h_{oe} = 25μA/V, $V_{BE(sat)}$ = 0.8V, $V_{BE(active)}$ = 0.7V, $V_{CE(sat)}$ = 0.2V. The input pulse has an amplitude of -5V, pulse width = 5ms and space width = 2.5ms. [7+8]

6.a) Explain how to cancel the pedestal in a sampling gate with suitable circuit diagram.

b) Explain the function of a sampling gate is used in Sampling Scopes. [7+8]

7.a) Explain the factors which influence the stability of a relaxation divider with the help of a neat waveforms.

b) A UJT sweep operates with valley voltage (V_v)= 3V, peak voltage (V_p) =16V and η = 0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1 KHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronism with the sync signal? [7+8]

8.a) With the help of circuit diagram explain the purpose of clamping diode in a positive diode AND gate.

b) What is meant by active pull-up? Draw the circuit of TTL active pull-up NAND gate and explain its operation with the help of function table? [7+8]

B.Tech II Year - II Semester Examinations, April-May, 2012
PULSE AND DIGITAL CIRCUITS
(Common to BME, ECE, ETM)

Time: 3 hours   Max. Marks: 75

Answer any five questions
All questions carry equal marks
- - -

1.a) Which linear circuit is required to obtain the output for the given input shown in Figure.1. Explain its operation with necessary equations?
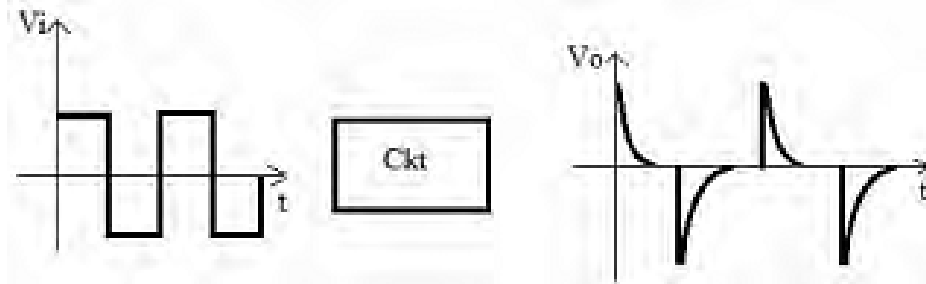
Figure.1

b) A constant voltage of 100V is applied to a series RLC circuit with L=10H, R=20Ω and C=5F. The initial current in the circuit is zero but there is an initial voltage of 50V on the capacitor in a direction which opposes the applied source. Find the expression for the current in the circuit and derive the expressions used.

[7+8]

2.a) The ideal transfer characteristic of particular clipper circuit is shown in Figure.2. Design the circuit using ideal diodes and draw the input-output waveforms with proper explanation, if $V_i = 15 \sin \omega t$.
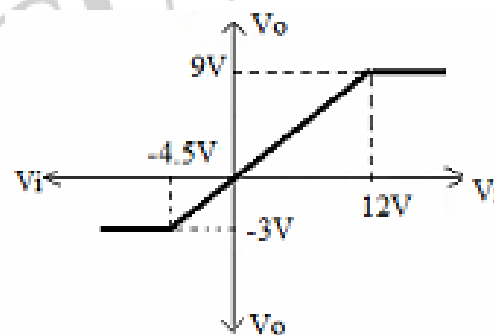
Figure.2

b) With neat diagrams, explain the use of clamper circuit in television receivers as DC restorer?

[10+5]

3.a) With neat sketches and necessary expressions, explain the affect of temperature on the saturated junction voltages of a transistor.

b) For a CE transistor circuit shown in Figure.3, $V_{CC} = 15V$, $R_C = 1.5K$ and $I_B = 0.3mA$. Determine the minimum value of h_{FE} required for saturation to occur.

[7+8]
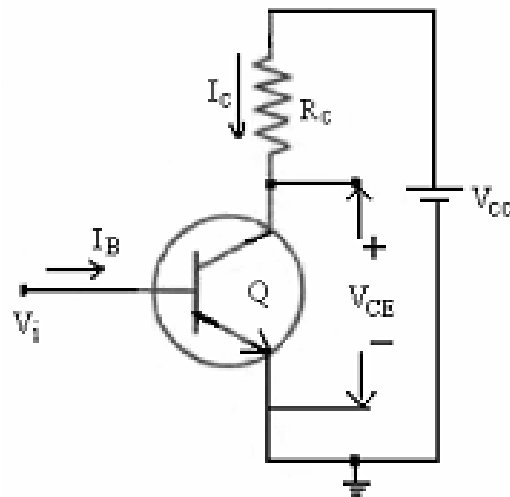
Figure.3

4.a) What are transpose capacitors? Explain how the commutating capacitors will increase the speed of a fixed-bias binary.

b) Design and draw a collector-coupled ONE-SHOT using silicon npn transistors with h_{FE}(min) =20. In stable state, the transistor in cut-off has $V_{BE} = -1V$ and the transistor in saturation has base current, I_B which is 50% excess of the I_B(min) value. Assume $V_{CC} = 8V$, I_C(sat) =2mA, delay time = 2.5ms & $R_1 = R_2$. Find R_C, R, R_1, C and V_{BB}. [3+12]

5.a) Draw and explain the circuit of transistorized Bootstrap sweep generator. Derive an expression for retrace interval, T_r.

b) A transistorized Miller sweep generator has the following parameters: R=1.2MΩ, $R_2 = 15$ MΩ, $R_3 = 120$ KΩ, $R_4 = 27$ KΩ, $R_e = 100$ KΩ and $V_{BB} = 40V$. The transistor h-parameters are $h_{fe} = 50$, $h_{ie} = 1.1KΩ$, $h_{re} = 2.5 \times 10^{-4}$ and $h_{oe} = 25\mu A/V$. If the output sweep amplitude is 25V, find the slope error? [7+8]

6.a) Explain how the loading of the control signal is reduced when the number of inputs increases in a sampling gate?

b) Draw the circuit diagram of a unidirectional sampling gate which delivers an output only at the coincidence of a number of control voltages and explain its working. [7+8]

7.a) With the help of a circuit diagram and waveforms, explain how frequency division is done by an astable multivibrator?

b) Draw and explain the block diagram of frequency divider without phase jitter. [8+7]

8.a) Which is the fastest non-saturated logic family? With a neat circuit diagram explain its operation in view of logic of operation, noise margin, propagation delay and fan-out.

b) In 4-input NAND gate, two inputs are to be used. What are the options available for the unused inputs and which one is the best and why? [10+5]

B.Tech II Year - II Semester Examinations, April-May, 2012
PULSE AND DIGITAL CIRCUITS
(Common to BME, ECE, ETM)

Time: 3 hours   Max. Marks: 75

Answer any five questions
All questions carry equal marks
- - -

1.a)   An inductor does not allow sudden changes in current and a capacitor does not allow sudden changes in voltage. Justify with relevant equations.
  b)   What are the disadvantages of RL linear wave shaping circuit compared to RC circuit?
  c)   A symmetrical square wave of $\pm 5V$ at a frequency of 5 KHz is applied to a high pass RC circuit with a cut-off frequency of 20 KHz. Sketch the steady state input and output voltage waveforms. Calculate the steady state output voltage levels?
                                                                    [4+3+8]

2.a)   A voltage signal of 10 sin ωt is applied to the circuit with ideal diodes shown in Figure.1. Estimate the maximum & minimum values of output waveform and maximum current through each diode. Also draw the input-output waveforms with proper explanation.
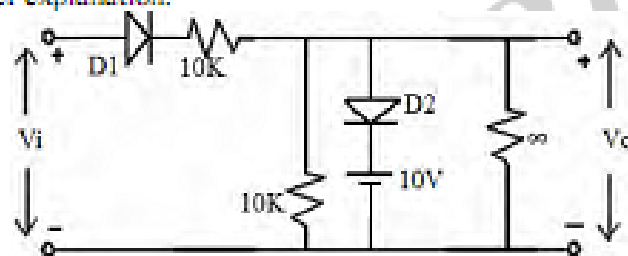
Figure.1
  b)   Explain the steps to analyze a clamping network with an example?   [10+5]

3.a)   Calculate the output levels of the circuit shown in Figure.2, for the inputs 0 and -6 Volts and verify that the circuit is an inverter. What is the minimum value of h_{FE} required? Neglect junction saturation voltages and assume an ideal diode.

b) With neat sketches representing minority-carrier density distribution as a function of distance from junction, explain the diode reverse recovery time in detail?

[10+5]

4.a) Explain various methods to improve the resolution of a binary.

b) Design a Schmitt trigger circuit using npn silicon transistors with $V_{BE} = 0.7V$, $V_{CE(sat)} = 0.2V$, $h_{fe}(min) = 60$ and $I_{C(ON)} = 3mA$ to meet the following specifications: $V_{CC} = 12V$, upper threshold voltage, $V_{UT} = 4V$, lower threshold voltage, $V_{LT} = 2V$.

[3+12]

5.a) Prove that when restoration time is zero, saw-tooth output waveform can be obtained from a sweep generator circuit.

b) The transistorized Bootstrap sweep generator circuit has the following parameters: $V_{CC} = 25V$, $-V_{EE} = -15V$, $R = 10 K\Omega$, $R_B = 150 K\Omega$, $R_E = 1K\Omega$, $C = 0.05 \mu F$. The gating waveform has 300μs duration. The transistor parameters are $h_{ie} = 1.1K\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 25\mu A/V$.

i) Draw the waveforms for the collector current of input transistor (Q_1), I_{C1} and output voltage at the emitter of output transistor (Q_2), labeling all current and voltage levels?

ii) What is the slope error of the sweep?

iii) What is the sweep speed and the maximum value of the sweep voltage?

iv) What is the retrace time T_r for C to discharge completely?

v) Calculate the recovery time T_1 for C_1 to recharge completely?

[7+8]

6.a) Draw the bidirectional diode sampling gate in the form of a bridge network and explain its working.

b) Explain how a sampling gate is used in chopper amplifier?

[8+7]

7.a) What do you mean by synchronization ?

b) What is the condition to be met for pulse synchronization?

c) Compare sine wave synchronization with pulse synchronization?

[3+6+6]

8.a) Compare the RTL and DTL logic families in terms of Fan out, propagation delay, power dissipated per gate and noise immunity.

b) What is meant by tri-state logic? Draw the circuit of tri-state TTL logic and explain its operation in detail?

[8+7]

Code No: R09220403

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B. Tech II Year - II Semester Examinations, November/December, 2012
PULSE AND DIGITAL CIRCUITS
(COMMON TO ECE, BME, ETM)

Time: 3 hours

Max. Marks: 75

Answer any five questions
All questions carry equal marks
- - -

1.a) The periodic wave form shown in Fig.1(a) is applied to an RC integrating network whose time constant is 10μsec. Sketch the output wave form. Calculate the maximum and minimum values of the output voltage with respect to ground under steady state conditions. Also, calculate and plot the output for the first two cycles of the input.
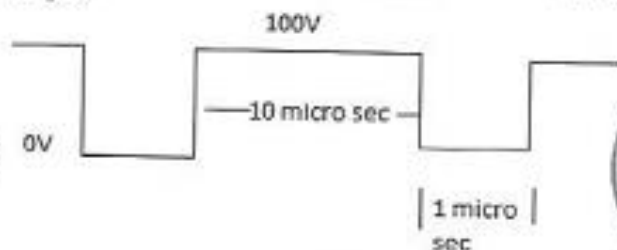
Fig.1(a)

b) Why does a resistive attenuator need to be compensated?
c) Why are RC circuits commonly used compared to RL circuits?   [9+3+3]

2.a) Draw a circuit, to transmit that part of a sine wave which lies between -3V and +6V. Explain its working with transfer characteristics.
b) What are the applications of a comparator?
c) Design a diode clamper to restore the positive peaks of 1 KHz input signal to a voltage level equal to 5V. Assume the voltage drop across diode as 0.7V.   [5+5+5]

3.a) What do you mean by delay time of a transistor? What factors contribute to it?
b) Explain how transistor acts as a switch? Draw the switching characteristics of it and explain.   [7+8]

4.a) Design a self-biased symmetrical binary with the following specifications: $V_{cc}=10V$, $R_c=1Ω$, $V_{BE}(sat)=0.3V$, $β_{ON}=20$, operating frequency up to 80kHz, impedances of the triggering source $=250Ω$.
b) With the help of a neat circuit diagram, explain the working of an Astable multivibrator.   [7+8]

5.a) What are the different methods of generating a time base waveform? Explain them briefly.
b) Design a transistor bootstrap ramp generator to provide an output amplitude of 12V over a time period of 2ms. The input signal is a negative going pulse with an amplitude of 5V, a pulse width of 2ms and time interval between pulses is 0.5ms. the load resistance is 1KΩ and the ramp is to be linear with 1%. The supply is to be ±15V. Take $h_{fe}(min)=80$.   [8+7]

6.a) Compare the unidirectional and bidirectional sampling gates.
 b) Draw the circuit diagram of six-diode sampling gate and explain its working.

[5+10]

7.a) Explain the frequency division with respect to a sweep circuit.
 b) Explain working of monostble relaxation device as a divider.

[7+8]

8.a) Draw the circuit diagram of AND gate using diodes and explain its working.
 b) Explain the working of TTL NAND gate with suitable circuit diagram.

[7+8]

Code No: R09220403

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year II Semester Examinations, May-2013
Pulse and Digital Circuits
(Common to ECE, BME, ETM)

Time: 3 hours

Max. Marks: 75

Answer any five questions
All questions carry equal marks
- - -

1.a) Compare linear wave shaping with non-linear wave shaping.
 b) A symmetrical square wave of peak-to-peak amplitude 'V' and frequency 'f' is applied to a high pass circuit. Show that the percentage tilt is given by

$$P = \frac{1 - e^{-1/2RCf}}{1 + e^{-1/2RCf}} \times 100\%$$

[7+8]

2.a) Explain the response of the clamping circuit when a square wave input is applied under steady state conditions.
 b) Explain the effect of diode characteristics on clamping voltage. [8+7]

3. Write short notes on:
 a) Diode switching times
 b) Switching characteristics of transistors
 c) FET as a switch. [4+7+4]

4. What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a monostable multivibrator, and derive an expression for pulse width. Draw the wave forms at collector and base of both transistors. [15]

5.a) Why the time base generators are called sweep circuits? Write the differences between the voltage and current time base generators?
 b) With neat sketches and necessary expressions, explain the transistor Miller time-base generator. [9+6]

6.a) With the help of a neat diagram, explain the working of four-diode sampling gate. Derive expressions for its gain(A) and V_{min}.
 b) Explain the application of sampling gate in a sampling scope. [10+5]

7.a) With the help of a neat circuit diagram and waveforms explain synchronization of a sweep generator with pulse signals.
 b) Compare sine-wave synchronization with pulse synchronization. [8+7]

8.a) Realize a three-input NAND gate using Transistor-Transistor Logic. Explain its operation with Totem-pole load.
 b) With reference to logic gates, explain the terms:
 (i) Fan-out, (ii) Noise Margin, (iii) Propagation Delay, (iv) Figure of Merit. [7+8]

18.Assignment topics

Unit – 1:

1. a. Derive the output equations and draw the output wave forms of a RC low pass circuit for the pulse and the square waveform inputs.
    b. How an RC low pass circuit works as an integrator?
2. a). Derive the expression for percentage tilt P of a square wave output of a RC high pass circuit.
    b). Why compensation is required in attenuator circuits? Derive the expression for perfect compensation.
3. a. A 100 Hz square wave is fed to an RC circuit. Calculate and plot the waveform under the following conditions, The lower 3-dB frequency is 1) 3 Hz 2) 30 Hz 3)300 Hz
    b. Derive expression for rise time in a RC low pass circuit.
4. a. Derive the output equations and draw the output waveforms of a RC high pass circuit for the square wave and ramp signals as inputs.
    b. What is the amplitude and gain of a sinusoidal input in a RC high pass circuit?
5. a) Explain how a high pass RC circuit works as a differentiator. Also, explain double differentiation.
    b) Explain about RLC ringing circuit

Unit – 2:

1. a. what is non-linear wave shaping? What is clipping ? Explain the operation of below mentioned circuits with circuit diagrams, transfer characteristics and waveforms i) series positive clipper with and without V_R. ii) Shunt negative clipper with and without V_R.
    b) For a 2-level clipper with peak input 100V and forward bias diode reference voltage 75V and reverse bias diode reference voltage 50V, sketch the transfer characteristics, input and output voltage waveforms. Consider the diodes as ideal.

2. Explain the operation of transistor clippers (common emitter type and emitter follower type) with neat sketches.
3. a. What is clamping operation? Explain the operation of biased positive peak clamper with output waveforms.
    b. What is the effect of source resistance and the diode resistance in clamping circuits?

4. a. State and prove clamping circuit theorem.
    b. Draw the output waveform of a practical clamping circuit when a square wave is given as input. Derive the relation between Δ_f and Δ_r in this case.

5. a) What is synchronized clamping? Draw the circuit and explain its operation.
    b) Explain the operation of diode comparator. Briefly mention various applications of comparators.

Unit – 3 a:

1. a. How the minority carriers are distributed in a p-n junction diode during forward biased condition and the reverse biased condition.
    b. Draw the Ideal and piecewise linear model diode characteristics and explain.
2. a. Explain the operation of a diode as switch. What is reverse recovery time, storage time and transition time of a diode? Draw the switching characteristics of the diode along with t_{rr}, t_s and t_t timings.

b. Explain Zener break down(Zener diode) and Avalanche break down(PN junction diode) mechanisms.
3. a. Explain the operation of a transistor as switch with its switching characteristics.
   b. Define the following for transistor switch

i) Rise time ii) Fall time iii) Storage time   iv) Delay time v) Switch ON time

vi) Switch OFF time

4. a. Explain the breakdown voltage consideration of transistor. Derive expression for BV_{CEO} in terms of BV_{CBO}.
   b. Explain the saturation parameters of transistor and their variations with temperature.
5. a. Explain the operation of Silicon Controlled Switch (SCS) and give its applications.
   b. Calculate the min ß required for a fixed bias common emitter Si transistor, where V_{CC}=10V, R_c= 1 KΩ, R_b= 10 K Ω, Vi= a square wave of 5V peak to peak. Draw the circuit.

Unit – 3. b:

1. a. What is a sampling gate? How it differs from logic gate?
    b. What are the other names for the sampling gates?
    c. Compare Unidirectional sampling gates with bi-directional sampling gates.
2. a. Explain diode based unidirectional sampling gates operation for multiple inputs.
    b. What is a pedestal? How it is reduced in Transistor based bidirectional sampling gates?
3. Explain the operation of the two diode bidirectional sampling gate. Derive the expression for Gain, control voltage Vc min and Vn min for this circuit.
4. a. Draw the circuits for the two types of the 4 diode bidirectional sampling gates and explain their operation. Derive the expression for Gain, Vc min and Vn min for these gates.
    b. Draw the circuit for the 6 diode bidirectional sampling gate and explain its operation.
5. Name various applications of the Sampling gates. How Sampling gates can be used in
    a. Chopper amplifiers
    b. Sampling Scopes

Unit – 4 a:

1. What is monostable multivibrator? Explain with the help of neat circuit diagram the principle of operation of monostable multivibrator, and derive the expression for pulse width. Draw the waveforms at collector and base of the both transistors.
2. a) Draw the circuit of bi-stable multivibrator with symmetrical collector triggering.
    b) Write the applications bistable and monostable multivibrators
3. a) Draw the circuit diagram of Astable multivibrator to obtain the frequency division by 5. Explain its working with waveforms.
    b) Why collector catching diodes are used in multivibrators?
4. Explain and explain the operation of Schmitt trigger with neat sketches, and derive the expressions for UTP and LTP.
6. Design a monostable multivibrator circuit that produces a pulse width of 10ms. Assume hfe= 30,

$V_{CE(sat)}$=0.3V, $V_{BE(sat)}$= 0.7V, $I_{c(sat)}$=5mA, V_{cc}=6V, V_{BB}= -1.5V.

Unit – 4 b:

1. Explain the principle of working of exponential sweep circuit with a circuit diagram. What are slope error, transmission error and displacement error? Derive the expressions for these errors for the exponential sweep? What is the relation between these three errors?
2. Draw the characteristics of the UJT. Draw the circuit diagram of the relaxation oscillator and obtain the value of the frequency of the same.

3. Explain the basic principle of working of Boot-strap time base generator. Draw the circuit diagram for the transistor based boot-strap time base generator and derive the expressions for Ts and Tr for the same

4. Explain the basic principle of working of Millar type time base generator. Draw the circuit diagram for the transistor based Millar time base generator and derive the expressions for the sweep speed error for the same.

5. a. What are the differences between voltage and current time base generators?
   b. What are the applications of the time base generators?
   c. What are the various methods of generating a time base waveforms?
   d. Draw the circuit of a simple current sweep generator and explain its operation.

Unit – 5.a:

1. a. Explain the principle of 'synchronization' and 'synchronization with frequency division'.
   b. With the help of a neat circuit diagram and waveform, explain synchronization of a UJT sweep generator with pulse inputs. What is the condition to be met for pulse synchronization?
   c. Explain the frequency division with respect to a sweep circuit.

2. a. What are Phase Delay and Phase Jitter? Draw and explain the block diagram of a frequency divider with out phase jitter
   b. Explain the factors which influence the stability of a relaxation divider, with the help of neat waveforms.

3. With the help of a circuit diagram and waveforms, explain how frequency division is done by a Mono-stable multivibrator?
   b. Compare sine wave synchronization with pulse synchronization.

4. A) With the help of a circuit diagram and waveforms, explain how frequency division is done by an astable multivibrator for positive pulse and negative pulse synchronization.
   B) Draw the circuit diagram of an astable Multivibrator to obtain frequency division by 6.

5. a. Explain the synchronization of sweep circuit with symmetric signals.
   b. How a sine wave frequency division is done with a sweep circuit?
   c. Draw the block diagram and explain the operation of Sinusoidal divider using Regeneration and modulation.

Unit -5 b:

1. a. Design a 2 input TTL NAND gate with totem-pole output and explain its operation.
   b.   Define the following parameters
        i) Fan-in   ii) Fan-out   iii) Noise margin   iv) Propagation delay   v) Power dissipation
        vi) Speed power product.   vii) Figure of merit

2. a) Design a 2 input NOR gate using ECL logic family.
   b) Explain about positive and negative logic systems.
   c) Explain wired logic in TTL logic family.

3. a) Compare RTL, TTL, ECL (CML) and DTL logic families in terms of Fan-out, Propagation delay, Power dissipation and Noise immunity.
   b) Design a 3-input NAND gate using DTL logic family and explain its operation with truth table.
   c) With the help of a circuit diagram, explain the purpose of clamping diode in a positive diode AND gate.

4. a) Design a 2 input NOR gate using RTL and DCTL logic family and explain its operation.
   b) Give some applications of logic gates.
   c) Compare the advantages and disadvantages of DTL and Diode logic family.

5. a) Design 3-Input AND and OR gates using diode logic family and RTL logic family and explain their operation.
   b) Design a NOT gate using transistor.
   c) What is Tri-state logic? Design a Tristate TTL inverter and explain its operation.

19. Unit-Wise Quiz Questions And Long Answer Questions

Unit-Wise Quiz Questions

Unit 1: Linear wave shaping

1. A Network which can be mathematically described by linear constant coefficient different equations is called a __.
2. The process whereby the form of a non-sinusoidal signal is altered by transmission through a linear network is called __.
3. Except for the __ signal, no other signal can preserve its form when it is transmitted thorough a linear network.
4. A __ circuit passes low frequency signals and attenuates high frequency signals.
5. The frequency at which the gain is __ of its maximum value is called the cut-off frequency.
6. The lower cut-off frequency of a low pass circuit is __.
7. The upper cut-off frequency of a high pass circuit is __ and is equal to its __ and is given by f_2 = __.
8. At very high frequencies, the capacitor acts almost as a __ and at very low frequencies, the capacitors acts almost as an __.
9. The capacitor __ the dc signal.
10. At the cut-off frequency of the RC circuit, the ___ reactance is equal to the __ and the gain is ___.
11. A signal which maintains the value zero for all times t < 0, and maintains the value V for all times t ≥ 0, is called a __.
12. The expression for the output of a low pass circuit excited by a step input is v_0 = ___.
13. __ is defined as the time taken by the output to rise from 10% to 90% of its final steady-state value for a step input.
14. The rise time of a waveform is directly proportional to the __ and inversely proportional to the __.
15. The rise time t_r of a waveform is given by t_r = ____.
16. In an RC circuit, for a step input, if the initial slope of the output voltage across the capacitor is maintained constant, the output reaches its final value in one ___.
17. For the most applications, the steady-state condition is assumed to be reached at t =____.
18. A pulse may be treated as the sum of a __ followed by a delayed __ of the same amplitude.
19. A pulse shape is preserved when it is passed through a low-pass circuit, if the 3-dB frequency is approximately equal to the __ of the pulse width.
20. A periodic waveform which maintains itself at one constant level V' with respect to ground for a time T_1, and then changes abruptly to another level V" and remains constant at that level for a time T_2, and repeats itself with a period $T=T_1+T_2$ is called a __.
21. Under ___ conditions, the capacitor in the RC circuits charges and discharges to the same level in each cycle. So the shape of the output waveform is fixed.
22. A waveform which is zero for t < 0 and which increases linearly with time for t > 0 is called a ___ or ___.
23. At the end of a ramp input, the difference between the input and the output divided by the input is called the ___.
24. If two stages whose individual rise times are t_{r1} and t_{r2} respectively are cascaded, the rise time of the output waveform will be t_r = ____.
25. A low pass circuit acts as __ if the time constant of the circuit is very large in comparison with the time required for the input signal to make an appreciable change.

26. For an RC low-pass circuit to act as an integrator, it is necessary that RC ___ where T is the period of the sine wave.
27. A __ attenuates all low frequency signals and transmits only signals of high frequency.
28. The lower cut-off frequency of a high pass circuit is ___ and is given by f1 = __.
29. The upper cut-off frequency of a high pass circuit is ___ and hence its bandwidth = ___.
30. The capacitor in the high-pass circuit blocks the dc component of the input from going to the output. Hence it is called a __.
31. The high pass RC circuit is called as __circuit.
32. The process of converting pulses into pips by means of a circuit of very short time constant is called __.
33. A high-pass circuit with a very small time constant is called a __ .
34. The output of a __ circuit excited by a square wave input exhibits a tilt when the time constant of the circuit is high.
35. A high pass circuit acts as a ___ if the time constant of the circuit is very small in comparison with the time required for the input signal to make an appreciable change.
36. The derivative of a step signal is __ at the occurrence of the discontinuity.
37. The derivative of an ideal pulse is a __ followed by a __ each of infinite amplitude and occurring at the points of discontinuity.
38. The derivative of a square wave is a waveform which is uniformly zero except at the points of discontinuity, where __ occur.
39. A high pass circuit is treated as a differentiator if the phase shift between the input and the output is at least __.
40. For an RC high pass circuit to act as a differentiator, it is necessary that wRC < ___.
41. For double differentiation, two __ networks with small time constants are connected in __.
42. __ are almost invariably preferred over __ in analog computer applications.
43. The gain of a __ increases with frequency but the gain of an __ decreases with frequency.
44. An __ is less sensitive to noise voltages than a __ because of its limited bandwidth.
45. If the input waveform changes very rapidly, the amplifier of a __ may get overloaded.
46. It is more convenient to introduce initial conditions in an __ than in a __.
47. Attenuators are ___ used to reduce the amplitude of the input signal.
48. The attenuation of an ideal attenuator is __ of frequency.
49. The attenuator is __ to make the output independent of frequency.
50. In a compensated attenuator, the initial output voltage is determined by the __ and the final output voltage is determined by the ___.
51. For a perfectly compensated attenuator, $v_0(()^+)$ ____ $v_0(\infty)$.
52. For an over compensated attenuator, $v_0(()^+)$ ____ $v_0(\infty)$.
53. For an under compensated attenuator, $v_0(()^+)$ ____ $v_0(\infty)$.
54. If the output of an attenuator is α times the input, the rise time of the output will be __ times the rise time of the input.
55. If C and R of the low-pass and high-pass RC circuits are replaced with R' and L respectively, and if ___ = RC, then all the results of the RC circuits are valid for RL circuits as well.
56. RL circuits are rarely used when a __ time constant is required.
57. The current through an inductor can change instantaneously if __ is applied across it.
58. The voltage across a capacitor can change instantaneously if __ passes through it.
59. An RLC circuit producing as nearly un-damped oscillations as possible is called as __ circuit.
60. A __ circuit may be used to generate a sequence of pulses regularly spaced in time.

Unit 2: Non-Linear wave shaping

1. __ is the process of cutting and removing a part of the waveform.
2. __ circuits are used to select for transmission that part of an arbitrary waveform which lies above or below some particular reference voltage level.
3. Clipping circuits are also called __ or __ limiters, __ selectors or ___.
4. Clipping circuits do not require __ elements.
5. In the simple clipping circuits, the external resistance R is selected to be the __ of the diode forward and reverse resistance, i.e. R = __
6. The use of the diode as a series element has the disadvantage that __

7. The use of the diode as a shunt element has the disadvantage that __
8. A transistor has __ nonlinearity which can be used for clipping purpose.
9. A diode has __ nonlinearity which can be used for clipping purposes.
10. Single ended clipping is also called __ clipping.
11. Double ended clipping is also called __ clipping.
12. In a diode, the nonlinearity occurs when it goes from _- to ___
13. In a transistor, the nonlinearities occur when a) the device goes from __ region to __ region and b) the device goes from __ region to __ region.
14. the emitter coupled clipper is a __ clipper. It is an emitter coupled __ amplifier.
15. A clipping circuit may be used to convert a sine wave into a __ wave.
16. A __ circuit is one, which may be used to mark the instant when an arbitrary waveform attains some particular reference level.
17. Comparators may be __ comparators or __ comparators.
18. __circuits may be used as comparators
19. Clipping circuits are __ comparators.
20. The Schmitt trigger is a __ comparator.
21. Regenerative comparators employ __feedback.
22. In a __ clipper, when the diode is OFF, the output follows the input.
23. In a ___ clipper, when the diode in ON, the output follows the input.
24. Clipping circuits differ from comparators in that __.
25. An example of a non-regenerative comparator is a __.
26. An example of a regenerative comparator is a __
27. The Schmitt trigger comparator generator generates approximately __
28. The blocking oscillator comparator generates ___
29. ___ are used to fix the positive or negative extremity of a periodic waveform at some constant reference level.
30. Under steady-state condition, the clamping circuits restrain the __ of a waveform going beyond VR.
31. Clamping circuits may be __ clamps or __ clamps.
32. When only one diode is used and the voltage change in only one direction is restrained, the circuits are called __ clampers.
33. When two diodes are used and the voltage change in both directions is restrained, the circuits are called __ clamps.
34. The __ circuit is often referred to as dc restorer or dc reinserter.
35. A clamping circuit should be actually called a __.
36. Clamping circuit may be __ clamping circuits or __ clamping circuits.
37. In __ clamping, the negative extremity of the waveform is fixed at the reference level and the entire waveform appears above the reference.
38. In __ clamping, the positive extremity of the waveform is fixed at the reference level and the entire waveform appears below the reference.
39. in __ circuits, the average level of the input plays no role in determining the steady-state output waveform.
40. The difference between the clippers and the clampers is that ___
41. the clamping circuit theorem states that __
42. The precision of operation of the circuit depends on the conditions __ and ___.
43. The response of a clamping circuit is independent of __ of the input signal and is determined only by the ___.
44. Only when __, the tilts in the forward and reverse directions are equal.
45. A __ clamping circuit is one in which R_f and R_s are not negligible and C is not arbitrary large.
46. In __ clamping, a reference voltage source is connected in series with the diode.
47. The tilt in the __ direction is almost always less than the tilt in the __ direction.
48. The clamping circuit theorem for biased clamping is __.
49. In the design of a clamping circuit, the value of R is to be selected such that R= __.
50. It is not possible to clamp the peak of __ pulses precisely.

Unit 3 a: Switching characteristics of Devices

1. The static resistance of a diode is the ratio of _- to __
2. the dynamic resistance of a diode is the ratio of __ to __
3. When a diode is reverse biased, it acts as an __ switch, and when it is forward biased, it acts as a __ switch.
4. In the steady state condition, the current which flows, through the diode is a __ current.
5. The __ current results from the gradient of the minority carriers.
6. At large current amplitudes, the diode behaves as a combination of a __ and __.
7. At intermediate currents, the diode behaves as a __ , ___ and a __.
8. At low currents, the diode is represented by a parallel combination of a __ and __.
9. The forward recovery time t_{fr} is the time difference between the __ and the time when this voltage reaches and remains within __.
10. The __ recovery time of a diode does not usually constitute a problem.
11. The time required for the stored minority charge to become zero after the application of the reverse voltage is called the __.
12. The time which elapses between the instant when the stored minority charge becomes zero and the time when the diode has nominally recovered is called the __.
13. A large signal approximation which often leads to a sufficient accurate engineering solution is the __ representation.
14. Once breakdown occurs, the diode current can be controller only by the resistance of the ___.
15. The breakdown due to thermally generated carriers is called the __ breakdown.
16. The breakdown due to existence of strong electric fields is called the __ breakdown.
17. __ breakdown occurs at voltages below 6 V.
18. The operating voltages in __ breakdown are from several volts to several hundred volts.
19. The breakdown voltage of a Zener diode __with temperature where as the breakdown voltage of an avalanche diode __ with temperature.
20. The breakdown voltage for a particular diode depends on the __ levels in the junction.
21. When a transistor is in saturation, junction voltages are __ but the operating currents are __.
22. When a transistor is in cut off, the junction voltages are ___ but the currents are __.
23. For Ge, Vv = ____ . For Si, Vv = _____. For avalanche diodes, Vv=___.
24. The time required for the current to rise to 10% of its saturation value after the application of the input is called the ___.
25. The time required for the current to rise from 10% to 90% of the saturation value is called the __.
26. The sum of the delay time and the rise time of a transistor is called the __ time.
27. The interval which elapses between the transition of the input waveform and the time when Ic has dropped to 90% of saturation current is called the __.
28. The time required for Ic to fall from 90% to 10% of its saturation level is called the __.
29. The sum of the storage time and the fall time of a transistor is called the __ time.
30. A transistor can operate in three regions : ___, ____ and ___.
31. The hFE of a transistor ___ with temperature.
32. In the cut-off region of a transistor, both the emitter junction and the collector junction are __ and the transistor acts as an ___.
33. In the saturation region, both the emitter junction and the collector junction are ___ and the transistor acts as an ___.
34. In the active region, the emitter junction is __ and the collector junction is ___ and the transistor acts as a ___.
35. The saturation voltage VCE (sat) of a transistor depends not only on the __ but also on the __ and on the type of ___.
36. BVCBO is a characteristic of the ___ alone.
37. BVCEO= ____BVCBO.
38. ___ lies between BVCER and BVCBO.
39. In fast switching circuits, __ must be kept small.
40. In switching circuits, the largest possible output voltage swing is desirable in order to reduce the sensitivity of the switching circuit to __, __, __ and __.
41. ___ transistors and __ transistors give the lowest values for VCE (sat), where as the __ transistors yield the highest.
42. Germanium transistors have __ values for VCE (sat) than those for silicon.

43. At small and moderate currents h_{FE} __ substantially with temperature. At high currents, h_{FE} may become __ to temperature changes.

Unit 3 b : Sampling gates:

1. A __ is basically a transmission circuit which allows an input signal to pass through it during a selected time interval and blocks its passage outside that time interval.
2. The output of a sampling gate is an __ of the input signal during the selected interval and is zero otherwise.
3. A sampling gate is also referred to as a __ or _ or __
4. Sample gate may be _ gates or __ gates
5. The interval of time of transmission of a signal excursion of only one polarity is termed __
6. A sampling gate which can handle the input signal excursion of both the polarities is termed __
7. A sampling gate which can handle the input signal excursion of both the polarities is termed __
8. The gate signal is also referred to as __ or __ or__.
9. __ is an externally impressed signal to select the time interval for transmission.
10. __ is the base voltage in the output on which the input signal is superimposed.
11. The gain of a sampling gate is defined as __
12. The diode sampling gates have the basic disadvantage of __. Also they can be adjusted easily to obtain__
13. the sampling gates are used in a) __ b) __ c) __ d) __ and e) __
14. The disadvantages of the two diode gate are __ , __ , __ and __
15. The advantages of the unidirectional gate are __, __, __ and __
16. The disadvantages of the unidirectional gate are a) __ and b) __
17. A chopper amplifier is used to amplify small signals of the order of __ with very small value of __
18. The chopper is often called a __

Unit 4 a: Multivibrators:

1. A circuit which can oscillate at a number of frequencies is called a __.
2. Basically there are __ types of multivibrators. They are __, __ and __.
3. Resistive coupling is called __ coupling and capacitive coupling is called ___ coupling.
4. A __ multivibrator is the basic memory element.
5. In bistable multivibrators, the coupling elements are __.
6. In monostable multivibrator, the coupling elements are __.
7. In astable multivibrator, the coupling elements are __.
8. A __ circuit is one which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other.
9. A bistable multivibrator is also called __ , __, __, ___ and __.
10. A __ multivibrator is used to perform many digital operations such a counting and storing of binary information. It is also used in the generation and processing of pulse type waveform.
11. A __ of a binary is one in which the currents and voltages satisfy Kirchhoff's laws and are consistent with the device characteristics and in which, in addition, the condition of loop gain being less than unity is satisfied.
12. A __ state of a binary is one in which the device can remain permanently.
13. Loop gain will be __ if either of the two devices is below cut-off or if either device is in saturation.
14. In the stable state, the loop gain is __
15. During transition, the loop gain is __
16. The change in collector voltage resulting from a transition from one state to the other is called __ and is given by ___.
17. __ reduces the output swing.
18. The flip-flop circuit components must be chosen so that under the maximum load which the binary drives, one transistor remains in ___ while the other is __.
19. A constant output swing and a constant base saturation current can be obtained by clamping the collectors to an auxiliary voltage V __ Vcc through the diodes D1 and D2.
20. The diodes used in a bistable multivibrator to maintain a constant output swing are called __ diodes.
21. The interval during which conduction transfers from one transistor to another is called the __.

22. The transition time may be reduced by shunting the coupling resistor with __ called the __
23. Commutating capacitors, also called __ or __ capacitors are used to increase the speed of operation.
24. The smaller allowable interval between triggers is called the __ of the flip-flop.
25. The reciprocal of the resolving time of the flip-flop is the __ at which the binary will respond.
26. The additional time required for the purpose of completing the recharging of capacitors after the transfer of conduction is called the __.
27. The sum of the transition time and the settling time is called the __.
28. If the commutating capacitors are too small, the __ time is increased and if they are too large the ___ time increased.
29. The resolution time of a binary can be improved by a) __ , b) __ and c) ___.
30. The disadvantages of non-saturated binary are a) ___, b) ___ and c) ___.
31. The application of an external signal to induce a transition from one state to the other is called __.
32. The triggering signal which is usually employed is either a ___or a __
33. If the triggering signal is effective in inducing the transition in only on e direction, the triggering is called __.
34. If each successive triggering signal induces the transition regardless of the state in which the binary happens to be, the triggering is called __.
35. __ triggering is used when the binary is to be used as a generator of a gate whose width equals the interval between triggers. It is also used in logic circuitry.
36. __ triggering is used in binary counting circuits.
37. An excellent method for triggering a binary __ on the leading edge of a pulse is to apply the pulse from a high impedance source at the output of the non-conducting device.
38. The __ is called a emitter coupled binary.
39. A Schmitt trigger exhibits hysteresis when loop gain is __.
40. ___ is said to exist if to effect a transition in one direction, we must first pass beyond the voltage at which the reverse transition takes place.
41. Hysteresis in a Schmitt trigger may be eliminated by adjusting the loop gain to ___.
42. The __ is used as an amplitude comparator and as a squaring circuit.
43. for a Schmitt trigger, ___ is defined as the input voltage at which Q1 starts conducting.
44. For a Schmitt trigger, __ is defined as the input voltage at which Q2 resumes conduction.
45. A Schmitt trigger can be used to convert a __ wave into a __ wave.
46. Any slowly varying input waveform can be converted into a square wave by using a __.
47. A Schmitt trigger is also a __ multivibrator.
48. A circuit which ahs got one permanent stable state and one quasi-stable state is called a __.
49. Quasi-stable state means a __ stable state.
50. The monostable multivibrator is also called __, ___, __, ___ or ___.
51. Since a monostable multivibrator generates a rectangular waveform and hence can be used to gate other circuits, it is also called a ___.
52. Since the monostable multivibrator generates a fast transaction at a predetermined time T after input trigger, it is also called a __.
53. A ___ multivibrator is used as a delay circuit and as a gating circuit.
54. ___ triggering is used in monostable multivibrator.
55. The __ multivibrator has two quasi-stable states. It is a free running circuit.
56. The ___ multivibrator is used as a master oscillator.
57. the astable multivibrator can be used as a __ by connecting R_1 and R_2 to an auxiliary supply voltage and varying that voltage.
58. The astable multivibrator is called a __ multivibrator. It is also called a __ generator.
59. the astable multivibrator is used as a __.
60. An __ multivibrator can be used as a voltage to frequency converter.
61. An astable multivibrator is used as a ___ generator.
62. An astable multivibrator can be used as a __ to __ converter.

Unit 4 b: Time base generators:

1. The time base generators may be __ or ___

2. A __ is one that provides an output waveform a portion of which exhibits a linear variation of voltage or current with time.
3. A __ is one that provides an output current waveform a portion of which exhibits a linear variation with time.
4. A __ is one that provides an output voltage waveform a portion of which exhibits a linear variation with time.
5. The most important application of a time-base generator is in __
6. The output of a time base generator is called the __ and the time base generators are called __ .
7. Time-base generators are used in __, __ and __.
8. The time during which the output increases linearly is called the __ and the time required by the sweep voltage to return to the initial value is called the __
9. When __ is zero, we get a saw-tooth or ramp output waveform.
10. The waveforms which increase linearly with time are called __
11. The deviation from linearity is expressed in three ways a) __ b) __ and c) __
12. the ratio of the difference in slope at beginning and end of the sweep to the initial value of slope is called the __
13. The ratio of the maximum difference between the actual sweep and the linear sweep which passes through the beginning and endpoints of the actual sweep to the amplitude of the sweep is called the __
14. The ratio of the difference between the input and the output to the input at the end of the sweep time is called the __
15. If the deviation from linearity is small, then the slope error e_s, the displacement error e_d, and the transmission error e_t are related as __
16. If the restoration time of the sweep is zero, we get a__
17. There are __ methods of generating a sweep.
18. In __ circuit, an operational integrator is used to convert an input step voltage into a ramp.
19. In __ circuit, a pulse input is converted into a ramp.
20. __ may be used to improve the linearity of Miller and bootstrap circuits.
21. In a Miller circuit, the gain A of the __ amplifier should be __
22. In bootstrap circuit, the gain A of the __amplifier should be __
23. A Miller time-base generator produces a __ going sweep, where as a bootstrap time-base generator produces a __ going sweep.
24. A linearly varying current waveform can be generated by applying a constant voltage across __
25. A __ oscillator is a circuit which generates non-sinusoidal oscillations.
26. __ currents are required for magnetic deflection applications.
27. In a simple current time-base generator when the resistance of the coil and the resistance of the transistor in saturation are considered, a __ voltage rather than a __ voltage is applied across the inductor to obtain a linear current.

Unit 5 a: Synchronization and Frequency division:

1. Two or more generators are said to be running __ if all of them arrive at some reference point I the cycle at exactly the same instant of time.
2. Synchronization may be on a __ or may be with __
3. When two generators produce waveforms at different frequencies, it is essential for proper synchronization that the frequency of one generator is an __ of that of the other generator.
4. when generators with equal frequencies run in synchronization , the synchronization is said to be on a __
5. if synchronization is achieved with different frequencies i.e. one frequency being n times the other, then is is termed __
6. Counting circuits are an examples of synchronization with __
7. The circuits in which the timing interval is established through the gradual charging of a capacitor, the timing interval being terminated by the sudden discharge of a capacitor, are called __
8. The multivibrators, time-base generators, blocking oscillators, etc. examples of __.
9. Synchronization with pulse signals is possible only if __
10. In case of synchronization with symmetrical signals, synchronization is possib le for both __ and __
11. In pulse synchronization as well as synchronization with symmetrical signals, __ increases with increasing __

12. Between the instant of occurrence of the pulse which prematurely terminates the cycle and the instant of the change of state of the oscillator there is a certain time delay. This is termed as __
13. The several factors which affect the phase delay give rise to __
14. Any __ controlled negative resistance device can be used as relaxation circuit.

Unit5 b: Realization of logic gates using diodes and transistors:

1. The IC technologies which use bipolar transistors are __ , __ and __.
2. The IC technologies which use unipolar transistors are __ and _ .
3. The __ voltage is defined as that voltage at the input of a gate which causes a change in the state of the output from one logic level to the other.
4. The _- of a gate is defined as the time taken by the pulse to propagate from input to output.
5. The __ of a gate is defined as the power required by the gate to operate with 50% duty cycle at a specified frequency.
6. The __ of a logic gate is defined as the number of inputs that the gate is designed to handle.
7. the __ of a logic gate is defined as the maximum number of similar gates that the output of the gate can drive without impairing its normal operation.
8. The __ is defined as the maximum noise signal that can be added to the input signal of a digital circuit without causing an undesirable change in the circuit output.
9. The __ of a logic gate is defined as the product of the gate propagation delay and the gate power dissipation.
10. A __ is defined as the amount of current needed by an input of another gate of the same logic family.
11. __ is the most popular and most widely used digital IC family.
12. __ is the fastest of the saturated logic families.
13. __ , ___ and __ are the three types of TTL gates.
14. The three possible output states of a tri-state TTL are __, __ and __.
15. __ series is the most suitable for high frequencies.
16. __ is the fastest logic family.
17. __ family has got both the logic levels negative.
18. __ is a non saturated logic.
19. MOS family mostly uses __ devices.
20. The two types of MOSFETs are __ and __
21. The MOS digital IC s use __ MOSFETs exclusively.
22. MOS IC s are ideally suited for __ , __ and __.
23. The __ technology is used to construct small, medium and large scale ICs for a wide variety of applications.
24. __ ICs are used in watches and calculators.
25. __ is ideally suited for applications involving battery power and battery backup power.
26. __ consumes maximum power and __ family consumes the least power.
27. ___ family has the highest fan-out and __ family has the least fan-out.
28. ___ family has the highest noise margin and __ family ahs the least.
29. __ gates are suitable for wired AND operation.
30. __ gates are suitable for wired OR operation.
31. The advantages of totem pole configuration are __ and __
32. __ is most suitable for SSI and MSI. __ can also be used for SSI and MSI.
33. __ is more suitable for LSI and VLSI.
34. __ and __ are suitable for VLSI and ULSI.
35. A __ gate is simply a digitally controller CMOS switch.

Unit-Wise Long Answer Questions

Unit-1
1. What is linear wave shaping? Give some examples.

2. Draw the low pass RC circuit and explain its working.
3. How a Low Pass RC circuit is used in linear wave shaping?
4. Find the lower cut of frequency of a low-pass circuit?
5. Derive an expression for the upper cut-off frequency of a low pass circuit.
6. Derive an expression for the output of low pass circuit excited by a step input.
7. Derive an expression for the rise time of the output of a low-pass circuit excited by a step input
8. Define the rise time and write the expression of it.
9. How does a low-pass circuit reserve the pulse shape?
10. Derive an expression for the output voltage levels under steady state conditions of a low pass circuit excited by a ramp input
11. Derive an expression for the output of a low-pass circuit excited by an exponential input.
12. Explain how a low pass circuit acts as an integrator?
13. Show that low-pass circuit with a large time constant acts as an integrator.
14. Draw the response of a low pass circuit with small, medium and large time constants when input is square wave.
15. Draw the high-pass circuit and explain its working.
16. How a High RC circuit is used in linear wave shaping?
17. Find the upper cut of frequency of a high-pass circuit?
18. Derive an expression for the lower cut-off frequency of a High pass circuit.
19. Derive an expression for the output of high pass circuit excited by a step input.
20. Derive an expression for the rise time of the output of a high-pass circuit excited by a step input
21. How does a high-pass circuit reserve the pulse shape?
22. Derive an expression for the output voltage levels under steady state conditions of a high pass circuit excited by a ramp input
23. Derive an expression for the output of a high-pass circuit excited by an exponential input.
24. Explain how a high pass circuit acts as a differentiator?
25. Draw the response of a High pass circuit with small, medium and large time constants when input is square wave.
26. Why the capacitor in an RC high-pass circuit is called a blocking capacitor?
27. Which type of RC circuit is called a capacitive coupling circuit? Draw the circuit diagram of it.
28. What must be the time constant of a high-pas circuit for the output to be in the form of a tilt for a square wave input?
29. What must be the time constant for a high pass circuit for the output to be in the form of spikes for a square wave input?
30. Derive an expression for the percentage tilt of the output of a high pass circuit with large time constant excited by a symmetrical square wav with zero average value.
31. Why does the output of a high-pass circuit contain zero dc value independent of the dc value of the input?
32. Show that for any periodic input waveform, the average level of the steady-state output waveform of the RC high-pass circuit is always zero independent of the dc value of the input?
33. How can the rate of rise of a pulse be measured by using a differentiator?
34. Draw and explain the response of RL circuit for a step input
35. Draw and explain the response of RLC circuit for a step input
36. Draw and explain the response of ringing circuit for a step input
37. Why are RC circuits commonly used compared to RL circuits?
38. Explain perfect compensation, over compensation and under compensation.
39. Why does a resistive attenuator need to be compensated?

40. Why the initial voltage distribution in an attenuator determined by the capacitors?
41. Why is the final voltage distribution in an attenuator determined by the resistors?
42. If the output of an attenuator is 1/10 of its input, what is the rise time of the output ?
43. What is difference between linear and non-linear waveshaping circuits.
44. Explain condition of RC circuit to work as differentiation.
45. For a long time constant RC high pass circuit with a symmetrical square wave input.
46. find the tilt.
47. Derive the different output equations and draw the output wave forms of a RC low pass circuit for the inputs pulse and square signals.
48. Derive the expression for percentage tilt P of a square wave output of a RC high pass circuit.
49. Explain about simple attenuator circuit and its applications.
50. A 10Hz square wave is fed to an amplifier calculate and plot the waveform under the following conditions, The lower 3-db frequency is   1).0.3Hz   2). 3Hz   3).30Hz
51. Derive the different output equations and draw the output waveforms of a RC high pass circuit for the inputs square and ramp signals.
52. Explain how high pass RC circuit works as a differentiator.
53. Explain about RLC ringing circuit
54. What is a Attenuator? Explain the applications.
55. Explain the operation of RLC circuits.
56. Explain condition of RC circuit to work as differentiator.

Unit-II

1. What are the clipping circuits? Give some examples?
2. How the clipping circuits are used in non-linear wave shaping?
3. Why should the resistance in the clipping circuit be chosen as the geometric mean of the diode forward and reverse resistances?
4. What is the disadvantage of having a diode as a series element in a clipper?
5. What are the other names of clipping circuits?
6. With the help of a neat circuit diagram, explain the working of an emitter-coupled clipper.
7. What is a comparator? How it is used?
8. Distinguish between comparators and clipping circuits.
9. What are the applications of voltage comparators?
10. What is the disadvantage of having a diode as a shunt element in a clipper?
11. What do you mean by a regenerative comparator? Give an example.
12. What do you mean by a non-regenerative comparator? Give an example
13. Draw a circuit to transmit that part of a sine wave which is below +6V and explain its working
14. Draw a circuit to transmit that part of a sine wave which is below -5V and explain its working
15. Draw a circuit to transmit that part of a sine wave which lies between +4V and +8V and explain its working
16. Draw a circuit to transmit that part of a sine wave which lies -3V and +6V and explain its working
17. Draw a circuit to transmit that part of a sine wave which lies between -4V and -7V and explain its working
18. Draw the emitter coupled clipper circuit and explain its operation
19. What do you mean by a two-way clamp and how it differ for one-way clamp?
20. What is clamper? How it is used in Non-linear wave shaping?
21. Why is clamping circuit also called dc inserter?
22. What do you mean by clamping? What the other names of a clamping circuit?
23. What is positive clamping and explain it with suitable circuit.
24. What is negative clamping and explain it with suitable circuit.

25. Derive the relation between the tilts in the forward and reverse directions of the output of a clamping circuit excited by a square-wave input.
26. State and prove the clamping circuit theorem
27. What is the difference between clamping and clamping?
28. What do you mean by biased clamping?
29. What are the limitations of practical clamping circuit?
30. What do you mean by biased clamping?
31. A 100V peak square wave with an average value of 0V and a period of 20ms is to be negatively clamped at 25V. Draw the input and output waveforms and necessary circuit diagram.
32. Draw the four diode Clipping circuits using the diode appears as a shunt and series element
33. Draw a circuit diagram of double-diode clipper which limits at two independent levels and explain it with its transfer characteristics.
34. What are the different schemes for temperature compensation of clipper? Explain them briefly.
35. Draw the circuit diagram of a diode differentiator comparator and explain its working
36. What are the applications of voltage comparators?
37. What types of difficulties are there in practical clamping circuit? How to overcome these.
38. State and prove clamping circuit theorem.
39. Discuss the effect of diode characteristics on clamping circuits.
40. Draw the diode differentiator comparator circuit and explain the operation of it when ramp input signal is applied.
41. Explain the operation of two level slicer.
42. Explain the operation of transistor clippers with neat sketches
43. Explain the operation of positive peak clamper with output waveforms.
44. Classify different types of clipper circuits. give their circuits and explain the operation with transfer characteristics.
45. For 2-level clipper with peak input 100V and forward bias reference voltage 75V and reverse bias diode reference voltage 50V assume ideal diodes. Sketch the output voltage
46. What is synchronized clamping .
47. Explain the operation of diode comparator.
48. Compare series diode clipper and shunt diode clipper.
49. Write short notes on practical clamping circuits.
50. Draw the diode differentiator comparator circuit and explain the operation of it when ramp input signal is applied.

Unit-III a
1. Name the devices that can be used as switches.
2. Define a storage time and transition time of a diode
3. Explain how a diode act as a switch?
4. Define a diode forward recovery time and reverse recovery time.
5. Explain how a transistor acts as a switch?
6. When does a transistor act as a closed switch and an open switch?
7. Define a rise time and fall time of a transistor switch.
8. What is delay time and storage time of a transistor? What factors does contribute to it?
9. Write a short notes on a diode switching times.
10. Write a short notes on a transistor switching times.
11. A rectangular pulse of voltage is applied to the base of a transistor driving it from cut-off to saturation. Discuss the various times involved in the switching process.
12. How are the junctions of a transistor biased for cut-ff, active and saturation regions of operations?
13. Prove that the total turn-on time of a transistor is the sum of the delay time and the rise time.

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14. Explain how a transistor acts as a closed switch in saturation region?
15. Explain how a transistor acts as a open switch in cut off region?
16. Draw and Explain the piece-wise linear characteristics of a diode.
17. Explain briefly about the breakdown voltages of a transistor.
18. Define collector to emitter breakdown voltage and Write its equation in terms of hFE.
19. For an npn Ge transistor(n=6 , hFE=50) and BVCBO is about 20V /Find the collector to emitter breakdown voltage?
20. Explain the design procedure of Transistor Switch.
21. For a CE transistor circuit with VCC = 15V, Rc=1.5K ohms, calculate the transistor power dissipation at open and closed positions.
22. Explain the variation of saturation parameters of transistor with temperature?
23. Explain the variation of VBE(sat) and VCE(sat) of transistor with temperature.
24. For a common emitter circuit, Vcc = 15V , RC =1.5Kohms and IB=0.3mA. Determine the value of hFE(min) for saturation to occur.
25. Sketch the typical transistor common-emitter characteristics. Identify the various regions of the characteristics and show how VCE(sat) differs with different load resistances.
26. A common emitter circuit has Vcc=20V and a collector resistor which can be either 20Konms to 2Kohms. Calculate the minimum level of base current to achieve saturation in each case.
27. Derive the expression for fall time of transistor switch.
28. Derive the expression for rise time of transistor switch.
29. Draw the collector waveform of transistor switch and indicate all the time intervals.
30. What the factors that contribute the delay time of transistor switch?
31. Define the storage time constant and how it is related to storage time of transistor switch?
32. Why a charge compensating capacitor is used in diode switch?
33. Define storage and transition times of a diode.
34. Explain breakdown voltage consideration of transistor.
35. Draw the piece-wise linear diode characteristics and explain how it works as s switch.
36. Explain the piecewise linear diode characteristics and explain breakdown voltage consideration of transistor characteristics.
37. Explain the BJT operation in active, cut off and saturation region and variation of it with temperature.
38. 6.Define the following terms a)rise time b)Fall time c)Storage time   d)Delay time e)reverse recovery time.
39. Explain the operation of transistor as switch with its switching times.
40. Explain in detail the junction diode with its switching times

Unit-III b

1. What is a sampling gate? What are the applications of it?
2. Why are sampling gates are called linear gates? what are the other names of it?
3. How do sampling gates differ from logic gates? Draw the circuit diagram of unidirectional sampling gate.
4. Draw the circuit diagram of unidirectional sampling gate and explain its working
5. Draw the circuit diagram of bidirectional sampling gate and explain its working.
6. What is pedestal? What are the effects of it in sampling gates?
7. Compare unidirectional and bidirectional sampling gates.
8. What are the draw backs of two-diode gates and how to overcome it?
9. With help of a neat diagram, explain the working of bidirectional gates using transistors.
10. With help of a neat diagram, explain the working of a two-diode sampling gate.
11. What is the gain of a gate? Derive expression for gain of a two-diode sampling gate.
12. Derive the expression for Vcmin of a two-diode sampling gate.

13. Derive the expression for Vnmin of a two-diode sampling gate.
14. With the help of a neat diagram, explain the working of a four-diode gate.
15. Draw and explain the circuit diagram of a six-diode gate
16. What are the advantages and disadvantages of the unidirectional diode gate?
17. Explain the basic principle of sampling gates.
18. Draw the circuit diagram of the unidirectional diode gate for more than on input signal and explain its working
19. Explain how the loading of the control signal is reduced when the number of inputs increases?
20. Draw the circuit diagram of a unidirectional gate which delivers an output only at a coincidence of a number of control voltages and explain its working.
21. Explain how to cancel a pedestal in a sampling gate with suitable circuit diagram.
22. What are the drawbacks of a circuit which is used to eliminate a pedestal?
23. Draw the bidirectional diode sampling gate in the form of a bridge network and explain its working.
24. Write the expressions for Vcmin and Vnmin for a four-diode sample gate.
25. For the four diode gate with a divider resistance R=100Ω, VS=25V, Rf=20 R = RC = 200KΩ. Find VCmin and Vnmin?
26. Explain how a sampling gate is used in chopper amplifier?
27. Explain how a sampling gate is used in Sampling Scope?
28. What is the application a chopper amplifier? How a sampling diode is used in it?
29. What are the applications of sampling gates? Explain any one of it with a neat circuit diagram.
30. Derive the expression for Vcmin of a bidirectional sampling gate.
31. What is sampling gate & explain how it differ from logic gate.
32. Why sampling gates are called selection circuits ?
33. With the help of neat diagram explain the working of two diode sampling gate.
34. Compare the unidirectional & bi-directional sampling gate
35. Write the differences between series sampling gate & shunt sampling gate.
36. Derive expressions for gate & minimum control voltage of a bidirectional 2-diode sampling gate
37. What is pedestal. How it effects the output of sampling gate.
38. What are the applications of sampling gate.
39. Describe the working of a 4-Diode sampling gate with necessary diagram & equationsExplain the working of bi-directional gate using transistors.

Unit-IV a
1.   What is a Bistable circuit? What are the other names of a bistable multivibrator?
2.   What are the applications of a bistable multivibrator?
3.   What do you mean by the term 'loop gain'?
4.   Explain how a constant output swing can be obtained in a binary?
5.   What are the commutating capacitors? Why these are used in binary?
6.   What do you mean by transition time? How it can be reduced?
7.   Define the resolving time, settling time and resolution time.
8.   What are the methods of improving the resolution of a binary?
9.   Explain the working of non-saturated binary.
10. What is a non saturated binary? What are the advantages and disadvantages of it?
11. Compare the saturated and non-saturated binary.
12. What is unsymmetrical triggering ? where is it used?
13. What is necessity of triggering ? What are the different types of triggering?
14. Compare symmetrical and unsymmetrical triggering.
15. Explain any one method of unsymmetrical triggering of a binary?

16.   Explain any one method of symmetrical triggering of a binary?
17.   What are the advantages and disadvantages of a direct-connected binary?
18.   What is a Schmitt trigger? What are the applications of it.
19.   With the help of neat circuit diagram and waveforms, explain the working of a Schmitt trigger.
20.   Define the terms upper triggering point and lower triggering point with the help of waveforms
21.   How can hysteresis be eliminated in a Schmitt trigger?
22.   Define the terms: stable state, quasi stable state, dc coupling and ac coupling
23.   Compare ac coupling and dc coupling in Multivibrator.
24.   Define the terms UTP and LTP of a Schmitt trigger and explain how these are varied?
25.   Why is monostable multivibrator also called a gating circuit and give its applications.
26.   Why is monostable multivibrator also called a delay circuit and draw its circuit diagram.
27.   With the help of neat circuit diagram explain the working of a collector coupled Monostable multivibrator.
28.   Derive an expression for the gate width of monostable multivibrator.
29.   Derive the expression for the gate width of a monostable multivibrator considering the effect of reverse saturation current.
30.   What type of triggering is used in a monostable multivibrator? Draw the circuit of it.
31.   With the help of a neat circuit diagram, explain the working of an emitter coupled monostable multivibrator.
32.   With the help of a neat circuit diagram explain the working of an astable multivibrator
33.   Draw and explain the base and collector waveforms of an Astable multivibrator.
34.   Draw and explain the base and collector waveforms of a monostable multivibrator.
35.   Draw and explain the base and collector waveforms of an bistable multivibrator.
36.   Derive an expression for the frequency of oscillations of an astable multivibrator.
37.   Show that an astable multivibrator can be used as a voltage to frequency converter.
38.   What is blocked condition in an astable multivibrator? How to overcome it?
39.   Draw the circuit of the gated astable multivibrator with vertical edges.
40.   Draw the circuit of the gated astable multivibrator and explain how it works?
41.   Draw the circuit of the astable multivibrator which does not block.
42.   Discuss the Self Starting feature in Stable multivibrator?
43.   Derive the expression for the period of oscillations of astable multivibrator.
44.   Draw the circuit of a seld-biased transistor binary and develop the design steps of analysis.
45.   Discuss the symmetrical and asymmetrical triggering methods with the relevant circuits.
46.   Explain the operation of bistable multivibrator in fixed bias with neat sketches.
47.   Vcc=12V,Vbb=-8V,R1=10KΩ,R2=50KΩ,Rc=2.2KΩ The transistors are silicon with hfe=30.calculte stable state currents and voltage when all junction voltages are neglected
48.   Explain the operation of astable multivibrator with neat sketches
49.   Explain the operation of Schmitt trigger circuit.
50.   Why collector catching diodes are used in multivibrators?
51.   write the applications bistable and monostable multivibrators
52.   Explain how hysteresis can be eliminated in a schimitt trigger.
53.   Draw the various wave shapes of the astable multivibrator.

Unit-IV b

1.   What is a voltage time base generator and compare it with a current time-base generator.
2.   What is a current time-base generator and compare it with linear time-base generator.
3.   Compare voltage, current and linear time-base generators.
4.   Why are time-base generators called a sweep generators and what are the applications of it?
5.   Define the sweep time and restoration time for time-base generators.
6.   Define the terms slope error, displacement error and transmission error.

7. How the slope error, displacement error and transmission error are related for an exponential sweep circuit?
8. Derive the relation between slope error, displacement error and transmission error.
9. Explain briefly the methods of generating a time-base waveform?
10. What are the methods of generating a time-base waveform? Explain any one of it.
11. With the help of a neat circuit diagram explain the working of a simple transistor current time-base generator.
12. with the help of a neat circuit diagram, explain the working of a transistor constant current sweep circuit.
13. Explain the basic principles of Miller and Bootstrap time-base generators.
14. Compare Miller and Bootstrap time-base generators.
15. With the help of a neat circuit diagram, explain the working of a transistor Miller time base generator.
16. With the help of a neat circuit diagram and waveforms, explain the working of a transistor bootstrap time base generator.
17. How are linearly varying current waveforms generated?
18. With the help of a neat circuit diagram, explain the working of a simple current sweep.
19. What type of voltage input is required to obtain a linear current sweep? Draw the circuit diagram of any type of linear current sweep generator.
20. How is linearity corrected through adjustment of the driving waveform for a current time-base generator.
21. With the help of a neat circuit diagram, explain the working of a transistor current time base generator.
22. Prove that when restoration time is zero, we get a saw-tooth output waveform.
23. Explain how the deviation from linearity is expressed.
24. Prove that when the deviation from linearity is small then the slope error is twice the transmission error.
25. Prove that when the deviation from linearity is small then the slope error is eight times than the displacement error.
26. Prove that when the deviation from linearity is small then the transmission error is four times than the displacement error.
27. Why an operational integrator is used in Miller circuit?
28. What type of currents are required for magnetic deflection applications?
29. How the linearity is improved in Miller and bootstrap circuits?
30. Compare the Miller and Bootstrap circuits.
31. How a linearly varying current waveform can be generated from a linearly varying voltage waveform?
32. Why time base generators are called sweep circuits.
33. What is a linear base generator? Give its applications.
34. Derive the relation between the slope , transmission and displacement errors.
35. What is a time base generator?
36. Design the terms
    i.   Slope error ii. Displacement error iiii. Transmission error of the time base signal
            and derive the expression for the relative errors.
37. Explain the basic principle of working of miller & boot strap time base generators with the neat Sketches
38. What are the methods of generating a time base waveform &explain each method.
39. Write the difference between voltage & current time base generator
40. Write the applications of time base generator & explain.
41. Explain the principle of working of exponential sweep circuit with a neat circuit diagram & also derive the equations for slope, transmission and displacement error.
42. Bring out the necessity and importance of current sweep circuits. List out its applications.
43. What are the techniques used to improve the linearity of current sweeps. Illustrate with examples.

Unit-V a

1. What is synchronization? Why it is necessary in waveform generators?

2. Explain the principle of synchronization.
3. What is the one-to one basis synchronization?
4. Explain the synchronization with frequency division.
5. Give some examples of synchronization with frequency division.
6. What is a relaxation circuit? Give a few examples of it.
7. How the negative-resistance devices used as relaxation oscillators?
8. With the help of a neat circuit diagram explain synchronization of a sweep generator with plus signals.
9. How does the synch signal affect the frequency of operation of the sweep generator?
10. What is the condition to be met for pulse synchronization?
11. With the help of a neat waveforms, explain frequency division with respect to a sweep circuit.
12. With the help of a circuit diagram and waveforms, explain frequency division by an astable blocking oscillator.
13. With the help of a circuit diagram , explain frequency division by an astable multivibrator.
14. Draw and explain the waveforms of a frequency division by an astable multivibrator.
15. what is the condition to be met form pulse synchronization of monostable circuits?
16. Explain the use of monostable relaxation device as a divider.
17. Explain the synchronization of a sweep circuit with symmetrical signals.
18. With the help of neat waveforms, explain sine wave frequency division with a sweep circuit.
19. Compare sine-wave synchronization with pulse synchronization.
20. How many types of synchronization methods are available? Explain them briefly.
21. Explain how to achieve a synchronization in the generators operate at different frequencies?
22. Explain how synchronization is achieved in counting circuits?
23. Explain the mechanism of synchronization in relaxation devices.
24. What type synchronization is used when the interval between pulses is less than or equal to the natural period of the wave form generator? Explain it briefly.
25. Explain the synchronization with symmetrical signals.
26. Prove that the range of synchronization increases with increasing sync signal amplitude.
27. Draw and explain a block diagram and waveforms for a divider without phase jitter.
28. What is phase jitter? How to reduce it in frequency division?
29. What are the various factors that affect on phase delay?
30. Explain a method of frequency division by a factor of 2 in a sweep generator.
31. Explain how the synchronization of a generator will depend on the interval between pulses and natural period?
32. What do you mean by synchronization.
33. What is the condition to be met for pulse synchronization.
34. What is relaxation oscillator? Name some negative devices used as relaxation oscillators and give its applications?
35. Explain the methods of obtaining balanced conditions in a bi-directional diode gate.
36. With the help of neat diagram explain frequency synchronization for Astable multivibrator.
37. Explain the factors which influence the stability of relaxation divider with the help of neat waveform.
38. What is synchronization & why it is necessary in waveform generators.
39. Explain how monostable multivibrator is used as frequency divider.
40. Explain the terms phase delay & Phase jitter
41. Compare sin wave synchronization & pulse synchronization.
42. Explain with neat diagram the synchronization of sweep circuit with symmetrical signal.
43. Explain the methods for achieving division without phase jitter.

1. Draw a diode OR circuit for negative logic and explain how it works. 2.
2. Explain how a OR circuit acts a buffer circuit?
3. Draw a diode OR circuit for positive logic and explain how it works.
4. What is positive logic and negative logic in digital systems?
5. Explain the influence of shunt capacitance on the output pulse of OR gate.
6. Explain the influence of diode internal capacitance on the output pulse of OR gate.
7. Explain how a bit is recognized in a dynamic logic system?
8. Explain the operation of OR gate with the help of truth table
9. Explain the operation of AND gate with the help of truth table
10. Draw a diode AND circuit for negative logic and explain how it works.
11. Draw a diode AND circuit for positive logic and explain its works.
12. Compare the operation of AND gate in positive and negative logics.
13. Compare the operation of OR gate in positive and negative logics.
14. What is logical noise? How to reduce it in AND gate?
15. Explain the purpose of a clamping diode in AND gate?
16. The following are the design parameters for a diode logic AND circuit in positive logic : source resistance RS, diode forward resistance Rf , diode break-point voltage Vγ and m number of inputs are at V(1) out of total n inputs. Find the expression for the output?
17. Why direct coupling is preferable to capacitive coupling in diode logics ?
18. Draw the Inverter for transistor logic and explain its working.
19. How to improve the transient response of the inverter?
20. What are the various transistor limitations in designing transistor inverters?
21. Draw the circuit diagram for a positive logic AND circuit in diode transistor logic and explain its working
22. What is LLL? How it is related to DTL logic?
23. Draw the circuit diagram of a positive NAND gate in DTL logic and explain its working.
24. How a NOR gate can be constructed using OR and NOT gates in DTL logic?
25. What are the basic gates can be constructed in DTL logic and write its truth tables?
26. Explain how a positive logic can be converted into a negative logic?
27. Draw an inverter for negative logic and explain the working of it with truth table
28. How the rise time is improved in AND gate using diodes?
29. Why a AND gate is called coincidence circuit?
30. Why a OR gate is called mixing gate?
31. Draw and explain the circuit diagram of a diode AND gate for positive logic.
32. With the help of a circuit diagram explain the purpose of clamping diode in a positive diode AND gate.
33. Compare different logic families.
34. Draw the transistor and diode logic NAND gate.
35. Draw the OR gate using diodes and resistors. Verify its truth table.
36. Define fan-in and fan-out.
37. Draw a TTL 2-i/p NAND gate and explain its operation
38. Give some applications of logic gates.
39. Define the following parameters a) Fan-in b) Fan-out c) Noise margin
   Propagation delay e) Power dissipation   f) Speed power product Adfa
40. Draw a 2-i/p NOR gate using ECL logic family
41. Explain about positive & negative pulse logic systems
42. Compare RTL and DTL logic families in terms of fan-out , Propagation delay,Power dissipation & noise immunity
43. Draw a 3-input AND gate using diodes and transistors & explain it with truth table.
44. Draw and explain the circuit diagram of integrated positive 2-i/p RTL NOR gate
45. Draw and explain the circuit diagram of integrated positive 2-i/p DTL NAND gate

46. What is wired logic? Give some applications.

20. Tutorial problems

UNIT-I

1. A step input of 10V when applied to the Low Pass RC circuit produces the output with a Rise time of 200 micro sec. Calculate the upper 3dB frequency of the circuit if the circuit uses a capacitor of 0.47 micro F, Determine the value of the resistance.

2. Derive expression for % tilt .

3. A step generator of 50ohms impedance applies a 10V step of 2.2 nsec rise time to a series combination of a capacitor C and a resistor R=50ohm. A pulse of amplitude 1V appears across R. Find the value of the capacitance C.

4. A symmetrical square wave whose peak-to-peak amplitude is 2V and whose average value is zero is applied to RC integrating circuit. The time constant is half the period of the square wave. Find the peak-to-peak value of output voltage.

5.What is the ratio of the rise time of the three sections in cascade to the rise time of single section of low pass circuit.

UNIT-2

1.Design a diode clamper circuit to clamp the positive peaks of the input signal at zero level. The frequency of the input signal is 500Hz.

2.The input to the diode differentiator comparator is ramp whose slope is 0.1V per second. Reference level is VR=0V. Amplifier gain 10 and $\tau_1 = \tau_2 =100$ micro second. What is peak to peak value of output.

3.Designa diode clamper to resistor a d.c. level of +3 volts to an input signal of peak value of 10volts. Assume drop across diode is 0.6 volts.

4.Draw the transfer characteristics of series clippers.

5. Draw the transfer characteristics of shunt clippers.

UNIT-3 a

1.Draw and explain transistor switching times.

2. Draw and explain diode switching tines.

3.Derive the expression for collector to emitter voltage with open circuit base.

4.Derive the expression for collector to emitter voltage with base is short circuited to emitter.

5. Derive the expression for collector to emitter voltage with RB in base in series with V_{BB}.

UNIT-3 b

1.Draw the circuit diagram of unidirectional diode gate.

2.Draw the block diagram of sampling scope.

3. Draw the sampling gate using six-diodes.

4. Draw the sampling gate using Transistors.

5. For the four diode gate $R_L=R_C= 100K\Omega$ and $R_2=2K\Omega$, $R_f=50\Omega$ for $V_s=25V$, compute gain(A), V_{min} and $V_{n(min)}$. Compute $V_{n(min)=}V_{min}$.

UNIT-4 a

1.Design a monostable multivibrator circuit that produces a pulse width of 10ms. Assume hfe= 30, $V_{CE(sat)}=0.3V$, $V_{BE(sat)=}0.7V$, $I_{c(sat)}=5mA$, $V_{cc}=6V$, $V_{BB}= -1.5V$.

2. Silicon transistors with $h_{fe(min)} = 30$ are available. If $V_{cc}= 12V$ and $V_{BB}= 6V$, design a fixed bias bistable multivibrator.

3.Consider the Schmitt trigger With germanium transistor having hfe= 20. The circuit parameters are $V_{CC}=15V$, $R_S=2K\Omega$, $R_{C1} = 1K\Omega$, $R_{C2}= 1K\Omega$, $R_1= 3K\Omega$, $R_2= 10K\Omega$ and $R_e= 6K\Omega$. Calculate LTP and UTP.

4. If a astable multivibrator has $C_1=C_2=1000pF$ and $R_1=R_2=K\Omega$. Calculate the frequency of oscillation.

5.Design a self-biased bistable multivibrator using silicon transistor given $V_{CC}=6$ V and $h_{fe(min)} =30$. Assume appropriate junction voltages for your design.

UNIT-4 b

1.A transistor bootstrap ramp generator is to produce a 15V , 5ms output to a $2K\Omega$ load resistor. The ramp is to be linear within 2 %. Design a suitable circuit using $V_{cc} =22$ V, $-V_{EE} =-22V$ and transistor with $h_{fe(min)} =25$. The input pulse has an amplitude of -5V, pulse width = 5ms and space width =2.5 ms.

2. In UJT sweep circuit $V_{BB} = 20V$, $V_{YY}=50V$, R= $5K\Omega$, $R_{B1}=R_{B2}= 0\Omega$ and C=0.01μF. The UJT fires when $V_1=$ 10.6V and goes to OFF state when $V_c= 2.8V$. Find the

i) The amplitude of sweep signal.   ii) The slope and displacement iii)The duration of the sweep

iv) the recovery time.

3 In a simple UJT circuit, the resistance and capacitance are 100Kohms and 0.4 microfarad. The ratio of peak voltage to supply voltage is 0.57. Find the frequency of the sweep circuit.

4.Derive the expression for slope error and sweep speed for Miller circuit.

5.Calculate the frequency of the sawtooth waveform generated by a UJT oscillator, if R=100KΩ, C=0.01μF and η = 0.8.

UNIT-5 a

1.A UJT sweep operates with $V_v=3V$, $V_p=16V$ and $\eta =0.5$. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1KHz, over what range of synch signal frequency will the sweep remain in 1:1 synchronism with the synch signal?

2.Draw the circuit diagram of an astable multivibrator to obtain frequency division by 6.

3.Draw and explain a sinusoidal divider using regeneration and modulation.

4.A free running oscillator has sweep amplitude of 100V and a period of 1msec synchronizing pulses are applied to the device such that breakdown voltage is lowered by 50V at each pulse. The synchronizing pulse frequency is 4KHz. What is the amplitude and frequency of synchronized oscillator waveform?

UNIT-5 b

1.Draw a TTL NAND gate and explain its operation.

2. Draw the three input OR gate.

3. Draw a NOR gate using DTL logic.

4. Draw NOR gate using RTL logic.

5. Draw a NOR gate ECL logic.

21.Known gaps, if any inclusion of the same in lecture schedule

a. Realization of logic gates using CMOS circuits

22.Discussion topics, if any

1. Applications of Diode

2.Switching characteristics of Diode ,Transistors and SCR

3.Applications of multivibrators

4. Applications of Sweep circuits

5. Applications of Synchronization techniques

6. Logic families and its comparison

23.References, Journals, websites and E-links if any

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B&focus=viewport&dq=Pulse,+Digital+and+Switching+Waveforms+-
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P.; Moritz, C.A. Nanoscale Architectures, 2007. NANOSARCH 2007. IEEE International

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3.**Stability analysis of a digitally based HVDC firing-pulse synchronization control**

Larsen, E.V.; Clark, K.; Lorden, D.J.

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24.Quality Control Sheets

a. Course end survey
b. Teaching Evaluation

25.Students list

ECE 2-2 A

SlNo	AdmnNo	StudentName
Class / Section: ECE 2-2 A		
1	14R11A0401	ADITYA B
2	14R11A0402	ADULLA JANARDHAN REDDY
3	14R11A0403	ANDE HEMANTH REDDY
4	14R11A0404	ANKATI NAVYA
5	14R11A0405	ASHFAQ AZIZ AHMED
6	14R11A0406	BANDI SANDHYA
7	14R11A0407	BASWARAJ SHASHANK YADAV
8	14R11A0408	BITLA SRIKANTH REDDY
9	14R11A0409	BUDDANA DHARANI KUMAR
10	14R11A0410	CHEBARTHI RAMYA GAYATHRI
11	14R11A0411	CHETLAPALLI NAGA SAI SUSHMITHA
12	14R11A0412	DASARI DHAMODHAR REDDY
13	14R11A0413	G AYESHA SULTANA
14	14R11A0414	G MADHURI
15	14R11A0415	G RISHI RAJ
16	14R11A0416	G VAMSHI KRISHNA
17	14R11A0417	G VENKATESH YADAV
18	14R11A0418	GONDA RISHIKA
19	14R11A0419	GUDE GOPI
20	14R11A0420	JAGGANNAGARI MANOJKUMAR REDDY
21	14R11A0421	JAGGARI SRINIJA REDDY
22	14R11A0422	JALAGAM NANDITHA
23	14R11A0423	JAMMIKUNTLA SHIVA CHARAN
24	14R11A0424	JATAPROLU LAKSHMI SOWMIKA
25	14R11A0425	JEKSANI SHREYA
26	14R11A0426	K VIJAY KUMAR
27	14R11A0427	KAALISETTY KRISHNA CHAITANYA
28	14R11A0428	KAKARLA MOUNICA
29	14R11A0429	KARRE PRIYANKA
30	14R11A0430	KL N SATYANARAYANA MURTHY
31	14R11A0431	KONDA KRITISH KUMAR
32	14R11A0432	KOPPULA RAHUL
33	14R11A0433	KURUGANTI RUNI TANISHKA SHARMA
34	14R11A0434	L THRILOK
35	14R11A0435	MANDULA SANTOSHINI
36	14R11A0436	MATLA PRINCE TITUS
37	14R11A0437	NARSETTI SAIPRAVALIKA
38	14R11A0438	NIKITHA RAGI

39	14R11A0439	P VIJAYA ADITYA VARMA
40	14R11A0440	PASHAM VIKRAM REDDY
41	14R11A0441	PELLURI KARAN KUMAR
42	14R11A0442	PERURI CHANDANA
43	14R11A0443	PODUGU SRUJANA DEVI
44	14R11A0445	RAJU PAVANA KUMARI
45	14R11A0446	RAMIDI NITHYA
46	14R11A0447	RAMOJI RAJESH
47	14R11A0448	S ALEKHYA
48	14R11A0449	SARANGA SAI KIRAN
49	14R11A0450	SHAIK SAMEER ALI
50	14R11A0451	SOUMYA MISHRA
51	14R11A0452	SRIRAMOJU MANASA
52	14R11A0453	THAMADA ARUN KUMAR
53	14R11A0454	T S SANTHOSH KUMAR
54	14R11A0455	V BAL RAJ
55	14R11A0456	V POOJA
56	14R11A0457	V SRIVATS VISHWAMBER
57	14R11A0458	V VISHNU VARDHAN REDDY
58	14R11A0459	VENNAMANENI VAMSI KRISHNA
59	14R11A0460	YERASI TEJASRI
60	15R15A0401	RAMIDI SANDEEP REDDY
61	15R15A0402	ODDARAPU HARISHBABU
62	15R15A0403	KOLUKURI BHARGAVI
63	15R15A0404	ADEPU MOUNIKA
64	15R15A0405	AVANCHA PRAVALIKA
65	15R15A0406	NELLUTLA VISHAL CHAITANYA
66	15R15A0407	VEMULA JAMEEMA
Total: 66 Males: 36 Females: 30		

Class / Section: ECE 2-2 B		
1	14R11A0461	ADDAKULA SURESH
2	14R11A0462	AGARTI MADHU VIVEKA
3	14R11A0463	AKULA SAI KIRAN
4	14R11A0464	ANUMULA SNIGDHA
5	14R11A0465	B DIVYA
6	14R11A0466	B MANOHAR
7	14R11A0467	BANDARI MAMATHA
8	14R11A0468	BINGI DIVYA SUDHA RANI
9	14R11A0469	BIRE BHAVYA
10	14R11A0470	CH SAI BHARGAVI

11	14R11A0471	CHAVALI SUMA SIREESHA
12	14R11A0472	CHELLABOINA SHIVA KUMAR
13	14R11A0473	CHETTY AKHIL CHAND
14	14R11A0474	CHINTAPALLI MADHAV REDDY
15	14R11A0475	CHIVUKULA VENKATA SUBRAMANYA PRASAN
16	14R11A0476	D NAGA SUMANVITHA
17	14R11A0477	D VAMSI
18	14R11A0478	DHARMENDER KEERTHI
19	14R11A0479	EADARA NAGA SIRISHA
20	14R11A0480	ERANKI SAI UDAYASRI ALAKANANDA
21	14R11A0481	GANGA STEPHEN RAVI KUMAR
22	14R11A0482	GUNDAM SHRUTHI
23	14R11A0483	GUNDREVULA SAMEERA
24	14R11A0484	K NAGA REKHA
25	14R11A0485	KANDADI VARSHA
26	14R11A0486	KURELLI SAI VINEETH KUMAR GOUD
27	14R11A0487	MADDIKUNTA SOMA SHEKAR REDDY
28	14R11A0488	MAMILLA SAI NISHMA
29	14R11A0489	MARELLA NAGA LASYA PRIYA
30	14R11A0490	MARKU VENKATESH
31	14R11A0491	MOHAMED KHALEEL
32	14R11A0492	MOHAMMED WASEEM AKRAM
33	14R11A0493	MOTURI DIVYA
34	14R11A0494	MUDIUM KOUSHIKA
35	14R11A0495	MYLAPALLI RAMBABU
36	14R11A0496	NAGU MOUNIKA
37	14R11A0497	NEELAM SNEHANJALI
38	14R11A0498	NIDAMANURI VENKATA VAMSI KRISHNA
39	14R11A0499	NIKHIL KUMAR N
40	14R11A04A0	ORUGANTI HARSHINI
41	14R11A04A1	PARAMKUSAM NIHARIKA
42	14R11A04A2	PASAM ABHIGNA
43	14R11A04A3	PATI VANDANA
44	14R11A04A4	PODISHETTY MANOGNA
45	14R11A04A5	PONAKA SREEVARDHAN REDDY
46	14R11A04A6	R NAVSHETHA
47	14R11A04A7	R PRANAY KUMAR
48	14R11A04A8	RAMIDI ROJA
49	14R11A04A9	RUDRA VAMSHI
50	14R11A04B0	S SHARAD KUMAR
51	14R11A04B1	SAGGU SOWMYA

52	14R11A04B2	TADELA SARWANI
53	14R11A04B3	THOTA SAI BHUVAN
54	14R11A04B4	VALLAPU HARIKRISHNA
55	14R11A04B5	VECHA PAVAN KUMAR
56	14R11A04B6	Y SAI VISHWANATH
57	15R15A0408	ERUKALA NIKITHA
58	15R15A0409	PUNGANUR JAYACHANDRA BHARATHWAJ
59	15R15A0410	GALIPALLY BHARGAVA
60	15R15A0411	PADMA ARUNRAJ
61	15R15A0412	JAMALAPURAM NAVEEN
62	15R15A0413	MACHANNI BALAKRISHNA YADAV
63	15R15A0414	ANABOINA MAHENDER
64	15R15A0415	ANABOINA SHIVA SAI
65	15R15A0416	VEMULA VINITHA
66	15R15A0417	CHEVU NAGESH
Total: 66 Males: 34 Females: 32		

Class / Section: ECE 2-2 C		
1	14R11A04B9	ANAMALI REETHIKA
2	14R11A04C0	ARUMILLI LEKYA
3	14R11A04C1	ARUMUGAM ASHWINI
4	14R11A04C2	BASAVARAJU MEGHANA
5	14R11A04C3	BEERAM TEJASRI REDDY
6	14R11A04C4	BHARAT SAKETH
7	14R11A04C5	BOMMANA HARIKADEVI
8	14R11A04C6	BYRAGONI ROJA
9	14R11A04C7	CANDHI SHASHI REKHA
10	14R11A04C8	CH RENUKA
11	14R11A04C9	CHAGANTI MOUNICA
12	14R11A04D0	CHITTARLA LOKESH GOUD
13	14R11A04D1	D LAVANYA
14	14R11A04D2	D MANIKANTA
15	14R11A04D3	DASARI VENKATA NAGA SAISH
16	14R11A04D4	DODDA MANOJ
17	14R11A04D5	E RAHUL CHOWDHARY
18	14R11A04D6	GOWRISHETTY VINEETHA
19	14R11A04D7	GUNTUPALLI RAVI TEJA
20	14R11A04D8	KONDURI LAKSHMI ANUSHA
21	14R11A04D9	K SASIDHAR
22	14R11A04E0	KANAKA RAMYA PRATHIMA
23	14R11A04E1	KASTURI SHIVA SHANKER REDDY

24	14R11A04E2	KODHIRIPAKA DHENUSRI
25	14R11A04E3	KOLA AISHWARYA
26	14R11A04E4	KONDOJU AKSHITHA
27	14R11A04E5	KOUDAGANI ALEKHYA REDDY
28	14R11A04E6	KUMMARIKUNTA PRASHANTH
29	14R11A04E7	KURVA SAI KUMAR
30	14R11A04E8	M AJAY KRISHNA
31	14R11A04E9	M MRIDULA GAYATRI
32	14R11A04F0	MANGALAPALLI SRAVANTHI
33	14R11A04F1	MERUGU PALLAVI
34	14R11A04F2	MITHIN VARGHESE
35	14R11A04F3	MOHD EESA SOHAIL
36	14R11A04F4	MUCHUMARI HARSHA VARDHAN REDDY
37	14R11A04F5	MUNUGANTI PRADHYUMNA
38	14R11A04F6	N DURGA RAJ
39	14R11A04F7	N SAKETH
40	14R11A04F8	N SANDHYA
41	14R11A04F9	NALLAGONI SRAVANTHI
42	14R11A04G0	P MANMOHAN SHASHANK VARMA
43	14R11A04G1	PRABHALA SRUTHI
44	14R11A04G2	PRAYAGA VENKATA SATHYA KAMESWARA PA
45	14R11A04G3	R SAILESH
46	14R11A04G4	SAMBANGI POOJA
47	14R11A04G5	SAMEENA
48	14R11A04G6	SANGOJI SAI CHANDU
49	14R11A04G7	SURANENI NAMRATHA
50	14R11A04G8	TADAKAPALLY VIVEK REDDY
51	14R11A04G9	THUMUKUNTA VAMSHI TEJA
52	14R11A04H0	TIRUNAGARI SRAVAN KUMAR
53	14R11A04H1	TRIPURARI SOWGANDHIKA
54	14R11A04H2	TUNIKI MADHULIKA REDDY
55	14R11A04H3	U SAI MANASWINI
56	14R11A04H4	VAIDYA KEERTHI MALINI
57	14R11A04H5	VANGETI PRAVALLIKA
58	14R11A04H6	VASIREDDY VENKATA SAI
59	14R11A04H7	VELDURTHY SAI KEERTHI
60	14R11A04H8	WILSON DAVIES
61	15R15A0418	KOTA RAJESH
62	15R15A0419	NAREDDY MOUNIKA REDDY
63	15R15A0420	ARTHI SHARMA
64	15R15A0421	RAJPET SHIRISHA

65	15R15A0422	MALOTH RAMESH NAIK
66	15R15A0423	PAILLA PREM RAJ REDDY

Total: 66 Males: 32 Females: 34

Class / Section: ECE 2-2 D		
1	14R11A04H9	A SIRISHA
2	14R11A04J0	ABHIJEET KUMAR
3	14R11A04J1	ADULLA PRANAV REDDY
4	14R11A04J2	AINAPARTHI SAIVIJAYALAKSHMI SANDHYA
5	14R11A04J3	AMBATI SHIVA SAI
6	14R11A04J4	ANU PRASAD
7	14R11A04J5	B SAI APOORVA
8	14R11A04J6	B SRI KRISHNA SAI KIREETI
9	14R11A04J7	CHITTOJU LAKSHMI NARAYANAMMA
10	14R11A04J8	CHOWDARAPALLY SANTOSH KUMAR
11	14R11A04J9	D SAHITHI
12	14R11A04K0	DEVULAPALLI SAI CHAITANYA SANDEEP
13	14R11A04K1	DUSARI ANUSHA
14	14R11A04K2	GOLLAPUDI SRIKETH
15	14R11A04K3	GOLLIPALLY TEJASREE
16	14R11A04K4	GOUTE SHRAVAN KUMAR
17	14R11A04K5	GUDA PRATHYUSHA REDDY
18	14R11A04K6	JUNNU RAVALI
19	14R11A04K7	K DEVI PRIYANKA
20	14R11A04K8	KANDULA MANI
21	14R11A04K9	KARRA AVINASH
22	14R11A04L0	KASULA PRADEEP GOUD
23	14R11A04L1	KOMARAKUNTA SHASHANK
24	14R11A04L2	KOTHAKOTA PHANI RISHITHA
25	14R11A04L3	MADHADI NIKHIL KUMAR REDDY
26	14R11A04L4	MANDUMULA RAGHAVENDRA
27	14R11A04L5	MOHD HAMEED
28	14R11A04L6	MOHD SHAMS TABREZ
29	14R11A04L7	MORSU GANESH REDDY
30	14R11A04L8	MUKKERA VARUN
31	14R11A04L9	NAGULAPALLY MANOHAR REDDY
32	14R11A04M0	NAMBURI LAKSHMI MANJUSHA
33	14R11A04M1	NIROGI SURYA PRIYANKA
34	14R11A04M3	PALLETI SUSHMITHA
35	14R11A04M4	PANCHAYAT SHAMILI
36	14R11A04M5	POOSA JAI SAI NISHANTH

37	14R11A04M6	PRANAV RAJU A
38	14R11A04M7	RAYCHETTI CHANDRASENA
39	14R11A04M8	REBBA BHAVANI
40	14R11A04M9	S BHARATH SAGAR
41	14R11A04N0	S V N SURYA TEJASWINI
42	14R11A04N1	SAMA MANVITHA REDDY
43	14R11A04N2	SHAMALA MEGHANA
44	14R11A04N3	SMITHA KUMARI PATRO
45	14R11A04N4	T L SARADA RAMYA KAPARDHINI
46	14R11A04N5	T VINAY KUMAR
47	14R11A04N6	TABELA OMKAR
48	14R11A04N7	TADACHINA SAINATH REDDY
49	14R11A04N8	VANGA MOUNIKA
50	14R11A04N9	VARRI PRASHANTHI
51	14R11A04P0	VASARLA SAI TEJA
52	14R11A04P1	VISHWANATHAM ANUSHA
53	14R11A04P2	Y SRI SAI ADITYA
54	14R11A04P3	YAKKALA ASHIKA
55	14R11A04P4	YALAVARTHY MAHIMA
56	14R11A04P5	YALLAPRAGADA SAI TEJASRI
57	14R11A04P6	YARASI SAI RAMYA REDDY
58	15R15A0426	JANUGANI SAI KRISHNA
59	15R15A0427	SATHENDER KUMAR YADAV
60	15R15A0428	KADEM PRAVEEN
61	15R15A0429	ARROJU AKHIL
62	15R15A0430	CH POOJA
63	15R18A0401	GUMMA SREEHARSHA REDDY
Total: 63 Males: 32 Females: 31		
Grand Total: 261(Males:134 Females:127)		

26. Group-Wise students list for discussion topics

SlNo	AdmnNo	StudentName	
Class / Section: ECE 2-2 A			
1	14R11A0401	ADITYA B	Group-1
2	14R11A0402	ADULLA JANARDHAN REDDY	
3	14R11A0403	ANDE HEMANTH REDDY	
4	14R11A0404	ANKATI NAVYA	
5	14R11A0405	ASHFAQ AZIZ AHMED	
6	14R11A0406	BANDI SANDHYA	
7	14R11A0407	BASWARAJ SHASHANK YADAV	Group-2

8	14R11A0408	BITLA SRIKANTH REDDY	
9	14R11A0409	BUDDANA DHARANI KUMAR	
10	14R11A0410	CHEBARTHI RAMYA GAYATHRI	
11	14R11A0411	CHETLAPALLI NAGA SAI SUSHMITHA	
12	14R11A0412	DASARI DHAMODHAR REDDY	
13	14R11A0413	G AYESHA SULTANA	Group-3
14	14R11A0414	G MADHURI	
15	14R11A0415	G RISHI RAJ	
16	14R11A0416	G VAMSHI KRISHNA	
17	14R11A0417	G VENKATESH YADAV	
18	14R11A0418	GONDA RISHIKA	
19	14R11A0419	GUDE GOPI	Group-4
20	14R11A0420	JAGGANNAGARI MANOJKUMAR REDDY	
21	14R11A0421	JAGGARI SRINIJA REDDY	
22	14R11A0422	JALAGAM NANDITHA	
23	14R11A0423	JAMMIKUNTLA SHIVA CHARAN	
24	14R11A0424	JATAPROLU LAKSHMI SOWMIKA	
25	14R11A0425	JEKSANI SHREYA	Group-5
26	14R11A0426	K VIJAY KUMAR	
27	14R11A0427	KAALISETTY KRISHNA CHAITANYA	
28	14R11A0428	KAKARLA MOUNICA	
29	14R11A0429	KARRE PRIYANKA	
30	14R11A0430	KL N SATYANARAYANA MURTHY	
31	14R11A0431	KONDA KRITISH KUMAR	Group-6
32	14R11A0432	KOPPULA RAHUL	
33	14R11A0433	KURUGANTI RUNI TANISHKA SHARMA	
34	14R11A0434	L THRILOK	
35	14R11A0435	MANDULA SANTOSHINI	
36	14R11A0436	MATLA PRINCE TITUS	
37	14R11A0437	NARSETTI SAIPRAVALIKA	Group-7
38	14R11A0438	NIKITHA RAGI	
39	14R11A0439	P VIJAYA ADITYA VARMA	
40	14R11A0440	PASHAM VIKRAM REDDY	
41	14R11A0441	PELLURI KARAN KUMAR	
42	14R11A0442	PERURI CHANDANA	
43	14R11A0443	PODUGU SRUJANA DEVI	Group-8
44	14R11A0445	RAJU PAVANA KUMARI	
45	14R11A0446	RAMIDI NITHYA	
46	14R11A0447	RAMOJI RAJESH	
47	14R11A0448	S ALEKHYA	
48	14R11A0449	SARANGA SAI KIRAN	

			Groups
49	14R11A0450	SHAIK SAMEER ALI	
50	14R11A0451	SOUMYA MISHRA	Group-9
51	14R11A0452	SRIRAMOJU MANASA	
52	14R11A0453	THAMADA ARUN KUMAR	
53	14R11A0454	T S SANTHOSH KUMAR	
54	14R11A0455	V BAL RAJ	
55	14R11A0456	V POOJA	
56	14R11A0457	V SRIVATS VISHWAMBER	Group-10
57	14R11A0458	V VISHNU VARDHAN REDDY	
58	14R11A0459	VENNAMANENI VAMSI KRISHNA	
59	14R11A0460	YERASI TEJASRI	
60	15R15A0401	RAMIDI SANDEEP REDDY	
61	15R15A0402	ODDARAPU HARISHBABU	Group-11
62	15R15A0403	KOLUKURI BHARGAVI	
63	15R15A0404	ADEPU MOUNIKA	
64	15R15A0405	AVANCHA PRAVALIKA	
65	15R15A0406	NELLUTLA VISHAL CHAITANYA	
66	15R15A0407	VEMULA JAMEEMA	
Total: 66 Males: 36 Females: 30			

Class / Section: ECE 2-2 B			Groups
1	14R11A0461	ADDAKULA SURESH	Group-1
2	14R11A0462	AGARTI MADHU VIVEKA	
3	14R11A0463	AKULA SAI KIRAN	
4	14R11A0464	ANUMULA SNIGDHA	
5	14R11A0465	B DIVYA	
6	14R11A0466	B MANOHAR	
7	14R11A0467	BANDARI MAMATHA	Group-2
8	14R11A0468	BINGI DIVYA SUDHA RANI	
9	14R11A0469	BIRE BHAVYA	
10	14R11A0470	CH SAI BHARGAVI	
11	14R11A0471	CHAVALI SUMA SIREESHA	
12	14R11A0472	CHELLABOINA SHIVA KUMAR	
13	14R11A0473	CHETTY AKHIL CHAND	Group-3
14	14R11A0474	CHINTAPALLI MADHAV REDDY	
15	14R11A0475	CHIVUKULA VENKATA SUBRAMANYA PRASAN	
16	14R11A0476	D NAGA SUMANVITHA	
17	14R11A0477	D VAMSI	
18	14R11A0478	DHARMENDER KEERTHI	
19	14R11A0479	EADARA NAGA SIRISHA	Group-4

20	14R11A0480	ERANKI SAI UDAYASRI ALAKANANDA	
21	14R11A0481	GANGA STEPHEN RAVI KUMAR	
22	14R11A0482	GUNDAM SHRUTHI	
23	14R11A0483	GUNDREVULA SAMEERA	
24	14R11A0484	K NAGA REKHA	
25	14R11A0485	KANDADI VARSHA	Group-5
26	14R11A0486	KURELLI SAI VINEETH KUMAR GOUD	
27	14R11A0487	MADDIKUNTA SOMA SHEKAR REDDY	
28	14R11A0488	MAMILLA SAI NISHMA	
29	14R11A0489	MARELLA NAGA LASYA PRIYA	
30	14R11A0490	MARKU VENKATESH	
31	14R11A0491	MOHAMED KHALEEL	Group-6
32	14R11A0492	MOHAMMED WASEEM AKRAM	
33	14R11A0493	MOTURI DIVYA	
34	14R11A0494	MUDIUM KOUSHIKA	
35	14R11A0495	MYLAPALLI RAMBABU	
36	14R11A0496	NAGU MOUNIKA	
37	14R11A0497	NEELAM SNEHANJALI	Group-7
38	14R11A0498	NIDAMANURI VENKATA VAMSI KRISHNA	
39	14R11A0499	NIKHIL KUMAR N	
40	14R11A04A0	ORUGANTI HARSHINI	
41	14R11A04A1	PARAMKUSAM NIHARIKA	
42	14R11A04A2	PASAM ABHIGNA	
43	14R11A04A3	PATI VANDANA	Group-8
44	14R11A04A4	PODISHETTY MANOGNA	
45	14R11A04A5	PONAKA SREEVARDHAN REDDY	
46	14R11A04A6	R NAVSHETHA	
47	14R11A04A7	R PRANAY KUMAR	
48	14R11A04A8	RAMIDI ROJA	
49	14R11A04A9	RUDRA VAMSHI	Group-9
50	14R11A04B0	S SHARAD KUMAR	
51	14R11A04B1	SAGGU SOWMYA	
52	14R11A04B2	TADELA SARWANI	
53	14R11A04B3	THOTA SAI BHUVAN	
54	14R11A04B4	VALLAPU HARIKRISHNA	
55	14R11A04B5	VECHA PAVAN KUMAR	Group-10
56	14R11A04B6	Y SAI VISHWANATH	
57	15R15A0408	ERUKALA NIKITHA	
58	15R15A0409	PUNGANUR JAYACHANDRA BHARATHWAJ	
59	15R15A0410	GALIPALLY BHARGAVA	
60	15R15A0411	PADMA ARUNRAJ	

61	15R15A0412	JAMALAPURAM NAVEEN	Group-11
62	15R15A0413	MACHANNI BALAKRISHNA YADAV	
63	15R15A0414	ANABOINA MAHENDER	
64	15R15A0415	ANABOINA SHIVA SAI	
65	15R15A0416	VEMULA VINITHA	
66	15R15A0417	CHEVU NAGESH	
Total: 66 Males: 34 Females: 32			

Class / Section: ECE 2-2 C			Groups
1	14R11A04B9	ANAMALI REETHIKA	Group-1
2	14R11A04C0	ARUMILLI LEKYA	
3	14R11A04C1	ARUMUGAM ASHWINI	
4	14R11A04C2	BASAVARAJU MEGHANA	
5	14R11A04C3	BEERAM TEJASRI REDDY	
6	14R11A04C4	BHARAT SAKETH	
7	14R11A04C5	BOMMANA HARIKADEVI	
8	14R11A04C6	BYRAGONI ROJA	Group-2
9	14R11A04C7	CANDHI SHASHI REKHA	
10	14R11A04C8	CH RENUKA	
11	14R11A04C9	CHAGANTI MOUNICA	
12	14R11A04D0	CHITTARLA LOKESH GOUD	
13	14R11A04D1	D LAVANYA	Group-3
14	14R11A04D2	D MANIKANTA	
15	14R11A04D3	DASARI VENKATA NAGA SAISH	
16	14R11A04D4	DODDA MANOJ	
17	14R11A04D5	E RAHUL CHOWDHARY	
18	14R11A04D6	GOWRISHETTY VINEETHA	
19	14R11A04D7	GUNTUPALLI RAVI TEJA	Group-4
20	14R11A04D8	KONDURI LAKSHMI ANUSHA	
21	14R11A04D9	K SASIDHAR	
22	14R11A04E0	KANAKA RAMYA PRATHIMA	
23	14R11A04E1	KASTURI SHIVA SHANKER REDDY	
24	14R11A04E2	KODHIRIPAKA DHENUSRI	
25	14R11A04E3	KOLA AISHWARYA	Group-5
26	14R11A04E4	KONDOJU AKSHITHA	
27	14R11A04E5	KOUDAGANI ALEKHYA REDDY	
28	14R11A04E6	KUMMARIKUNTA PRASHANTH	
29	14R11A04E7	KURVA SAI KUMAR	
30	14R11A04E8	M AJAY KRISHNA	
31	14R11A04E9	M MRIDULA GAYATRI	Group-6
32	14R11A04F0	MANGALAPALLI SRAVANTHI	
33	14R11A04F1	MERUGU PALLAVI	

34	14R11A04F2	MITHIN VARGHESE	
35	14R11A04F3	MOHD EESA SOHAIL	
36	14R11A04F4	MUCHUMARI HARSHA VARDHAN REDDY	
37	14R11A04F5	MUNUGANTI PRADHYUMNA	Group-7
38	14R11A04F6	N DURGA RAJ	
39	14R11A04F7	N SAKETH	
40	14R11A04F8	N SANDHYA	
41	14R11A04F9	NALLAGONI SRAVANTHI	
42	14R11A04G0	P MANMOHAN SHASHANK VARMA	
43	14R11A04G1	PRABHALA SRUTHI	Group-8
44	14R11A04G2	PRAYAGA VENKATA SATHYA KAMESWARA PA	
45	14R11A04G3	R SAILESH	
46	14R11A04G4	SAMBANGI POOJA	
47	14R11A04G5	SAMEENA	
48	14R11A04G6	SANGOJI SAI CHANDU	
49	14R11A04G7	SURANENI NAMRATHA	Group-9
50	14R11A04G8	TADAKAPALLY VIVEK REDDY	
51	14R11A04G9	THUMUKUNTA VAMSHI TEJA	
52	14R11A04H0	TIRUNAGARI SRAVAN KUMAR	
53	14R11A04H1	TRIPURARI SOWGANDHIKA	
54	14R11A04H2	TUNIKI MADHULIKA REDDY	
55	14R11A04H3	U SAI MANASWINI	Group-10
56	14R11A04H4	VAIDYA KEERTHI MALINI	
57	14R11A04H5	VANGETI PRAVALLIKA	
58	14R11A04H6	VASIREDDY VENKATA SAI	
59	14R11A04H7	VELDURTHY SAI KEERTHI	
60	14R11A04H8	WILSON DAVIES	
61	15R15A0418	KOTA RAJESH	Group-11
62	15R15A0419	NAREDDY MOUNIKA REDDY	
63	15R15A0420	ARTHI SHARMA	
64	15R15A0421	RAJPET SHIRISHA	
65	15R15A0422	MALOTH RAMESH NAIK	
66	15R15A0423	PAILLA PREM RAJ REDDY	
Total: 66 Males: 32 Females: 34			

Class / Section: ECE 2-2 D			**Groups**
1	14R11A04H9	A SIRISHA	Group-1
2	14R11A04J0	ABHIJEET KUMAR	
3	14R11A04J1	ADULLA PRANAV REDDY	
4	14R11A04J2	AINAPARTHI SAIVIJAYALAKSHMI SANDHYA	

5	14R11A04J3	AMBATI SHIVA SAI	
6	14R11A04J4	ANU PRASAD	
7	14R11A04J5	B SAI APOORVA	Group-2
8	14R11A04J6	B SRI KRISHNA SAI KIREETI	
9	14R11A04J7	CHITTOJU LAKSHMI NARAYANAMMA	
10	14R11A04J8	CHOWDARAPALLY SANTOSH KUMAR	
11	14R11A04J9	D SAHITHI	
12	14R11A04K0	DEVULAPALLI SAI CHAITANYA SANDEEP	
13	14R11A04K1	DUSARI ANUSHA	Group-3
14	14R11A04K2	GOLLAPUDI SRIKETH	
15	14R11A04K3	GOLLIPALLY TEJASREE	
16	14R11A04K4	GOUTE SHRAVAN KUMAR	
17	14R11A04K5	GUDA PRATHYUSHA REDDY	
18	14R11A04K6	JUNNU RAVALI	
19	14R11A04K7	K DEVI PRIYANKA	
20	14R11A04K8	KANDULA MANI	Group-4
21	14R11A04K9	KARRA AVINASH	
22	14R11A04L0	KASULA PRADEEP GOUD	
23	14R11A04L1	KOMARAKUNTA SHASHANK	
24	14R11A04L2	KOTHAKOTA PHANI RISHITHA	
25	14R11A04L3	MADHADI NIKHIL KUMAR REDDY	
26	14R11A04L4	MANDUMULA RAGHAVENDRA	Group-5
27	14R11A04L5	MOHD HAMEED	
28	14R11A04L6	MOHD SHAMS TABREZ	
29	14R11A04L7	MORSU GANESH REDDY	
30	14R11A04L8	MUKKERA VARUN	
31	14R11A04L9	NAGULAPALLY MANOHAR REDDY	
32	14R11A04M0	NAMBURI LAKSHMI MANJUSHA	Group-6
33	14R11A04M1	NIROGI SURYA PRIYANKA	
34	14R11A04M3	PALLETI SUSHMITHA	
35	14R11A04M4	PANCHAYAT SHAMILI	
36	14R11A04M5	POOSA JAI SAI NISHANTH	
37	14R11A04M6	PRANAV RAJU A	
38	14R11A04M7	RAYCHETTI CHANDRASENA	Group-7
39	14R11A04M8	REBBA BHAVANI	
40	14R11A04M9	S BHARATH SAGAR	
41	14R11A04N0	S V N SURYA TEJASWINI	
42	14R11A04N1	SAMA MANVITHA REDDY	
43	14R11A04N2	SHAMALA MEGHANA	
44	14R11A04N3	SMITHA KUMARI PATRO	
45	14R11A04N4	T L SARADA RAMYA KAPARDHINI	Group-8

46	14R11A04N5	T VINAY KUMAR	
47	14R11A04N6	TABELA OMKAR	
48	14R11A04N7	TADACHINA SAINATH REDDY	
49	14R11A04N8	VANGA MOUNIKA	
50	14R11A04N9	VARRI PRASHANTHI	
51	14R11A04P0	VASARLA SAI TEJA	
52	14R11A04P1	VISHWANATHAM ANUSHA	Group-9
53	14R11A04P2	Y SRI SAI ADITYA	
54	14R11A04P3	YAKKALA ASHIKA	
55	14R11A04P4	YALAVARTHY MAHIMA	
56	14R11A04P5	YALLAPRAGADA SAI TEJASRI	
57	14R11A04P6	YARASI SAI RAMYA REDDY	
58	15R15A0426	JANUGANI SAI KRISHNA	
59	15R15A0427	SATHENDER KUMAR YADAV	Group-10
60	15R15A0428	KADEM PRAVEEN	
61	15R15A0429	ARROJU AKHIL	
62	15R15A0430	CH POOJA	
63	15R18A0401	GUMMA SREEHARSHA REDDY	
Total: 63 Males: 32 Females: 31			
Grand Total: 261(Males:134 Females:127)			