GEETHANJALI COLLEGE OF ENGINEERING AND TECHNOLOGY

Cheeryal (V), Keesara (M), R. R. District

ELECTRONIC CIRCUITS AND PULSE CIRCUITS LAB

STUDENTS' MANUAL

…striving toward perfection

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

Lab Incharge: **HOD-ECE:**

EC lab: J. Mrudula   **Dr.P.Srihari**

     Associate Professor

PC lab: Prof.K.Somasekhara rao

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     Assistant Professor

GEETHANJALI COLLEGE OF ENGINEERING & TECHNOLOGY

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LABORATORY MANUAL

FOR

ELECTRONIC CIRCUITS AND PULSE CIRCUITS LAB

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GEETHANJALI COLLEGE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF *Electrical and Electronics Engineering*

(**Name of the Subject / Lab Course) : Electronic circuits and Pulse circuits Lab**

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Branch: ECE   **Version No :** *01*

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        4) Date   :   26/11/15   **4) Date :**

Verified by : 1) Name   :Prof. K. Somasekhara Rao   *** For Q.C Only.**

        2) Sign   :   **1) Name :**

        3) Design : Professor   **2) Sign   :**

        4) Date   :   **3) Design :**

                                                           4) Date   :

Approved by : (HOD)   1) Name : Dr. P.Srihari

2) Sign   :

3) Date   :

ECE DEPARTMENT

Vision of the Department

To impart quality technical education in Electronics and Communication Engineering emphasizing analysis, design/synthesis and evaluation of hardware/embedded software using various Electronic Design Automation (EDA) tools with accent on creativity, innovation and research thereby producing competent engineers who can meet global challenges with societal commitment.

Mission of the Department

i.   To impart quality education in fundamentals of basic sciences, mathematics, electronics and communication engineering through innovative teaching-learning processes.

ii. To facilitate Graduates define, design, and solve engineering problems in the field of Electronics and Communication Engineering using various Electronic Design Automation (EDA) tools.

iii. To encourage research culture among faculty and students thereby facilitating them to be creative and innovative through constant interaction with R & D organizations and Industry.

iv. To inculcate teamwork, imbibe leadership qualities, professional ethics and social responsibilities in students and faculty.

Program Educational Objectives of B. Tech (ECE) Program:

I.   To prepare students with excellent comprehension of basic sciences, mathematics and engineering subjects facilitating them to gain employment or pursue postgraduate studies with an appreciation for lifelong learning.

II. To train students with problem solving capabilities such as analysis and design with adequate practical skills wherein they demonstrate creativity and innovation that would enable them to develop state of the art equipment and technologies of multidisciplinary nature for societal development.

III. To inculcate positive attitude, professional ethics, effective communication and interpersonal skills which would facilitate them to succeed in the chosen profession exhibiting creativity and innovation through research and development both as team member and as well as leader.

Program Outcomes of B.Tech ECE Program:

1. An ability to apply knowledge of Mathematics, Science, and Engineering to solve complex engineering problems of Electronics and Communication Engineering systems.

2. An ability to model, simulate and design Electronics and Communication Engineering systems, conduct experiments, as well as analyze and interpret data and prepare a report with conclusions.

3. An ability to design an Electronics and Communication Engineering system, component, or process to meet desired needs within the realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability and sustainability.

4. An ability to function on multidisciplinary teams involving interpersonal skills.

5. An ability to identify, formulate and solve engineering problems of multidisciplinary nature.

6. An understanding of professional and ethical responsibilities involved in the practice of Electronics and Communication Engineering profession.

7. An ability to communicate effectively with a range of audience on complex engineering problems of multidisciplinary nature both in oral and written form.

8. The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental and societal context.

9. A recognition of the need for, and an ability to engage in life-long learning and acquire the capability for the same.

10. A knowledge of contemporary issues involved in the practice of Electronics and Communication Engineering profession

11. An ability to use the techniques, skills and modern engineering tools necessary for engineering practice.

12. An ability to use modern Electronic Design Automation (EDA) tools, software and electronic equipment to analyze, synthesize and evaluate Electronics and Communication Engineering systems for multidisciplinary tasks.

13. Apply engineering and project management principles to one's own work and also to manage projects of multidisciplinary nature.

SYLLABUS

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

II Year B.Tech. ECE-II Sem   L   T/P/D

-        -/3/-

(A40484) ELECTRONIC CIRCUITS AND PULSE CIRCUITS LAB

List of Experiments (16 experiments to be done):

PART –I: ELCTRONIC CIRCUITS

Minimum eight experiments to be conducted:

I) Design and Simulation in Simulation Laboratory using a Simulation Software (Minimum 6 Experiments):

1. Common Emitter Amplifier
2. Common Source Amplifier
3. Two Stage RC Coupled Amplifier
4. Current shunt and Voltage Series Feedback Amplifier
5. Cascode Amplifier
6. Wien Bridge Oscillator using Transistors
7. RC Phase Shift Oscillator using Transistors
8. Class A Power Amplifier (Transformer less)
9. Class B Complementary Symmetry Amplifier
10. Common Base (BJT) / Common Gate (JFET) Amplifier.

II) Testing in the Hardware Laboratory (Minimum 2 Experiments)

1. Class A Power Amplifier (with transformer load)
2. Class C Power Amplifier
3. Single Tuned Voltage Amplifier
4. Hartley & Colpitt's Oscillators
5. Darlington Pair
6. MOS Common Source Amplifier

Equipment required for the Laboratory:

1. For software simulation of Electronic circuits
    i) Computer Systems with latest specifications
    ii) Connected in LAN (Optional)
    iii) Operating system (Windows XP)
    iv) Suitable Simulations software
2. For Hardware simulations of Electronic Circuits
    i) Regulated Power Supply (0-30V)
    ii) CRO's

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   iii)   Functions Generators
   iv)   Multimeters
   v)   Components
3.   Win XP/ Linux etc.

PART –II: PULSE CIRCUITS

Minimum eight experiments to be conducted:

1. Linear Wave Shaping
   a. RC Low Pass Circuit for different time constants
   b RC High Pass Circuit for different time constants
2. Non-linear wave shaping
   a. Transfer characteristics and response of Clippers:
      i) Positive and Negative Clippers
      ii) Clipping at two independent levels
   b. The steady state output waveform of clampers for a square wave input
      i) Positive and Negative Clampers
      ii) Clamping at reference voltage
3. Comparison Operation of Comparators
4. Switching characteristics of a transistor
5. Design a Bistable Multivibrator and draw its waveforms
6. Design an Astable Multivibrator and draw its waveforms
7. Design a Monostable Multivibrator and draw its waveforms
8. Response of Schmitt Trigger circuit for loop gain less than and greater than one
9. UJT relaxation oscillator
10. The output- voltage waveform of Boot strap sweep circuit
11. The output- voltage waveform of Miller sweep circuit

Equipment required for Laboratories:
   Regulated Power Supply   - 0 – 30 V
   CRO   - 0 – 20 M Hz.
   Function Generators   - 0 – 1 M Hz
   Components
   Multi Meters

Mapping of the Course Outcomes related to laboratory experiments with Program Outcomes (POs):

Experiment No/Experiment Name	Course Outcome	Linkage to the Theoretical Concept	Linkage to Other Courses	Mapping of POs
Electronic Circuits: 1. Common emitter amplifier 2.Common source amplifier 3.Two stage RC coupled amplifier 4. Current shunt and voltage series feedback amplifier 5.MOS Amplifier	The student will be able to design and implement analog electronic circuits using transistors (like BJT, FET, UJT) and diodes. An ability to use multi-sim software to validate analog circuits	Single stage and Multi stage Amplifier Design by using BJT and FET. Concept of topology of feedback amplifiers	Analog and Digital communication systems, Linear Integrated Circuits	PO2,PO3,PO4,PO5, PO11,PO12
6.RC phase shift oscillator using transistors 7.Hartley oscillator and colpitt's oscillator 8.UJT relaxation oscillator	The student will be able to design and implement analog electronic circuits using transistors (like BJT, FET, UJT) and diodes. An ability to use multi-sim software to validate analog circuits	Conditions of oscillations and basic principles oscillators. Concept of feedback network, Characteristics of UJT	Analog Communications (AC), Linear integrated circuits	PO2,PO3,PO4,PO5, PO11,PO12
9.Class-A power amplifier (Transformer load)	The student will be able to design and implement analog electronic circuits using transistors (like BJT, FET, UJT) and diodes. An ability to use multi-sim software	power Amplifiers and concept of transformer load,	Analog Communications (AC), Linear integrated circuits	PO2,PO3,PO4,PO5, PO11,PO12

	to validate analog circuits			
10.Linear wave shaping a)RC low pass circuit for different time constants b)RC high pass circuit for different time constants	Able to gain expertise in designing of pulse shaping circuits by analyzing different characteristics of circuits	Working principle of RC low pass and high pass circuits	EDC,DSP,AC,	PO2,PO3,PO5,PO11, PO12
11.Non-linear wave shaping: a)Transfer characteristics and response of clippers i)Positive and negative clippers ii)Clipping at two independent levels b)The steady state out put wave form of clampers for a square wave input i)Positive and negative clampers	Able to extend and comprehend the concepts of circuit modeling to design linear & non-linear wave shaping and multi-vibrators	concept of clippers and clampers working principles of series and shunt clippers, working principles of positive and negative Clampers	Analog Communications .	PO2,PO3,PO5,PO11, PO12

ii)Clamping at reference voltage			
12.Comparison operation of comparators	Able to extend and comprehend the concepts of circuit modeling to design linear & non-linear wave shaping and multi-vibrators	Concept of basic clippers	Linear integrated circuits, Analog communications	PO2,PO3,PO5,PO11, PO12
13.Switching characteristics of transistor	The student will be able to design and implement analog electronic circuits using transistors (like BJT, FET, UJT) and diodes. An ability to use multi-sim software to validate analog circuits	Basic concepts operation of BJT	Digital integrated circuits, VLSI Design	PO2,PO3,PO5,PO11, PO12
14.Design an Astable multi-vibrators and draw its waveforms

15.Design an mono stable multi-vibrators and draw its waveforms

16.Response of Schmitt trigger circuit for loop gain less than and greater than one | An ability to design, implement and manage the electronic projects for real world applications | The principles of multi-vibrators | Linear integrated circuits, Analog communications | PO2,PO3,PO5,PO11, PO12 |
| **Additional Experiments:** | The student will be able to design and implement analog | Single stage and Multi stage Amplifier Design by using BJT | Analog and Digital communication | PO2,PO3,PO4,PO5, |

1. Two stage FET amplifier.	electronic circuits using transistors (like BJT, FET, UJT) and diodes. An ability to use multi-sim software to validate analog circuits	and FET. Concept of topology of feedback amplifiers	systems, Linear Integrated Circuits	PO11,PO12
2. Common collector amplifier				
3. Boot Strap Sweep Circuit	The students will be able to use design time base generators using BJTs			

INSTRUCTIONS

Instruction for students:-

1. Do not handle any equipment without reading the instructions /Instruction manuals.
2. Observe type of sockets of equipment power to avoid mechanical damage.
3. Do not insert connectors forcefully in the sockets.
4. Strictly observe the instructions given by the Teacher/ Lab Instructor.
5. After the experiment is over, the students must hand over the Bread board, Trainer kits, wires, CRO probes and other components to the lab assistant/teacher.
6. It is mandatory to come to lab in a formal dress (Shirts, Trousers, ID card, and Shoes for boys). Strictly no Jeans for both Girls and Boys.
7. It is mandatory to come with observation book and lab record in which previous experiment should be written in Record and the present lab's experiment in Observation book.
8. Observation book of the present lab experiment should be get corrected on the same day and Record should be corrected on the next scheduled lab session.
9. Mobile Phones should be Switched OFF in the lab session.
10. Students have to come to lab in-time. Late comers are not allowed to enter the lab.
11. Prepare for the viva questions. At the end of the experiment, the lab faculty will ask the viva questions and marks are allotted accordingly.
12. Bring all the required stationery like graph sheets, pencil & eraser, different color pens etc. for the lab class.
13. While shorting 2 or more wires for common connections like grounding, do not twist wires. Use shorting link on the bread board.

Instructions to Laboratory Teachers:-

1. Observation book and lab records submitted for the lab work are to be checked and signed before the next lab session.
2. Students should be instructed to switch ON the power supply after the connections are checked by the lab assistant / teacher.
3. The promptness of submission of records/ observation books should be strictly insisted by awarding the marks accordingly.
4. Ask viva questions at the end of the experiment.
5. Do not allow students who come late to the lab class.
6. Encourage the students to do the experiments innovatively.

PART- II PULSE CIRCUITS

INDEX.

PART-II
PULSE CIRCUITS

LINEAR WAVE SHAPING

Experiment no. 1

Prior to Lab session:

1. Study the working principle of high pass and low pass RC circuits for non-sinusoidal signal inputs.
2. Study the definitions of % tilt, time constant, cut-off frequencies and rise time of RC circuits.
3. Study the procedure for conducting the experiment in the lab.

Objective::

1. To design High pass and Low pass RC circuits for different time constants and verify their responses for a square wave input of given frequency.
2. To find the % tilt of high pass RC circuit for large time constant.
3. To study the operation of high pass RC circuit as a differentiator and low pass circuit as an integrator.

Apparatus:

1. CRO (Dual Channel 0-20 MHz)   -   1 No.
2. Signal Generator (1Hz to 1 MHz)   -   1No.
3. Decade capacitance box   -   1 No.
    Or Capacitors: 0.1µF, 0.01 µF, 0.001 µF   -   1 No. each
4. Resistor (100 KΩ)   -   1 No.
5. Connecting wires
6. Bread board

Circuit Diagrams:
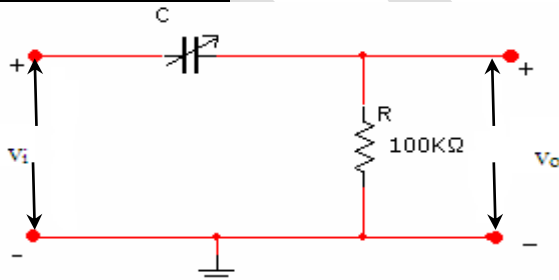
Fig 1.1 High Pass RC circuit   Fig 1.2 Low Pass RC circuit
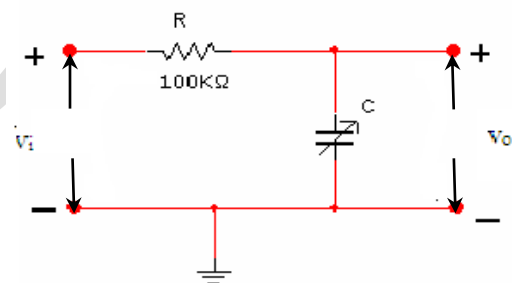
Theory:

Resistors and Capacitors can be connected in series or parallel in various combinations. The RC circuits can be configured in two ways as shown in the above circuit diagrams.

i.e.   i) High Pass RC circuit   ii) Low Pass RC circuit

High Pass RC circuit:

The reactance of the capacitor depends upon the frequency of operation.   At   very high frequencies, the reactance of the capacitor is very low. Hence the capacitor in fig.1.1 acts as short circuit for high frequencies. As a result the entire input almost appears at the output across the resistor.

At low frequencies, the reactance of the capacitor is very high. So the capacitor acts as almost open circuit. Hence the output is very low. Since the circuit allows only high frequencies, it is called as high pass RC circuit.

High - pass RC circuit as a differentiator:

In high pass RC circuit, if the time constant is very small in comparison with the time required for the input signal to make an appreciable change, the circuit is called a "Differentiator". Under these circumstances, the voltage drop across R will be very small in comparison with the drop across C. Hence we may consider that the total input Vi   appears across C, so that the current is determined entirely by the capacitor.   **i = C dVi/dt.**

The output voltage across R is, V_o = **RC (dVi/dt).**

i.e. The output voltage is proportional to the differential of the input signal. Hence the high pass RC circuit acts as a differentiator when RC << T.

Low Pass RC circuit:

The reactance of the capacitor   depends upon the frequency of operation.   At   very high frequencies, the reactance of the capacitor is almost zero. Hence the capacitor in fig.1.2 acts as short circuit. As a result, the output will fall to zero.

At low frequencies, the reactance of the capacitor is infinite. So the capacitor acts as open circuit. As a result the entire input appears at the output. Since the circuit allows only low frequencies, it is called as low pass RC circuit.

Low — Pass RC circuit as an integrator:

In low pass circuit, if the time constant is very large in comparison with the time required for the input signal to make an appreciable change, the circuit is called an "integrator".   Under these circumstances the voltage drop across C will be very small in comparison to the drop across R and almost the total input Vi appears across R .i.e. **i = V_i/R.**

∴The output signal across C is $$V_o = \left(\frac{1}{c}\right)\int i\,dt = \left(\frac{1}{RC}\right)\int V\,dt$$

i.e. The output is proportional to the integral of the input signal. Hence the low pass RC circuit acts as a integrator for $RC \gg T$.

Design:

RC high pass circuit:

    i)   Large time constant: $RC \gg T$:

    Where RC is the time constant 'τ' and T is time period of Input signal.

            Let $RC = 10\ T$, Choose $R = 100k\Omega$, $f = 1kHz$.

                       $C = 10 / (10^3 \times 100 \times 10^3) = 0.1\mu f$

    ii)   Medium time constant: $RC = T$

                    $C = T/R = 1/ (10^3 \times 100 \times 10^3) = 0.01\mu f$

    iii)   Short time constant: $RC \ll T$

                $RC = T/10$ ➡ $C = T/10R = 1/(10 \times 10^3 \times 100 \times 10^3) = 0.001\ \mu f$.

RC low pass circuit: (Design procedure is same as RC high pass circuit)

i) Large time constant   : $RC \gg T$, $C = O.1\mu f$

ii) Medium time constant : $RC = T$, $C = 0.01\ \mu f$

iii) Short time constant   : $RC = T/10$, $C = 0.001\ \mu f$

Expected output wave forms of High pass RC circuit for square wave input:

    Consider the input at V^1 during T_1 and V^{11} during T_2 then the voltages V_1, $V_1{}^1$, V_2, $V_2{}^1$ are given by following equations.

$$V_1^1 = V_1.\,e^{-\frac{T1}{RC}}$$ $V_1{}^1 - V_2 = V$

$$V_2^1 = V_2.\,e^{-\frac{T2}{RC}}$$ $V_1 - V_2{}^1 = V$

For a symmetrical square wave

$$V_1^1 = V \div \left(1 + e^{\frac{T}{2RC}}\right)$$ and $$V_1 = V \div \left(1 + e^{-\frac{T}{2RC}}\right)$$

and   because of symmetry $V_1 = -V_2$ $V_1{}^1 = -V_2{}^1$

The percentage tilt 'P' is defined by $P = (V_1 - V_1{}^1) / (V/2) \times 100$ -------------1.1

Input wave Form
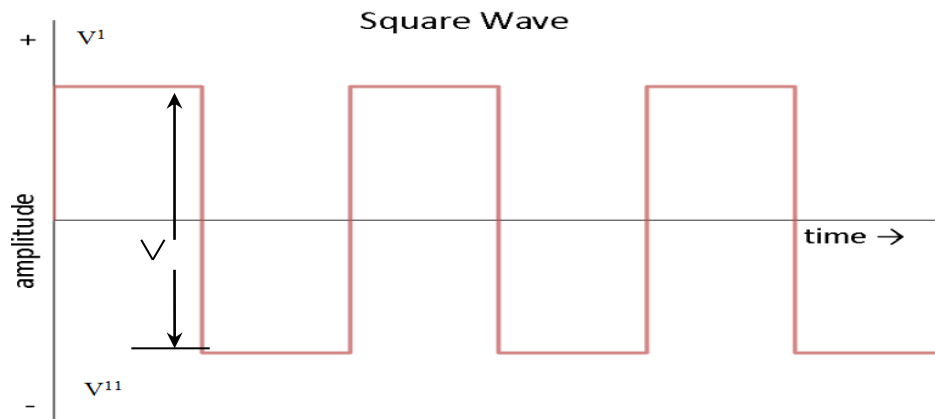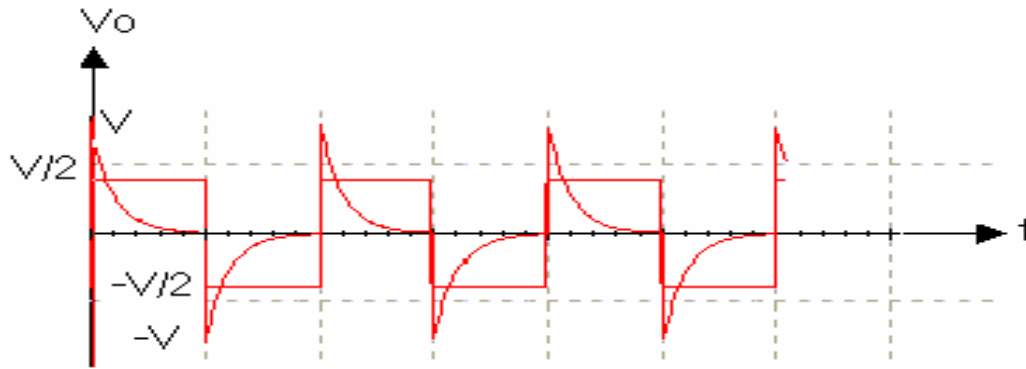

a) RC = T
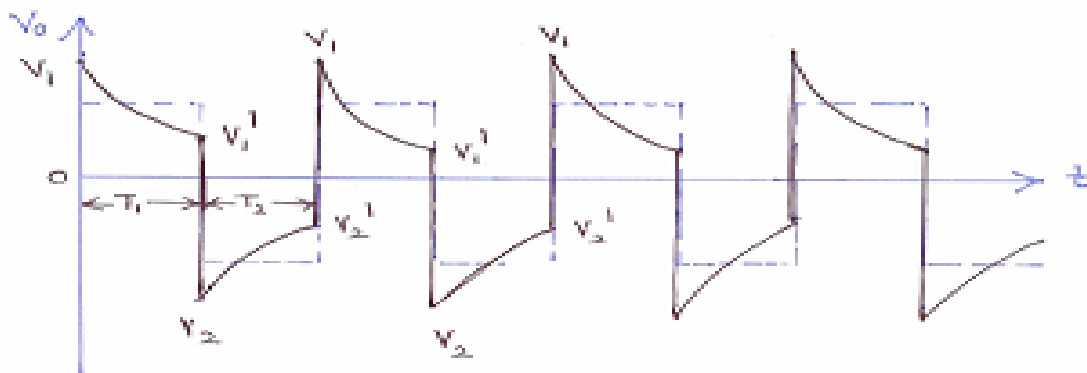
b) RC >> T (RC = 10T)
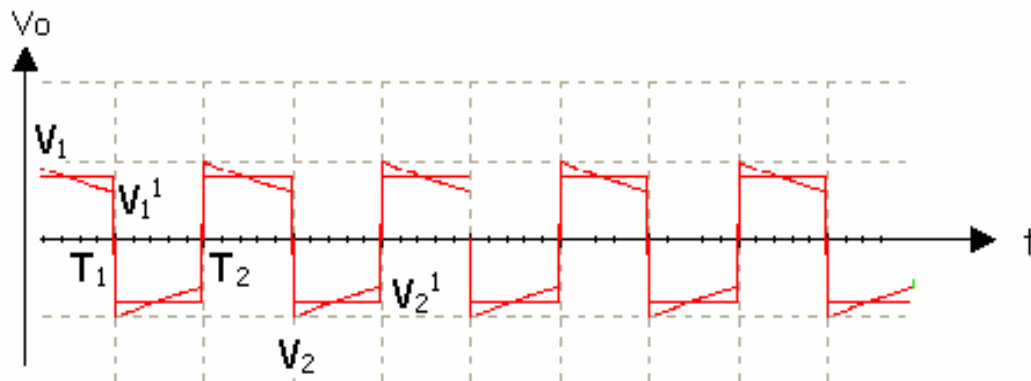
c) RC << T (RC = 0.1T)

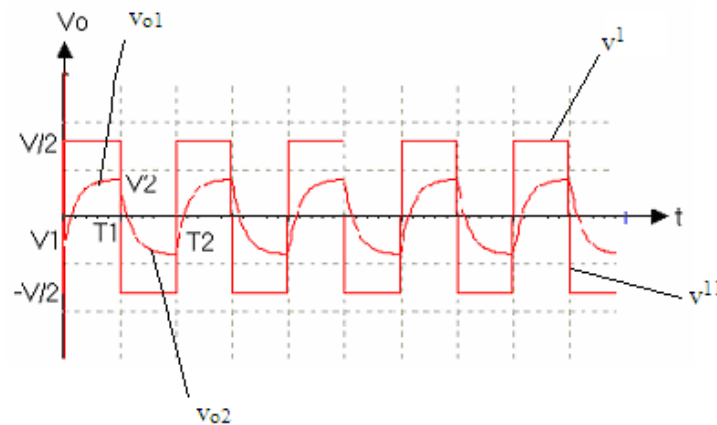**Expected output wave forms of Low pass RC circuit for square wave input:**

Consider the input at V^1 during T_1 and V^{11} during T_2 then the voltages V_{01}, V_{02} during T_1 and T_2 is given by following equations.

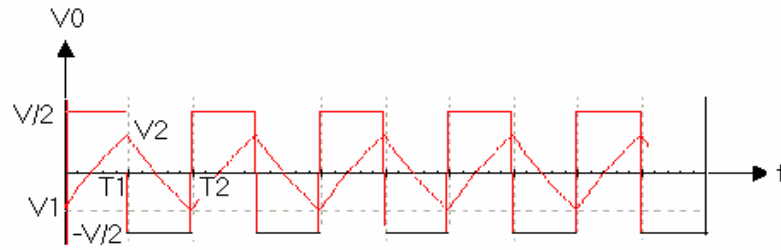$$V_{01} = V^1 + (V_1 - V^1).e^{-\frac{T1}{RC}}$$

$$V_{02} = V^{11} + (V_2 - V^{11}).e^{-\frac{T2}{RC}}$$

For a symmetrical square wave $V_2 = V/2(\tanh x)$ and $V_1 = -V_2$ where $x = T/(4RC)$

a) RC = T

b) RC >> T

c) RC << T
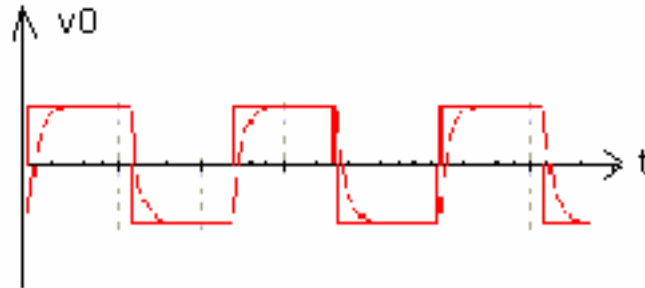
Procedure:

      1. Connect the circuits as shown in the above figures (fig.1.1 and fig 1.2).

      2. Apply the Square wave input to this circuit ($Vi = 2\ V_{P-P}$, f = 1KHz)

      3. Observe the output waveform for (a) RC = T, (b) RC<<T, (c) RC>>T

      4. Verify the values with theoretical calculations.

Observations:

High pass RC circuit

S.No.	Time constant	Voltage levels	
1.	RC=T	V_1	
		$V_1{}^1$	
		V_2	
		$V_2{}^1$	
2	RC>>T (RC=10T)	V_1	
		$V_1{}^1$	
		V_2	
		$V_2{}^1$	
3	RC<<T (RC=0.1T)	V_1	
		$V_1{}^1$	
		V_2	
		$V_2{}^1$	

Table 1.1

Low pass RC circuit:

S.No	Time constant	Voltage levels	
1	RC=T	V_1	
		V_2	
2	RC>>T (RC=10T)	V_1	
		V_2	
3	RC<<T (RC=0.1T)	V_1	
		V_2	

Table 1.2

Time Constant	Voltage levels (Theoretical)			Voltage levels (Practical)			%Tilt (Theoretical)	%Tilt (use equation 1.1) (Practical)
	V_1	V_1^1	V_1	V_1	V_1^1	V		
RC<<T								
RC=T								
RC>>T								

Result:

1. The responses of Low pass and High pass RC circuits have been verified for square wave inputs for different time constants.
2. Verified the theoretical and practical values of %P.
3. Observed the operation of differentiator and integrator circuits.

Viva questions

1. What is a linear network? What is linear wave shaping?
2. Define Time constant. What is its formula?
3. Define % tilt and rise time. Write the expressions for the same.
4. When High pass RC circuit is used as Differentiator? What is the formula for the output, when operated as differentiator?
5. When Low pass RC circuit is used as Integrator? What is the formula for the output, when the circuit is operated as Integrator?
6. What is the Difference between Low pass and High pass RC circuits.
7. A Capacitor blocks __ signal and passes __ signal. The voltage across the ___ will not change suddenly.
8. Explain 3 dB values for a LP and HP circuit.
9. A differentiator converts a square wave into what form? An integrator converts a square wave into what form?
10. What are the formulae for charging a capacitor from an initial voltage of Vi to a final voltage of Vo.
11. Instead of using RC components for a low pass or high pass, how the circuit changes , if we want to use RL components? What are the values for the Time constant for RL circuits?
12. When a capacitor in a low pass circuit charges to 99.3 % (treated as fully charged) for a step input to a Low pass filter?
13. What is a peaking circuit?
14. What is a ringing circuit?
15. Why resistive attenuators are to be compensated?

Design Problems
1. Design RC Differentiator circuit for frequency of 2kHz.
2. Design RC high circuit for a square wave input signal of frequency 2.5KHz for
    i) RC=10T   ii)RC=T   iii)RC=T/10
3. Design low pass circuit for a square wave signal of 3KHz for
    i)   RC=5T   ii) RC=T   iii) RC = T/5

4. Verify the output of circuits given in Fig1.1 and Fig 1.2 for input square wave of frequencies 10KHz and 500Hz.
5. Verify the RC high pass circuit output for sinusoidal input.

Outcomes: After finishing this experiment the students are able to
1. Design High pass and Low pass circuits with different time constants.
2. Find % Tilt
3. Observe the output waveforms for a given square wave.

Experiment No: 2

NON LINEAR WAVE SHAPING - CLIPPERS

Prior to the Lab session:

1. Study the operation and working principle of Diode under Forward bias and Reverse bias conditions.
2. Study the Classification of clipper circuits and their operation with positive reference, negative reference and zero reference voltages.
3. Study the procedure for conducting the experiment in the lab.

Objective:

1. To study the various clipper circuits and to plot the output waveforms for a sinusoidal input of given peak amplitude.(Choose f=1 kHz, Vp-p =10v)
2. To observe the transfer characteristics of all the clipping circuits on CRO.

Apparatus:

1.	CRO (Dual Channel 0 to 20 MHz)	-	1 No.
2.	Signal Generator (1Hz to 1 MHz)	-	1 No.
3.	Diode (1N4007)	-	1 No.
4.	Resistor (2.2 KΩ)	-	2 Nos.
5.	D.C Power Supply (0 – 30 V (dual))	-	1 No.
6.	Connecting wires		
7.	Bread board		

Theory:

The process whereby the form of sinusoidal signals is going to be altered by transmitting through a non-linear network is called non-linear wave shaping. Non-linear elements (like diodes, transistors) in combination with resistors can function as clipper circuit.

Clipping circuits are used to select transmission of that part of an arbitrary wave form which lies above or below some particular reference voltage level. Clipping circuits are also referred to as Limiters, Amplitude selectors or Slicers.

Clipping circuits are constructed using a combination of resistors, diodes or transistor and reference voltage. Clipping circuits are classified based on the position of diode as

i) Series diode clipper   ii) Shunt diode clipper

and further they are classified as, with '0' reference, with +ve reference, with –ve reference; also as positive clipper , negative clipper.
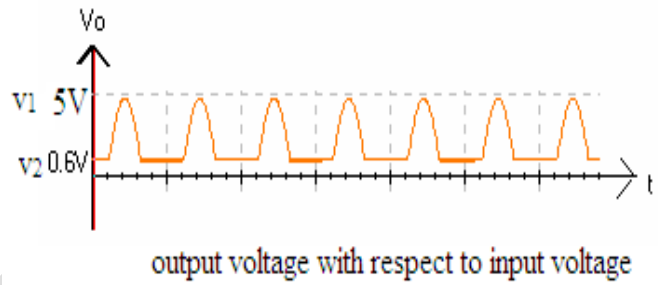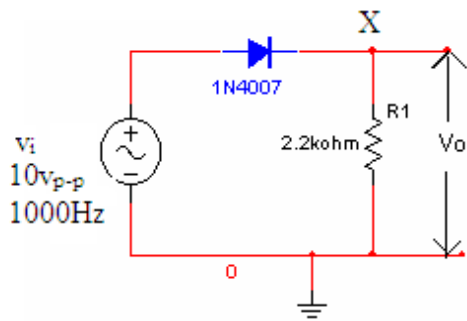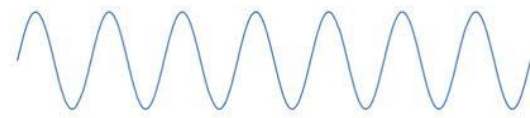
Procedure:

1. Connect the circuit as shown in the figures given below.
2. In each case, apply 10 V P-P, 1 KHz Sine wave as Input using a signal generator.
3. Observe the Output waveform (V_O in the circuit) on the CRO and compare it with Input waveform.
4. Sketch the Input as well as Output waveforms and mark the voltage levels.
5. Note the changes in the Output due to variations in the reference voltage $V_R = 0V$, 2V.. etc.
6. Obtain the transfer characteristics of Clipper circuit, by keeping CRO in X-Y mode.
7. Repeat the above steps for all the clipping circuits.

Precautions:

1. Set the CRO Output channel in DC mode always.
2. Observe the waveforms simultaneously in two channels by keeping the same reference ground.
3. See that there is no DC component in the INPUT.
4. To find transfer characteristics, apply input to the X-Channel, Output to Y-Channel, adjust the dot at the center of the screen when CRO is in X-Y mode. Both the channels must be in ground, then remove ground and plot the transfer characteristics

Circuit diagrams:

Input Signal

X

1N4007

V_i
$10v_{p-p}$
1000Hz

2.2kohm   R1   Vo

0

V_O

v_1 5V

v_2 0.6V

t

output voltage with respect to input voltage

V_O

v_1 4.4 V

v_2 0.6V

t

output voltage as measured at point X

Transfer characteristics:

$V_o(V)$

Diode
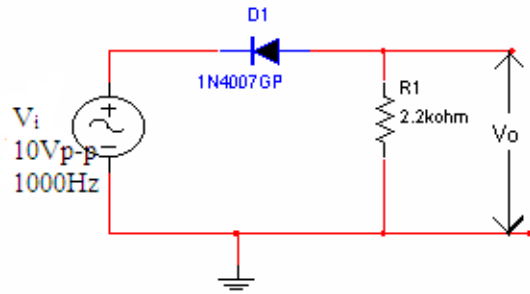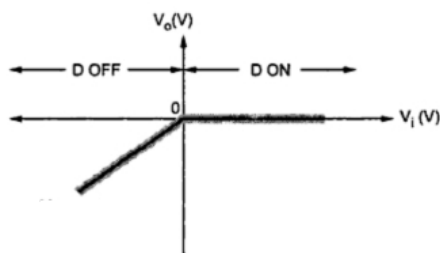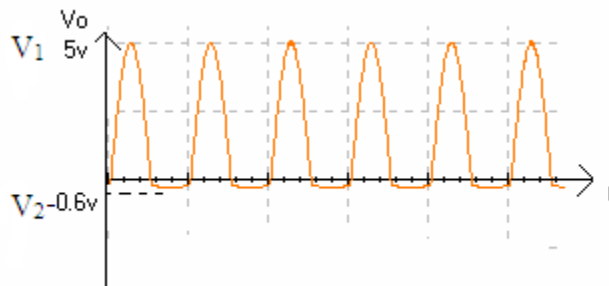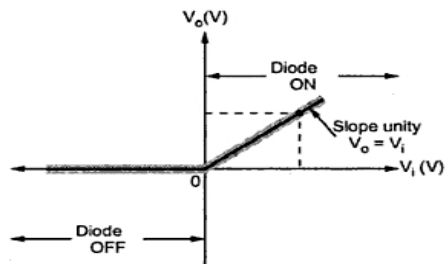ON

Slope unity
$V_o = V_i$

0    $V_i (V)$

Diode
OFF
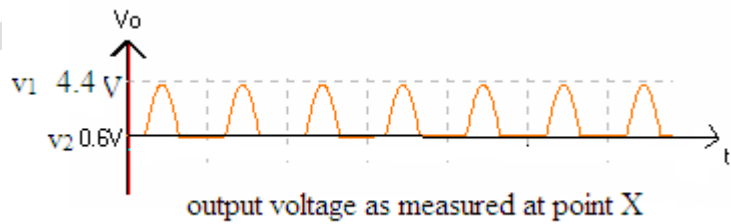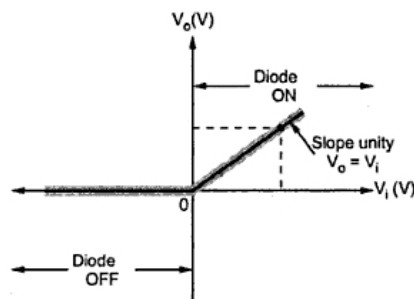
Fig 2.1 Negative clipper with zero reference (Series clipper)
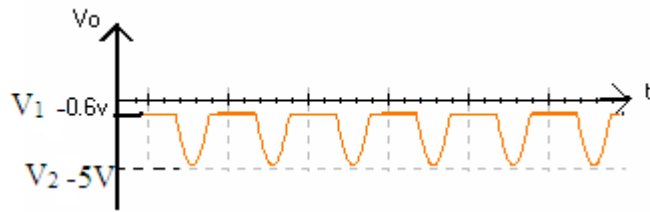
Transfer characteristics:

Fig 2.2 Positive clipper with zero reference (Series clipper)
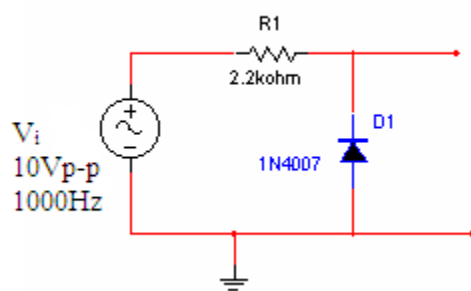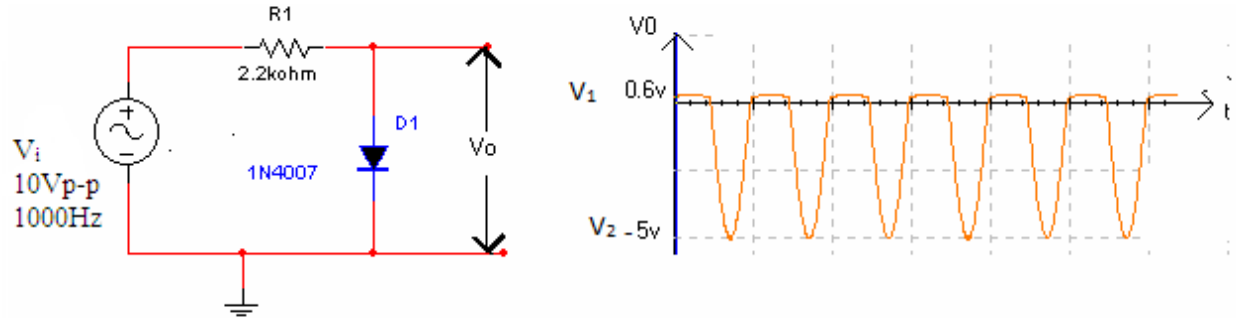

Transfer characteristics:

Fig 2.3 Negative clipper with zero reference (Shunt clipper)

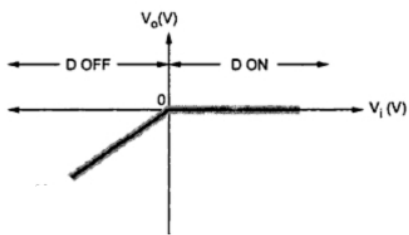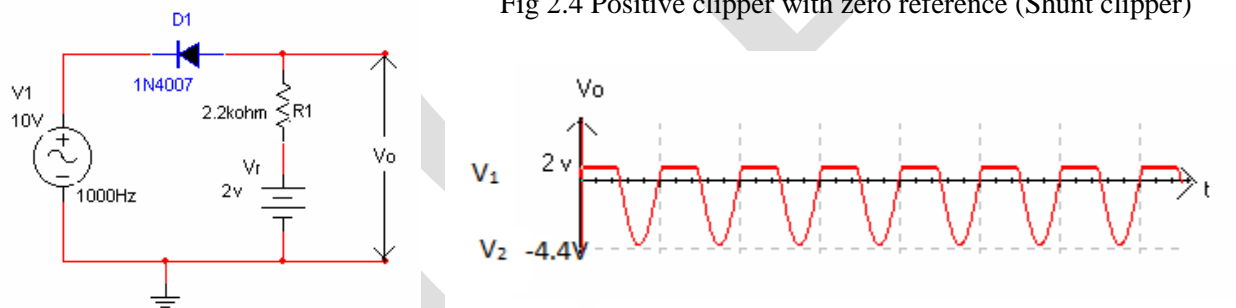**Transfer characteristics:**

Fig 2.4 Positive clipper with zero reference (Shunt clipper)
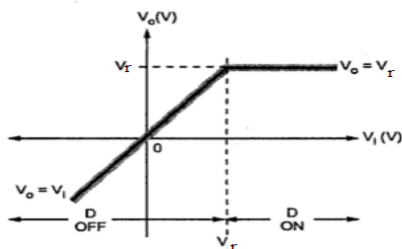

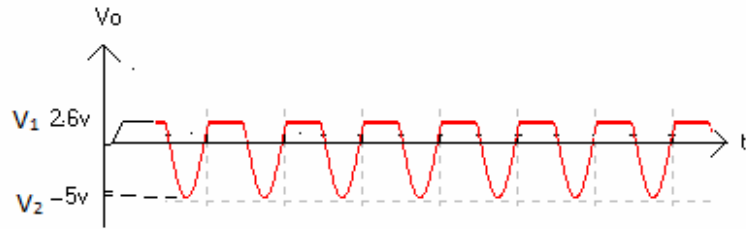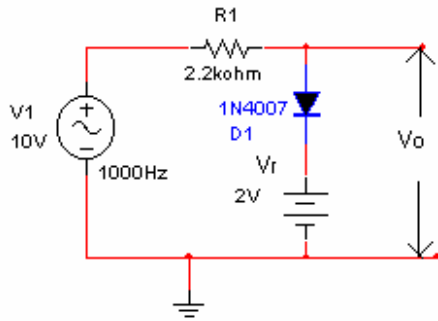**Transfer characteristics:**

Fig. 2.5 Positive clipper with positive reference (Series clipper)
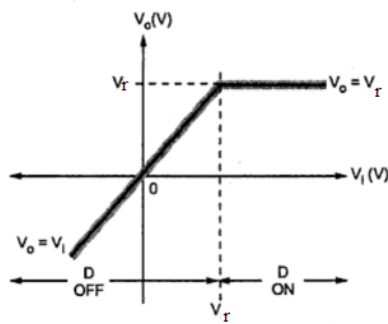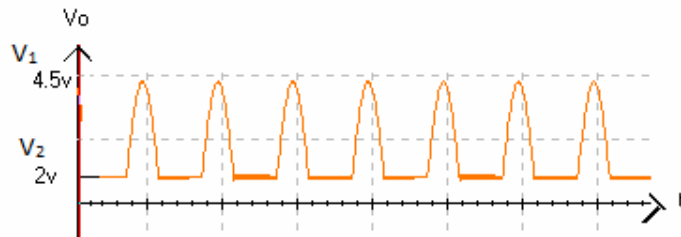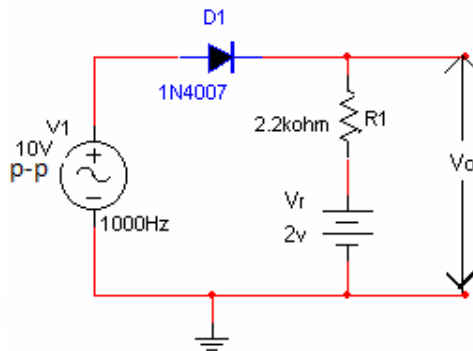
F

Transfer characteristics:

Fig. 2.6 Positive clipper with positive reference (Shunt clipper)

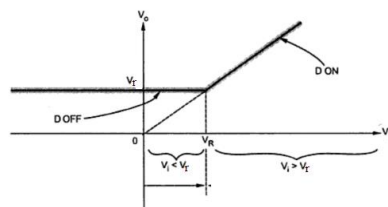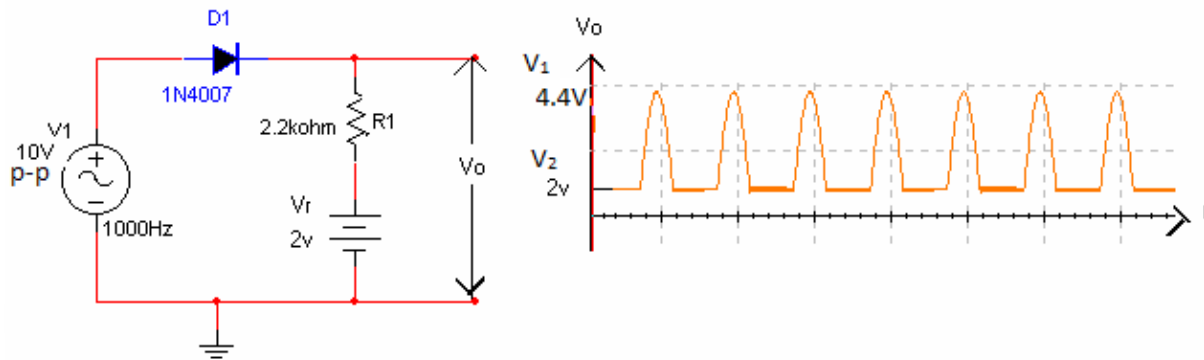**Transfer characteristics:**

Fig. 2.7 Negative clipper with positive reference (Series clipper)
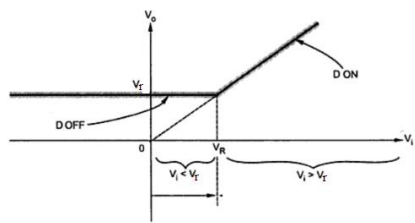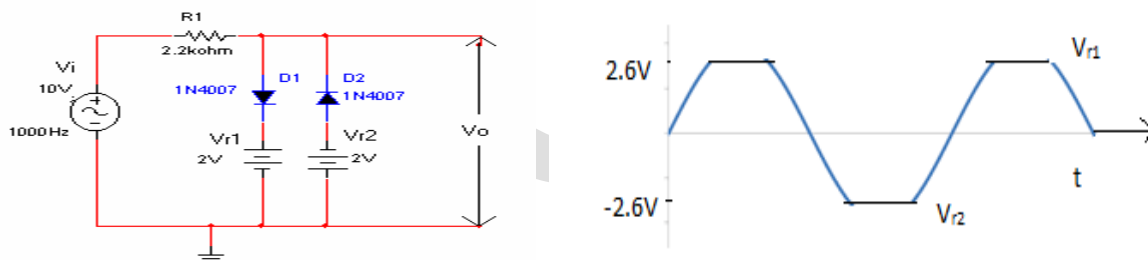

Transfer characteristics:

Fig.2.8 Negative clipper with positive reference (Shunt clipper)
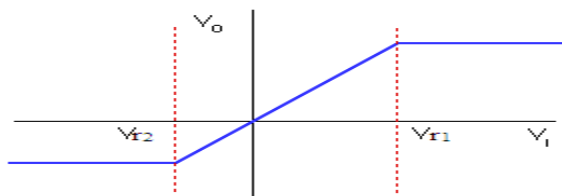

Transfer characteristics:

Fig.2.9 Clipping at two independent levels.

Observations:

S. No.	Type of Clipper	Reference Voltage	Practical Clipping Voltage levels	
1	Series Positive Clipper	0V	V1	
			V2	
		2V	V1	
			V2	
2	Series Negative Clipper	0V	V1	
			V2	
		2V	V1	
			V2	
3	Shunt Positive Clipper	0V	V1	
			V2	
		2V	V1	
			V2	
4	Shunt Negative Clipper	0V	V1	
			V2	
		2V	V1	
			V2	
5	Two level clipper		V1	
			V2	

Inference: The different types of clippers circuits are studied and observed the response for various combinations of V_R and clipping diodes.

Viva Questions:

1. Define non linear wave shaping? What are the non-linear components?
2. Define clipping circuit? What are the other names for clippers?
3. Write the piecewise linear characteristics of a diode?
4. What are the different types of clippers?
5. Which kind of a clipper is called a slicer circuit?
6. What are the applications of Clipper Circuits?
7. What is the figure of merit for diodes used in clipping circuits?
8. What is the influence of the practical diode compared to the ideal diode, in the above circuits?
9. Instead of sinusoidal wave form as input, if we give other wave forms like triangular or square, then how the clipping action is performed?
10. What is $V\gamma$ for Ge diode and $V\gamma$ for Si diode?

Design Problems
1. Design a clipper circuit to get the output shown in below for a sinusoidal input with 10V peak to peak.
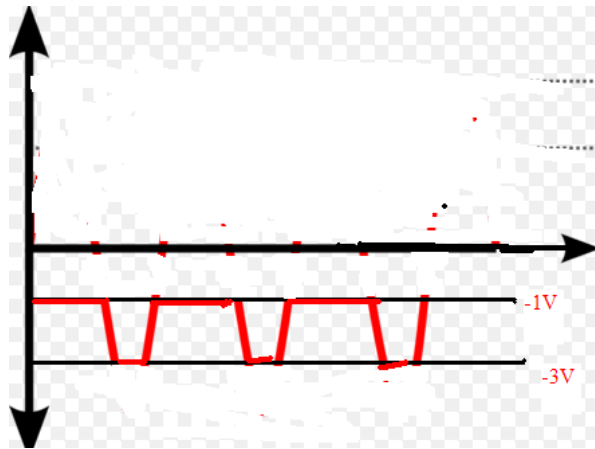
2. Design a clipper circuit using zener diode with 4.7V break down voltage.
3. Verify the output of clipper circuit for square & triangular inputs.

Outcomes: After finishing this experiment, students are able to design different types of clipper circuits and observe the input – output waveforms in the CRO and obtain the transfer characteristics for each circuit.

Experiment No: 3

NON LINEAR WAVE SHAPING-CLAMPPERS

Prior to the Lab session:

1. Study the operation and working principle of Clamper circuits
2. Study the Classification of clamper circuits and its operation with positive reference, negative reference and zero reference voltages.
3. Study the procedure for conducting the experiment in the lab.

Objective:

l. To study the various clamping circuits and to plot the output waveforms for a sinusoidal input of given peak amplitude. (Choose f=l KHz, Vp-p =l0 V)

Apparatus:

l.	CRO (Dual Channel 0 to 20 MHz)	-	l No.
2.	Signal Generator (1Hz to 1 MHz)	-	l No.
3.	Diode (lN4007)	-	l No.
4.	Resistor (l00 KΩ)	-	l No.
5.	Capacitor (0.1 pF)	-	l No.
6.	D.C Power Supply 0 – 30 V (dual)	-	l No.
7.	Connecting wires		
8.	Bread board		

Theory:

The process where sinusoidal signals are going to be altered by transmitting through a non-linear network is called non-linear wave shaping. Non-linear elements (like diodes) in combination with resistors and capacitors can function as clamping circuit.

Clamping circuits add a DC level to an AC signal. A clamper is also referred to as DC restorer or DC re-inserter. The Clampers clamp the given waveform either above or below the reference level, which are known as positive or negative clampers respectively.

Clamping circuits are classified as two types.

i) Negative Clampers   ii) Positive Clampers

Procedure:

l. Connect the circuit as shown in the figure 3.1 below.

2. Apply a Sine wave of 10V P-P, 1 KHz at the input terminals with the help of Signal Generator.
3. Observe the Input & Output waveforms on CRO and plot the waveforms and mark the values with
   $V_R = 0V$, 3V, etc.
4. Output is taken across the load RL.
5. Repeat the above steps for all clamping circuits (fig 3.2 to fig 3.6) as shown.
6. Draw the waveforms, assuming the diode is practical.
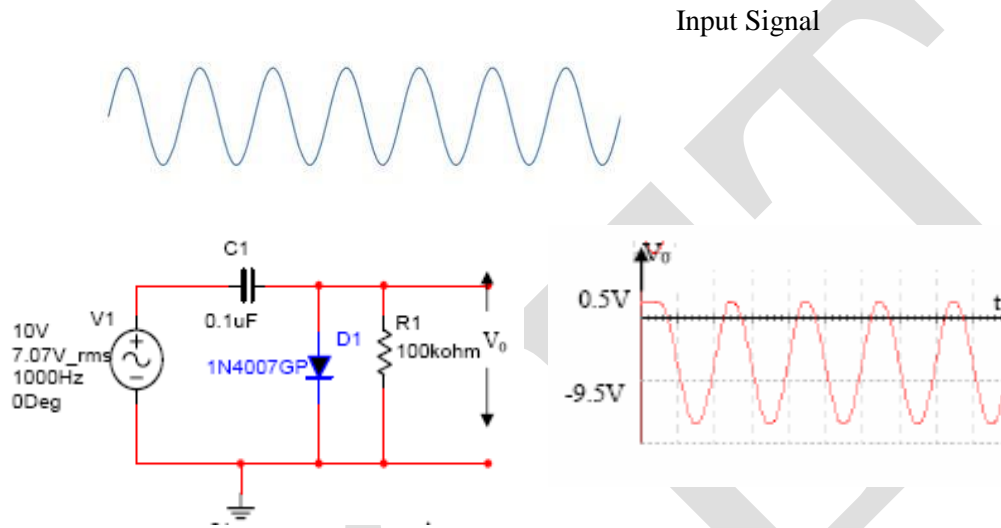
Circuit diagrams:

Input Signal

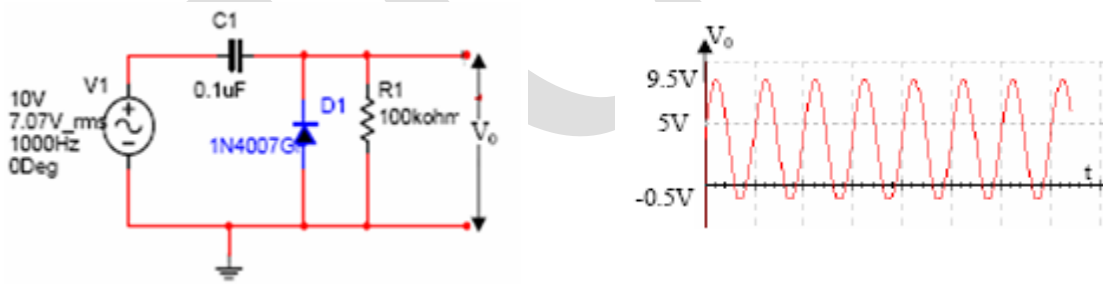Fig.3.1 Negative clamping with zero reference voltage

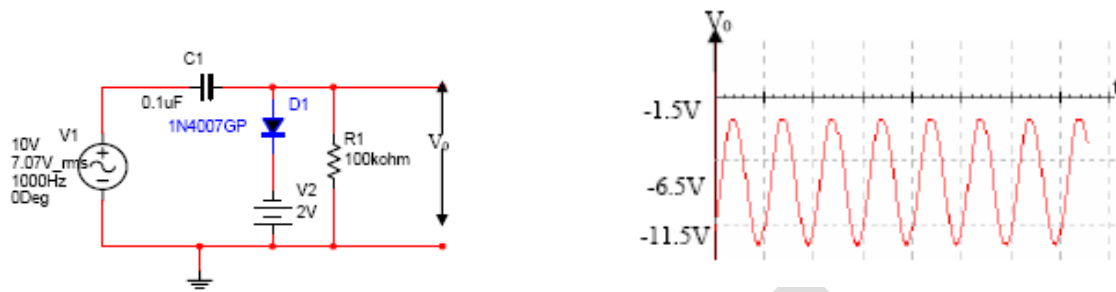Fig.3.2 positive clamping with zero reference voltage

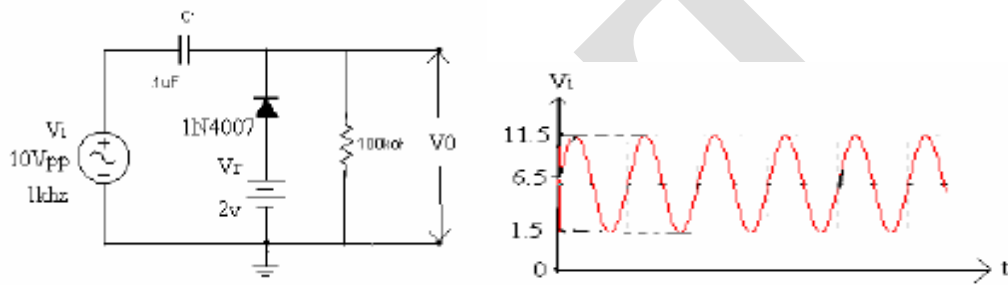Fig.3.3 Negative clamping with Negative reference voltage

Fig.3.4 positive clamping positive reference voltage
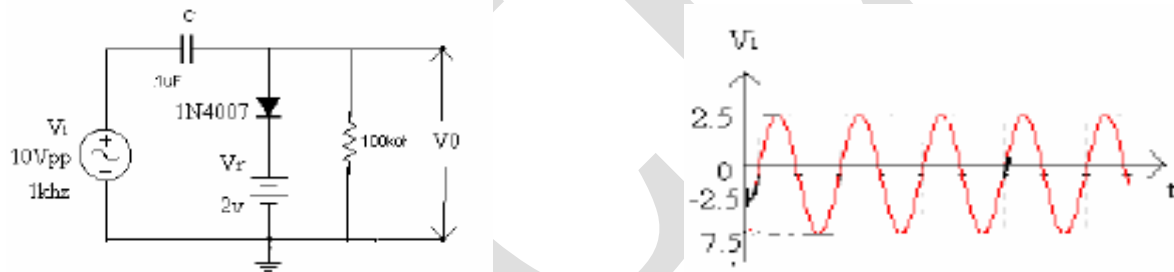
Fig.3.5 Negative clamping with Positive reference voltage
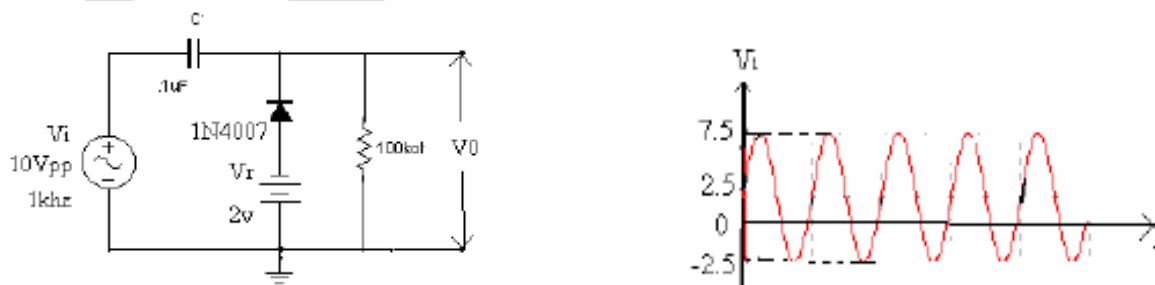
Fig.3.6 Positive clamping with Negative reference voltage

Observations:

Sl No.	Type of Clamper	Reference Voltage	Practical clamping reference Voltage levels	
1	Positive Clamper	0V	V1	
			V2	
		2V	V1	
			V2	
		-2V	V1	
			V2	
2	Negative Clamper	0V	V1	
			V2	
		2V	V1	
			V2	
		-2V	V1	
			V2	

Inference:

The different types of clamping circuits are studied and the response was observed for various combinations of V_R, capacitors and diodes.

Viva Questions

1. What are the applications of clamping circuits?
2. What is the synchronized clamping?
3. Explain the Principle of operation of Clampers.
4. What is clamping circuit theorem.
5. What is the function of the capacitor in clamper circuit?
6. What are the effects of diode characteristics on the output of the Clamper?
7. If we interchange the diode and the capacitor in fig 1 above, how the circuit behaves?
8. Calculate the power dissipation in the Resistor for any one of the above circuits?
9. What is the difference between a clipper and a clamper?
10. What are the other names for clampers?

Design Problems

1. Design a circuit that clamps the positive peaks to zero that can effectively provide DC restoration to input with frequency extending up to 1.5KHz.
2. How much voltage will get across capacitor in clamper circuit with input voltage of 20Vp-p

3. Design a negative clamper circuit from positive clamper circuit.

Outcomes: After finishing this experiment students are able to design different types of clamper circuits.

TRANSISTOR AS A SWITCH

Prior to the Lab session:

1. Study the operation and working principle of the Transistor in all regions.
2. Study the procedure for conducting this experiment in the lab.

Objective:

1. To study the Switching characteristics of a transistor.
2. Design Transistor to act as a Switch and verify the operation. Choose $V_{CC} = 10V$, $I_{Cmax} = 10$ mA, $h_{fe} = 50$, V_{CESat}
   $V_{CESat} = 0.2V$, $V_{in} = 4Vp$-p, $V_{BESat} = 0.6$ V.

Apparatus:

1.	CRO 0 – 20 MHz (Dual Channel)	-	1 No.
2.	Function Generator 1Hz– 1 MHz	-	1 No.
3.	Resistor (1 KΩ, 8.2 KΩ)	-	1 each
4.	Transistor (BC 107)	-	1 No.
5.	D.C Power Supply 0-30V (dual)	-	1 No.
6.	Connecting wires		
7.	Bread board		

Circuit diagram:
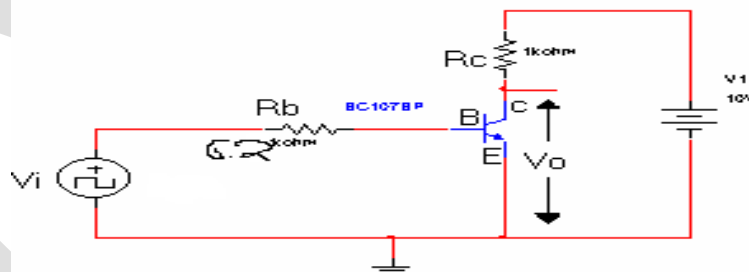
Theory:

        The Transistor can act as a switch. To operate the transistor as a switch, it has to be operated in saturation region for ON state and to be operated in cut off region for OFF state.

        When the Input voltage V_i is negative or zero, transistor is cut-off and no current flows through R_c. Hence V_0 is approximately equal to V_{CC}. When Input Voltage V_i is changed to positive voltage, transistor will be driven into saturation. Then, $V_0 = Vcc – I_CR_C \cong V_{CESat}$., which is a very small voltage.

Design procedure:

When Transistor is ON, $R_C = (V_{CC} - V_{CEsat})/I_{Cmax}$
$$= (10-0.2) / 10mA$$
$$= 1K\Omega$$

$I_B \geq I_{Cmax} /h_{fe}$
$\geq 10mA /50$
$I_B \geq 0.2mA$

To keep transistor remain in ON, I_B should be greater then $I_{Bmin} = 0.2mA$

$V_{in} = I_B R_B + V_{BEsat}$
$2V = 0.2mA. R_B + 0.6 V$
$R_B = 7 K\Omega$ (Choose Practical values as 8.2 KΩ)

Procedure:

1. Connect the circuit as shown in the above figure.
2. Apply the Square wave of 4 Vp-p at frequency of 1 KHz
3. Observe the waveforms at Collector and Base of the transistor and plot it.

Precautions:

1. Keep the CRO in DC mode while measuring the Output waveform at collector and base,
2. For measuring $V_{BE\ Sat}$ and $V_{CE\ Sat}$ keep volts/div switch at either O.2 or O.5 position.
3. When the square wave is being applied, ensure that there is no DC voltage in that. This can be checked by CRO in either in AC or DC mode. There should not be any jumps/distortion in waveform on the screen.

Waveforms:
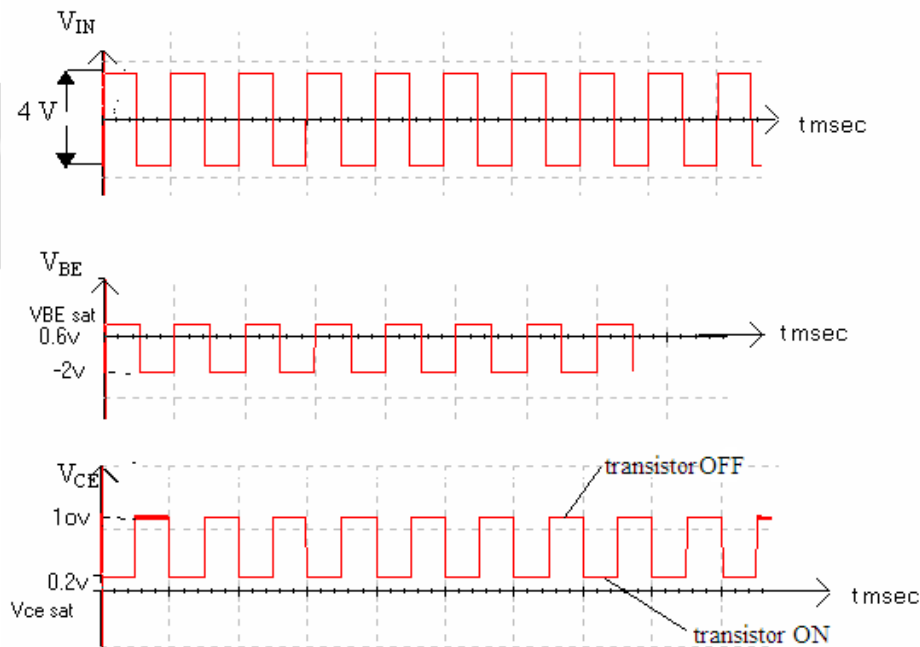
Inference:

Transistor as a switch has been designed operated and Output waveforms are observed.

Viva Questions

1. Mention typical values of $V_{BE\ Sat}$, $V_{CE\ Sat}$ for both Si, Ge Transistors?
2. Define ON time and OFF time of the transistor?
3. Define Rise time & fall time of a transistor switch?
4. Define Storage time and delay time?
5. What is the phase difference between the input and the output, when the transistor is conducting?
6. What modifications are to be done in the above circuit if we use PNP transistor instead of NPN transistor?
7. How to calculate I_C in the above circuit, when the transistor is ON?
8. What is the output voltage swing for the above circuit?
9. Why square wave is given as input instead of a sinusoidal wave for switching ON and OFF of the transistor?
10. In which regions Transistor acts as a switch?

Design problem
1. Design transistor switch to get an output of $12V_{p-p}$ swing.
2. Can we apply sinusoidal signal to transistor as switch & verify the output for the same.
3. Design a high speed transistor switch.

Outcomes: After finishing this experiment, the students are able to design a transistor switch circuit and observe the waveforms.

Experiment No: 5

UJT RELAXATION OSCILLATOR

Prior to the Lab session:

1. Study the operation and working of Uni-Junction Transistor.

2. Study the procedure for conducting the experiment in the lab.

Objective:

   1.To Study the operation of UJT as a Relaxation Oscillator

   2.Calculate sweep time and flyback time of UJT relaxation oscillator.

Apparatus:

1. CRO 0 – 20 MHz (Dual channel)   -   1No.
2. Function generator 1Hz – 1 MHz   -   1No.
3. Capacitor (0.1µF)   -   1 No
4. Resistors (1kΩ, 33KΩ, 510Ω)   -   1 No each.
5. Uni- junction transistor (2N2646)   -   1 No.
6. Regulated Power supply 0-30 VDC (dual)   -   1 No.
7. Connecting wires
8. Bread board

Circuit diagram:
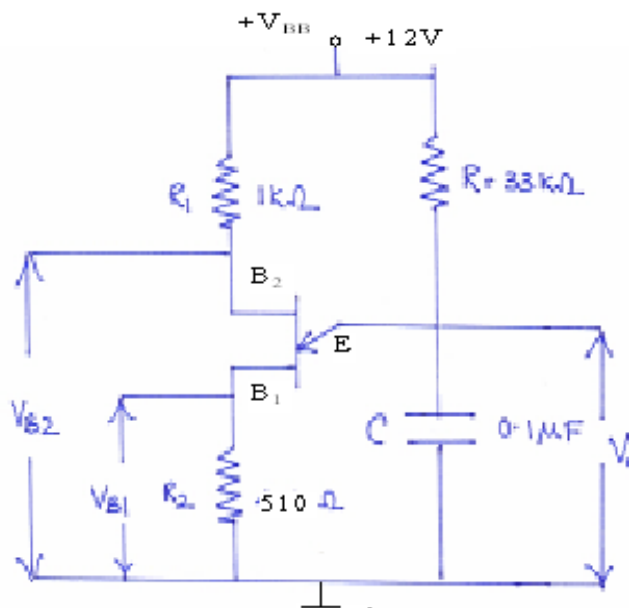
Theory:

Pin assignment of UJT:
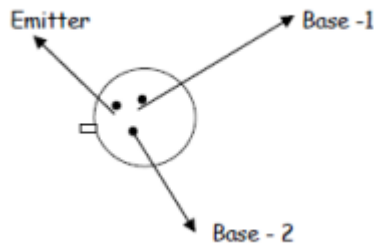
Viewing from the side of pins

The uni-junction transistor (UJT) has two doped regions with three external leads. It has one emitter and two bases. The emitter is heavily doped having many holes. The n-region is lightly doped. For this reason, the resistance between the bases is relatively high, typically $5K\Omega$ to $10 K\Omega$ when the emitter is open. This is called Inter-base Resistance R_{BB}.

Operation:

The inter-base resistance between B2 and B1 of the silicon bar is, $R_{BB}=R_{B1}+ R_{B2}$.
With emitter terminal open, if voltage V_{BB} is applied between the two bases, a voltage gradient is established along the n-type bar.
The voltage drop across R_{B1} is given by $= \eta V_{BB}$, where the intrinsic stand-off ratio
$$\eta =R_{B1}/(R_{B1} + R_{B2})$$
The typical value of η ranges from 0.56 to 0.75.

This voltage V1 reverse biases the PN-junction and emitter current is cut-off. But a small leakage current flows from B2 to emitter due to minority carriers.

The equivalent circuit of UJT is shown in figure below.

43
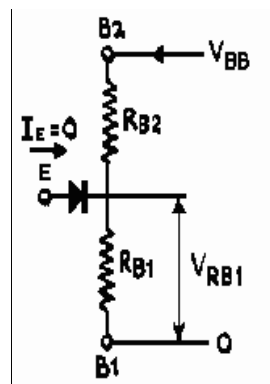
Fig.5.2 UJT equivalent circuit.

If a negative voltage is applied to the emitter, PN-junction remains reverse biased and the emitter current is cut-of. The device is now in the 'OFF' state.

If a positive voltage V_E is applied to the emitter, the PN-junction will remain reverse biased so long as V_E is less than V_i. If V_E exceeds V_i by the cut-in voltage vy, the diode becomes forward biased. Under this condition, holes are injected into n-type bar. These holes are repelled by the terminal B2 and are attracted by the terminal B1. Accumulations of holes in E to B1 region reduce the resistance in this section and hence emitter current IE is increased and is limited by V_E. The device is now in the 'ON' state.

Characteristicsof UJT:

Figure below shows the input characteristics of UJT.
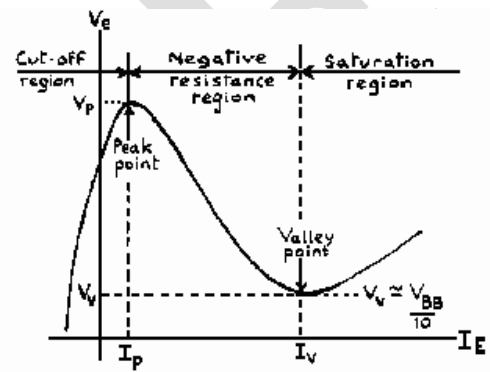
Fig.5.3 Characteristics of UJT

Here, up to the peak point, the diode is reverse biased and hence, the region to the left of the peak point is called cut-off region.

At P, the peak voltage $VP = \eta\ V_{BB} + V\gamma$, the diode starts conducting and holes are injected into n-layer. Hence, resistance decreases thereby decreasing V_E for the increase in I_E. So there is a negative resistance region from peak point P to valley point V.

After the valley point, the device is driven into saturation and behaves like a conventional forward biased PN-junction diode. The region to the right of the valley point is called saturation region.

In the valley point, the resistance changes from negative to positive. The resistance remains positive in the saturation region.

Due to the negative resistance property, a UJT can be employed in a variety of applications, viz., a saw-tooth wave generator, pulse generator, switching, and timing and phase control circuits.

Frequency of oscillations:

The time period and hence the frequency of the saw-tooth wave can be calculated as follows:
Assuming that the capacitor is initially uncharged, the voltage VC across the capacitor prior to breakdown is given by

$$V_C = V_{BB} (1 - e^{-t/R_E C_E})$$

Where $R_E C_E$ = charging time constant of resistor-capacitor circuit, and t= time from the commencement of the waveform.

The discharge of the capacitor occurs when VC is equal to the peak-point voltage VP, i.e,

$$V_P = \eta V_{BB} = V_{BB} (1 - e^{-t/R_E C_E})$$

$$\eta = 1 - e^{-t/R_E C_E}$$
$$e^{-t/R_E C_E} = 1 - \eta$$
$$t = R_E C_E \log_e(1/(1-\eta))$$
$$= 2.303 R_E C_E \log_{10}(1/(1-\eta))$$

If the discharge time of the capacitor is neglected, then t=T, the period of the wave.
Therefore, frequency of oscillations of saw-tooth wave,

$$F = 1/T = 1/(2.303 R_E C_E \log_{10}(1/(1-\eta)))$$

Procedure

1. Connect the circuit as shown in figure.
2. Apply 12V DC power supply to the circuit.
3. Observe the output waveform on the CRO at B1, B2 and V_O and Plot the graphs
4. Vary the time constant (RC) by varying capacitor (C) or potentiometer (R) and observe the variations in the output pulses on the CRO at B1, B2 and V_O.

Expected Graphs :
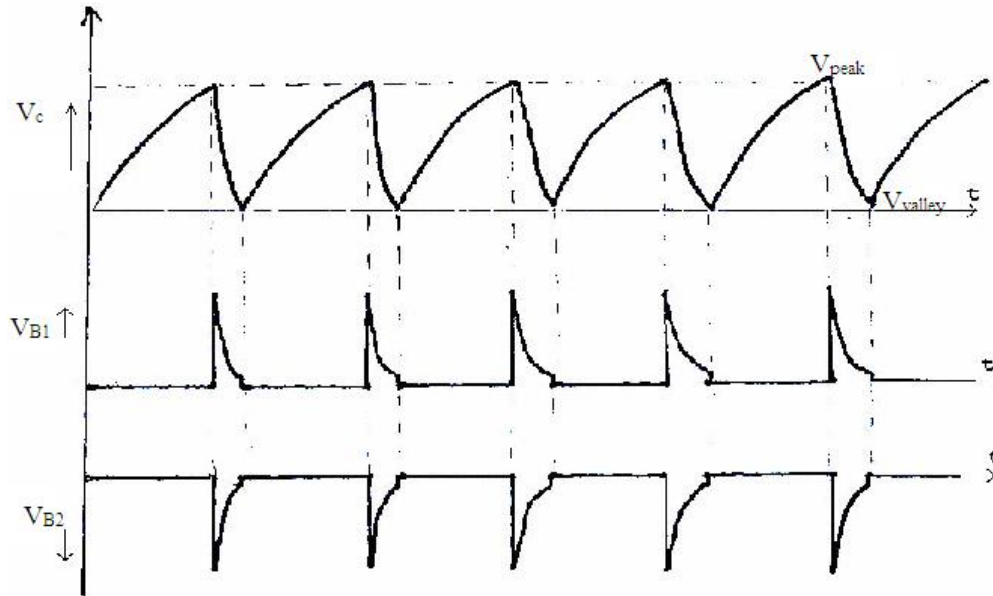
Fig.5.4 output waveforms of UJT relaxation oscillator

Inference: The operation of UJT as relaxation oscillator is studied.

Viva Questions:
1.   What is a relaxation oscillator?
2.   The most useful applications of a relaxation oscillator waveform are _, _
3.   What is meant by intrinsic stand off ratio of an UJT?
4.   Why UJT is called as negative resistance device? When the negative resistance exists in UJT characteristics.
5.   Draw the equivalent circuit of an UJT.
6.   The deviation from linearity of a relaxation oscillator is expressed in three ways. What are they?
7.   The other names of Relaxation oscillator are _, _ & _.
8.   The time during which the output increases linearly is called the __ and the time required by the sweep voltage to return to the initial value is called the __
9.   When __ of a relaxation oscillator output is zero, a saw-tooth or ramp output waveform is obtained.
10.   What are Peak point and valley point for an UJT? Write formula for Peak voltage.

Design problems
1.   Design UJT relaxation oscillator with sweep amplitude of 6V, with sweep interval of 3ms neglect flyback time and e_s=0.75.
2.   Design UJT relaxation oscillator with sweep amplitude of 10V, with sweep interval of 2ms neglect flyback time and e_s=0.8.

Outcomes: After finishing this experiment students are able to understand the operation of UJT as a relaxation oscillator.

Experiment No. 6

ASTABLE MULTIVIBRATOR

Prior to the Lab session:

1. Study the operation and working principle of Astable Multivibrator.
2. Study the procedure for conducting the experiment in the lab.

Objective:

1. To study the operation and observe the wave forms of Astable Multivibrator.
2. To Design an Astable Multivibrator to generate a square wave of 1 KHz frequency using Transistor.

Apparatus:

1.   CRO   0 to 20 MHz (Dual Channel)   -   1 No.
2.   Function Generator 1Hz to 1 MHz   -   1 No.
3.   Bread board   -   1 No.
5.   Resistor (1 KΩ, 10 KΩ)   -   2 Nos each
6.   Capacitors (0.1μF)   -   2 Nos
6.   Transistor (BC 107)   -   2 Nos
7.   Regulated D.C Power Supply 0 to 30V   (dual)   -   1 No.
8.   Connecting wires
9.   Bread board

Circuit diagram:
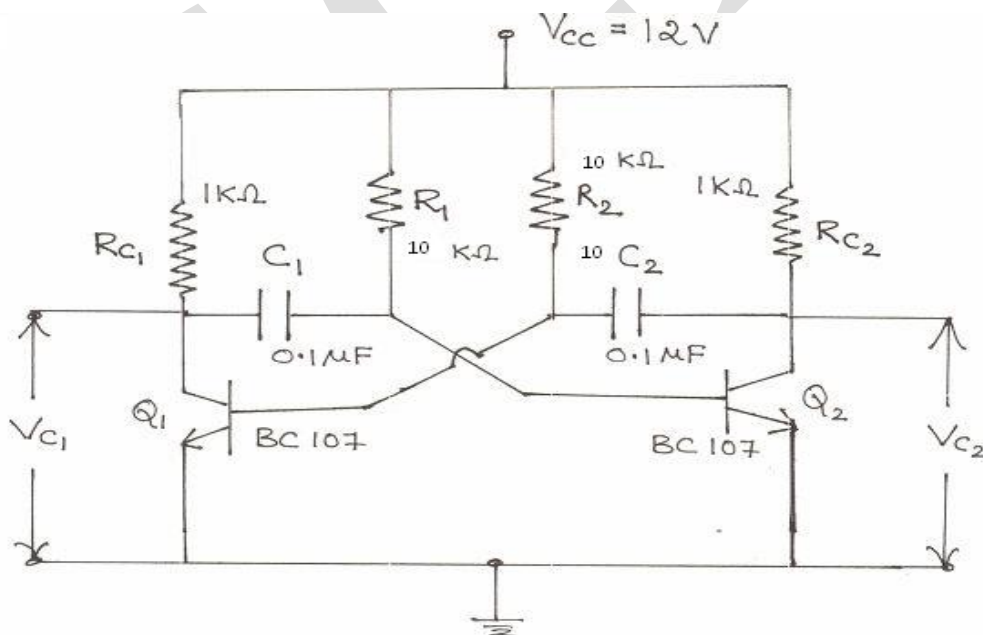
Theory:

The Astable circuit has two quasi-stable states. Without external triggering signal the Astable configuration will make successive transitions from one quasi-stable state to the other. The Astable circuit is an oscillator. It is also called as free running multivibrator and is used to generate "Square Wave". Since it does not require triggering signal, fast switching is possible.

Operation:

When the power is applied, due to some imbalance in the circuit, the transistor Q_2 conducts more than Q_1 i.e. current flowing through transistor Q_2 is more than the current flowing in transistor Q_1. The voltage V_{C2} drops. This drop is coupled by the capacitor C_1 to the base by Q_1 there by reducing its forward base-emitter voltage and causing Q_1 to conduct less. As the current through Q_1 decreases, V_{C1} rises. This rise is coupled by the capacitor C_2 to the base of Q_2. There by increasing its base- emitter forward bias. This Q_2 conducts more and more and Q_1 conducts less and less, each action reinforcing the other. Ultimately Q_2 gets saturated and becomes fully ON and Q_1 becomes OFF. During this time C_1 has been charging towards V_{CC} exponentially with a time constant $T_1 = R_1C_1$. The polarity of C_1 should be such that it should supply voltage to the base of Q_1. When C_1 gains sufficient voltage, it drives Q_1 ON. Then V_{C1} decreases and makes Q_2 OFF. V_{C2} increases and makes Q_1 fully saturated. During this time C_2 has been charging through V_{CC}, R_2, C_2 and Q_i with a time constant $T_2 = R_2C_2$. The polarity of C_2 should be such that it should supply voltage to the base of Q_2. When C_2 gains sufficient voltage, it drives Q_2 ON, and the process repeats.

Design Procedure:

The period T is given by

$$T = T_1 + T_2 = 0.69 (R_1C_1 + R_2C_2)$$

For symmetrical circuit, with $R_1 = R_2 = R$ & $C_1 = C_2 = C$

$$T = 1.38 \ RC$$

Let $V_{CC} = 12V$; $h_{fe} = 51$ (for BC107), $V_{BESat} = 0.7V$; $V_{CESat} = 0.3V$ Let $C = 0.1\mu F$ & T=1mSec.

$$T = 1.38 \ RC$$

$$10^{-3} = 1.38 \ x \ R \ X \ 0.1 \ X \ 10^{-6}$$

$$R = 7.24 \ K\Omega \ (Practically \ choose \ 10K\Omega) \ i.e \ R_1 \ and \ R_2 \ resistors.$$

Let I_{Cmax}=10mA

$$R_C = \frac{Vcc - Vcesat}{Icmax} = \frac{12 - 0.3}{0.01} = 1.17K\Omega \ (\ 1 \ K\Omega \ is \ selected \ for \ R_{c1} \ and \ R_{c2})$$

Procedure:

1. Make then connections as per the circuit diagram.
2. Observe the Base Voltage and Collector Voltages of Q1 & Q2 on CRO in DC mode and measure the frequency (f = 1/T).
3. Trace the waveforms at collector and base as each transistor with the help of dual trace CRO and plot the waveforms.
4. Verify the practical output frequency with theoretical values f = 1/T, where T = 1.38 RC

Expected Waveforms:
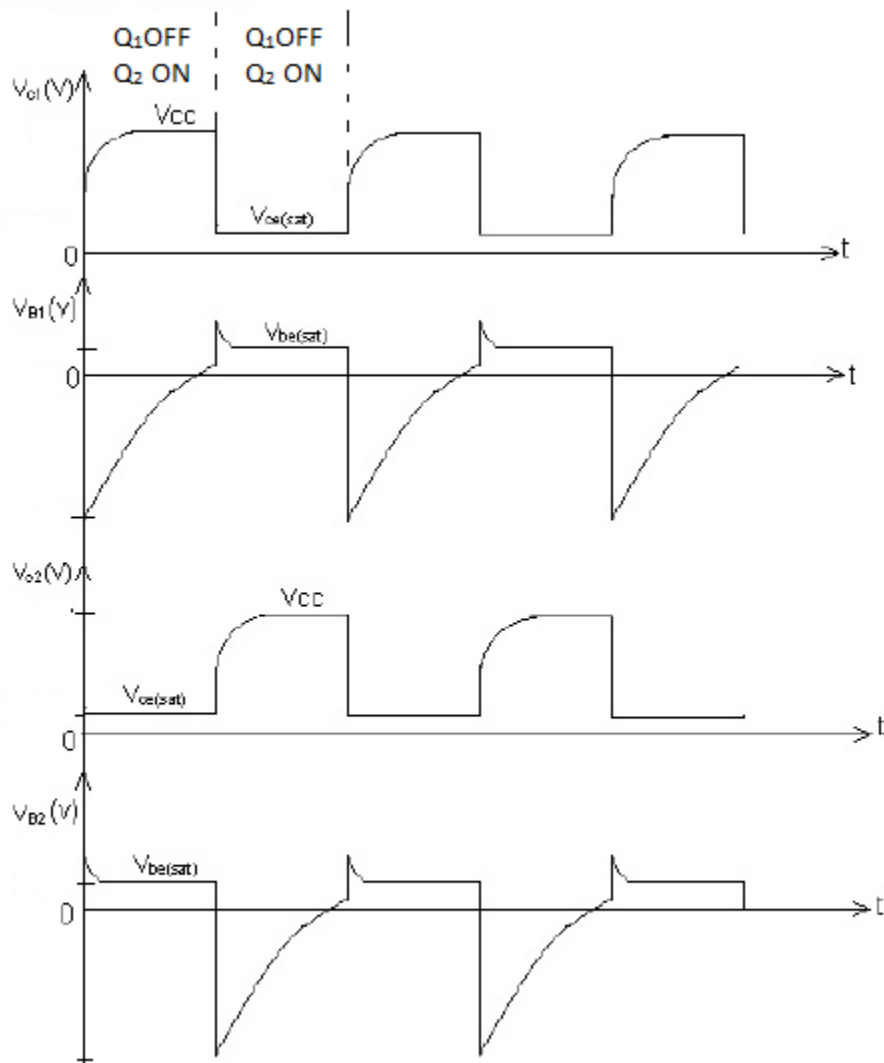
Theoretical calculations: F= 1/ T= (1/1.38RC)

R= 10K Ω C=0.1μF

Result: An Astable Multivibrator is designed; the waveforms are observed and verified the results theoretically.

Viva questions

1. What are the other names of Astable multivibrator?
2. The smaller allowable interval between two triggers is called the __ of the flip-flop.
3. Explain charging and discharging of capacitors in an Astable Multivibrator?
4. How can an Astable multivibrator be used as VCO?
5. What are symmetrical triggering and unsymmetrical triggering?
6. What are the applications of Astable Multivibrator?
7. Which multivibrator has two quasi-stable states? What is duty cycle?
8. What is the formula for frequency of oscillations?
9. An astable multivibrator is used as a ___ generator.
10. Design R and C for a frequency of 2KHz of a symmetric Astable oscillator.

  Design problems
1. Design a collector coupled astable multivibrator using 2-BC107 transistors to operate at 1.5KHz and with a duty cycle of 45% $h_{fe\ min)}$=40, V_{CC}=12V, I_C(sat)=10mA.
2. Design voltage to frequency converter using astable multivibrator.

Outcomes: After finishing this experiment students are able to design Astable Multivibrator and explain the operation of the same.

MONOSTABLE MULTIVIBRATOR

Pre-Lab:

1.   Study the operation and working principle Monostable Multivibrator.
2.   Study the procedure for conducting the experiment in the lab.

Objectives:

1. To study the operation and observe the wave forms of Monostable Multivibrator.
2. To Design a Monostable multivibrator for the pulse width of 0.3mSec.

Apparatus:

1.	CRO 0 to 20 MHz (Dual channel)	-	1No.
2.	Function generator 1Hz to 1 MHz	-	1No.
3.	Capacitors (0.033μF)	-	2 No.
4.	Capacitor(0.01 μF))	-	1 No.
5.	Resistors (1 kΩ, 10kΩ, 100KΩ, 47KΩ)	-	2, 2, 1 and 1 Nos .
6.	Transistor (BC 107)	-	2 No.
7.	Diode(IN4148)	-	1 No.
8.	Regulated Power supply 0 – 30 V(dual)	-	1 No.
9.	Connecting wires		
10.	Bread board		

Circuit diagram:

Theory:

The monostable circuit has one permanently stable and one quasi-stable state. In the monostable configuration, a triggering signal is required to induce a transition from the stable state to the quasi- stable state. The circuit remains in its quasi-stable for a time equal to RC time constant of the circuit. It returns from the quasi-stable state to its stable state without any external triggering pulse. It is also called as one-shot, a single cycle, a single step circuit or a univibrator.

Operation:

Assume initially transistor Q_2 is in saturation as it gets base bias from V_{CC} through R. coupling from Q_2 collector to Q_1 base ensures that Q1 is in cutoff. If an appropriate negative trigger pulse applied at collector of Q_1 (V_{C1}) induces a transition in Q_2, then Q2 goes to cutoff. The output at Q_2 goes high. This high output when coupled to Q_1 base, turns it ON. The Q_1 collector voltage falls by I_{C1} R_{C1} and Q2 base voltage falls by the same amount, as voltage across a capacitor 'C' cannot change instantaneously.

The moment, a negative trigger is applied at V_{C1}, Q_2 goes to cutoff and Q_1 starts conducting. There is a path for capacitor C to charge from V_{CC} through R and the conducting transistor Q_1. The polarity should be such that Q_2 base potential rises. The moment, it exceeds Q_2 base cut-in voltage, it turns ON Q_2 which due to coupling through R1 from collector of Q2 to base of Q1, turns Q1 OFF. Now we are back to the original state i.e. Q_2 is ON and Q1 is OFF. Whenever trigger the circuit into the other state, it cannot stay there permanently and it returns back after a time period decided by R and C.

Pulse width is given as T = 0.69RCsec.F

Design Procedure:

To design a monostable multivibrator for the Pulse width of 0.3 mSec.

Let I_{Cmax} = 15mA, V_{CC} = 15V, V_{BB} = 15V, R1 = 10KΩ.

$$T = 0.69RC$$

Choose C = 10nf(0.01μF)   T = 0.69 RC

$$0.3 \times 10^{-3} Sec = 0.69 \times R \times 10 \times 10^{-9}$$

$$R = 43.47\ KΩ ≈ 47KΩ$$

$$R_C = (V_{CC} - V_{CESAT}) / I_{CMAX} = (15 - 0.3) / 15 X 10^{-3}$$

$$= 1\ KΩ$$

Minimum requirement of $|V_{B1}| \leq 0.1$

For more margin, given V_{B1} = -1.185

$$V_{B1} = \frac{-V_{BB}}{R1 + R2} R_1 + \frac{-V_{CEsat}}{R1 + R2} R_2$$

Substitute the values , R_1=10kΩ   we will get R_2= 100KΩ

Procedure:

1. Make the connections as per the circuit diagram.
2. Select the triggering pulse such that the frequency is less than 1/T
3. Apply the triggering input to the circuit and to the CRO's channel and Connect the CRO channel-2 to the collector and base of the Transistor Q1&Q2.
4. Adjust the triggering pulse frequency to get stable pulse on the CRO and now measure the pulse width and verify with the theoretical value.
5. Obtain waveforms at different points like V_{B1}, V_{B2}, V_{C1} & V_{C2} and plot the graph.

Expected Waveforms:

Trigger input
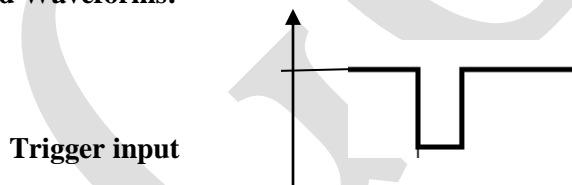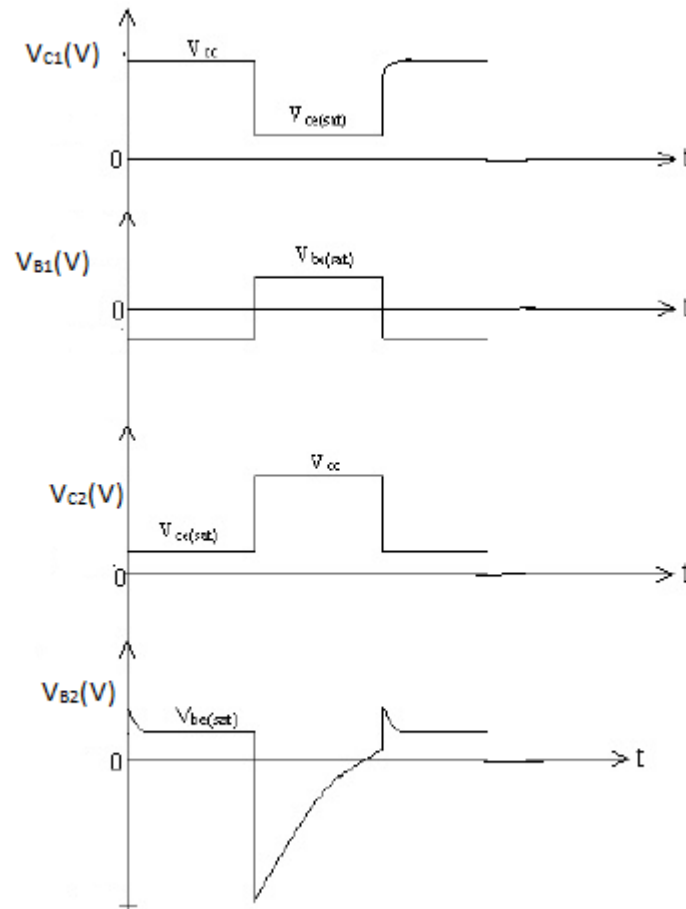
Theoretical calculations: $T_{ON} = 0.69\ RC$

$$R = 47K\Omega \ \ and \ \ C = 10nF \ or \ 0.01\mu F$$

Note: Normally Monostable Multivibrator generates single pulse output whenever a trigger is given. To observe this output storage oscilloscope is required.

Result: Monostable Multivibrator is designed; the waveforms are observed and verified the results theoretically.

Viva Questions:

1. What is a multivibrator? What is a quasi state?
2. What are applications of Monostable Multivibrator?
3. The monostable multivibrator is also called __, ___, __, ___ or ___.
4. A Monostable Multivibrator generates __ waveform.
5. Why is the time period T also called Delay time?
6. Justify, Why Monostable Multivibrator is called one-shot circuit?
7. In monostable multivibrator, the coupling elements are __.

8. What is the formula for the pulse width of a Monostable multivibrator? To get a pulse width of 2 mSec., get the values of R and C.
9. ___ triggering is used in monostable multivibrator.
10. What is monostable multivibrator and define its working states.

Design Projects

   1. Design a collector coupled monostable multivibrator using 2-BC107 transistor with 5ms quasi stable state duration V_{CC}=10V , $h_{fe(min)}$=30 $I_{C(sat)}$=5mA.
   2. Verify the output of monostable multivibrator by using different triggering methods.

Outcomes: After finishing this experiment students are able to design Monostable Multivibrator and able to explain its operation.

<div align="right">**Experiment No: 8**</div>

BISTABLE MULTIVIBRATOR

Prior to the Lab session:

1. Study the operation and working principle Bistable Multivibrator.
2. Study the procedure for conducting the experiment in the lab.

Objective

1. To Design a Bistable Multivibrator & observe its response.

Apparatus:

1.	CRO 0 to 20 MHz (Dual channel)	-	1No.
2.	Function generator 1Hz to 1 MHz	-	1No.
3.	Capacitor (0.001µF, 0.33 µF)	-	2 Nos each.
4.	Resistors (1 kΩ, 10kΩ, 100KΩ)	-	2 Nos each.
5.	Transistor (BC 107)	-	2 No. each.
6.	Diode (IN4007)	-	4 No. each.
7.	Regulated Power supply 0 – 30 V(dual)	-	1 No.
8.	Connecting wires		
9.	Bread board		

Circuit diagram:
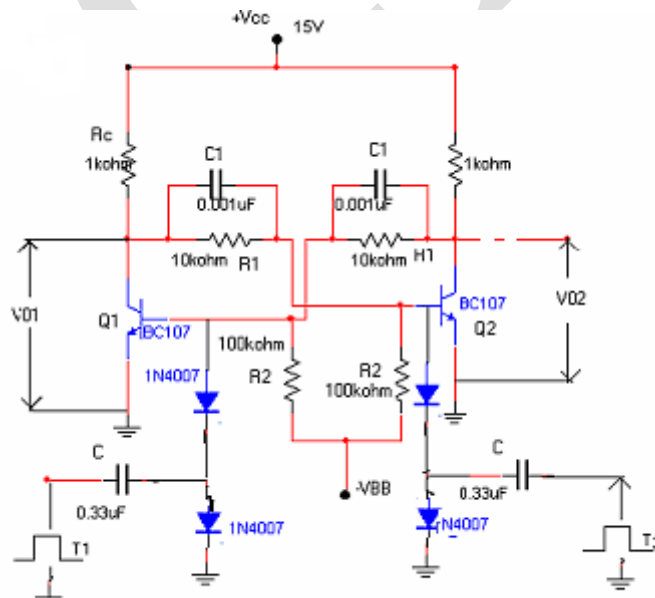
Theory:

A Bistable circuit is one which can exist indefinitely in either of two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. The Bistable circuit is also called as Bistable multivibrator, Eccles Jordon circuit, Trigger circuit, Scale-of-2 toggle circuit, Flip-Flop & Binary.

A Bistable multivibratior is used in a many digital operations such as counting and the storing of binary information. It is also used in the generation and processing of pulse-type waveform. They can be used to control digital circuits and as frequency dividers.

There are two outputs available which are complements of one another. i.e. when one output is high the other is low and vice versa .

Operation:

When V_{CC} is applied, one transistor will start conducting slightly more than that of the other, because of some differences in the characteristics of a transistor. Let Q_2 be ON and Q1 be OFF. When Q2 is ON, The potential at the collector of Q_2 decreases, which in turn will decrease the potential at the base of Q_1 due to potential divider action of R_1 and R_2. The potential at the collector of Q_1 increases which in turn further increases the base to emitter voltage at the base of Q_2. The voltage at the collector of Q_2 further decreases, which in turn further reduces the voltage at the base of Q_1. This action will continue till Q_2 becomes fully saturated and Q_1 becomes fully cutoff.

Thus the stable state of binary is such that one device remains in cut-off and other device remains at saturation. It will be in that state until the triggering pulse is applied to it. It has two stable states. For every transition of states triggering is required. At a time only one device will be conducting.

NEED OF COMMUTATING CAPACITORS (SPEED UP CAPACITORS):

It is desired that the transition should take place as soon as the trigger pulse is applied but such is not the case.

When transistor is in active region it stores charge in its base and when it is in the saturation region it stores even more charge. Hence transistor cannot come out of saturation to cut- off. Until all such charges are removed. The interval during which conduction transfer one transistor to other is called as the transition

Design Procedure:

$$R_C = \frac{V_{CC} - V_{CESAT}}{I_{Cmax}} = \frac{15 - 0.3}{15 \times 10^{-3}} = 1 K\Omega$$

$$V_{B1} = \frac{-V_{BB}}{R1 + R2} R_1 + \frac{-V_{CEsat}}{R1 + R2} R_2$$

$-1.2 = (-15R_1+0.2R_2) /(R_1+R_2)$; given $R_1=10K\Omega$

$R_2= 100K\Omega$

$F_{max}= (R_1+R_2)/2C R_1 R_2$ $R_1=10K\Omega$, $R_2 = 100K\Omega$ and $C= 0.1\mu F$

$= (10+100)X10^3/(2X0.3X10^{-6}X10X100X10^6) = 55KHz$

Procedure:

1. Make the connections as per the circuit diagram.
2. Apply trigger pulse of 1 KHz 5v (p-p) from function generator.
3. Obtain waveforms at different points such as V_{B1}, V_{B2}, V_{C1} & V_{C2}.
4. Trace the waveform at collector and base of each transistor with the help of dual trace CRO. Note the Time relation of waveforms.

Expected Waveforms:
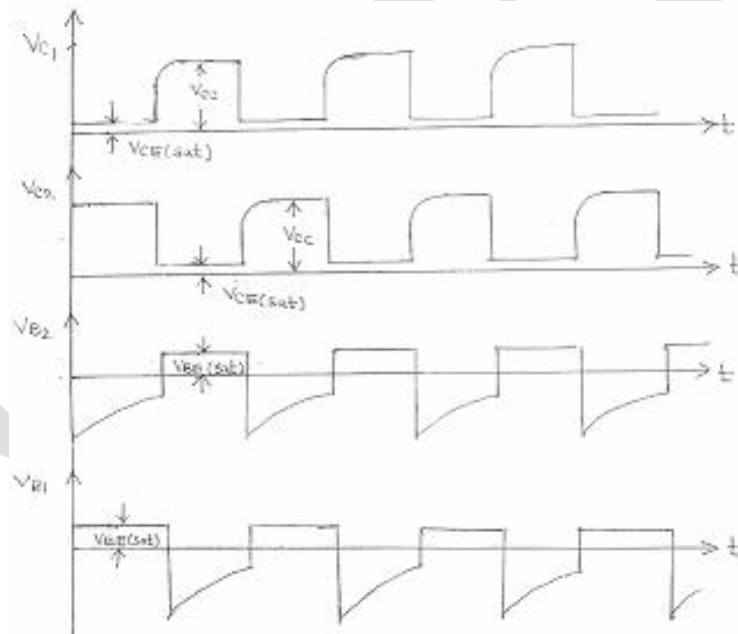
Inference: Bistable Multivibrator is designed; and the waveforms are observed

Viva Questions:

   1. What are the other names of Bistable Multivibrator?
   2. What are the applications of a Bitable Multivibrator?
   3. Describe the operation of commutating capacitors?
   4. Commutating capacitors are also called as __ or __ .
   5. What is the meaning of a stable state in a multi-vibrator?
   6. Mention the names of different kinds of triggering used in the circuit shown?
   7. What are the disadvantages of direct coupled Binary?
   8. The diodes used in a bistable multivibrator to maintain a constant output swing are called __ diodes.
   9. The interval during which conduction transfers from one transistor to another is called the __.

10. What are the coupling elements of a Bi-stable Multivibrator?

Design Projects

1. Design a fixed bias binary employing two n-p-n silicon transistor to operate max frequency of 16KHz, $V_{CC}=V_{BB}=10V$, $I_{C(sat)}=5mA$, $h_{fe(min)}=30$.

2. Design and verify the bistable multivibrator by using different triggering methods.

Outcomes: After finishing this experiment students are able to design Bistable Multivibrator and able to explain its operation.

Experiment : 9

ADDITIONAL EXPERIMENT

SCHMITT TRIGGER

Pre-Lab:

1. Study the operation and working principle of Schmitt Trigger.
2. Study the procedure for conducting the experiment in the lab.

Objectives:

1. To design the circuit of Schmitt trigger with UTP=2.2V and LTP=1V.
2. To obtain square wave from sine wave.
3. To obtain UTP and LTP values practically

Apparatus:

1.	CRO 0-20 MHz (Dual channel)	-	1No.
2.	Function generator 0- 1MHz	-	1No.
3.	Capacitor (0.1µF)	-	1 No.
4.	Resistors (1kΩ, 2.2KΩ, 330Ω)	-	1 No. each
5.	Resistor (1.2 KΩ)	-	3 No.
6.	Transistor (BC 107)	-	2 No.
7.	Regulated Power supply 0-30 V (dual)	-	1 No.
8.	Connecting wires		
9.	Bread board		

Circuit diagram:
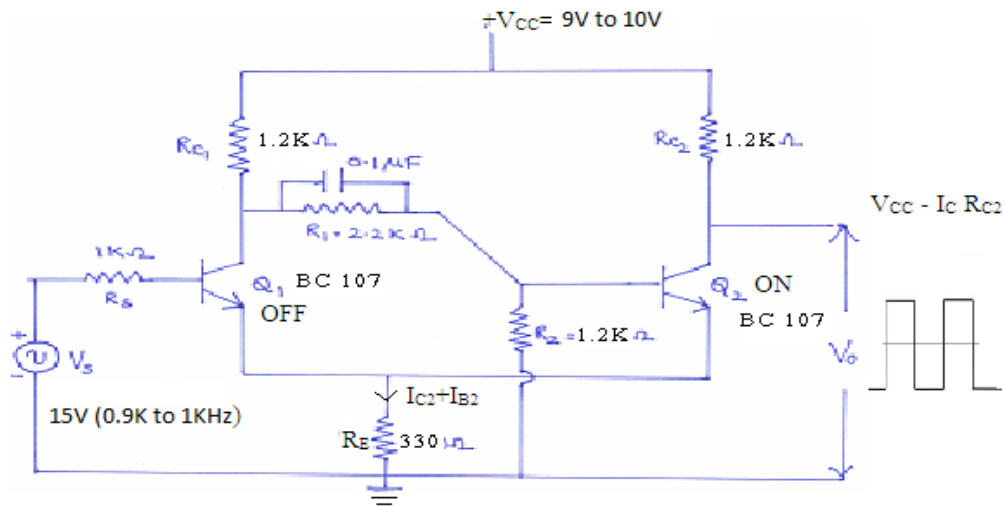
Theory:

In digital circuits fast waveforms are required i.e, the circuit remain in the active region for a very short time (of the order of nano seconds) to eliminate the effects of noise or undesired parasitic oscillations causing malfunctions of the circuit. Also if the rise time of the input waveform is long, it requires a large coupling capacitor. Therefore circuits which can convert a slow changing waveform (long rise time) in to a fast changing waveform (small rise time) are required. The circuit which performs this operation is known as "Schmitt Trigger".

In Schmitt trigger circuit, the output is in one of the two levels namely low or high. When the input voltage is raising above the UTP (upper threshold point) i.e. V1, the output changes to high level. Similarly when a falling output voltage passes through a voltage V_2 known as lower threshold point (LTP), the output changes to low. The level of the output changes V_1 is always greater than V_2. The differences of these two voltages is known as "**Hysteresis**".

Design Procedure:

The voltage required to drive the transistor Q1 from CFF to CN is called upper trigger point.

$\quad$ UTP = V1 = V^1 — 0.1

$\quad$ Where V^1 = V = ($V_{CC}R_2$)/ $(R_1+R_2+R_{C1})$

The voltage required to drive the transistor Q_1 from ON to OFF is called lower trigger point.

$\quad$ LTP = V_2= $V_{BE(active)}$+ $(V^1-V_{\gamma2})$ .R_e/$(aR_c{}^{th}+R_e)$

$\quad$ Where $R_c{}^{th}$ =$(R_{C1}(R_1+R_2))$/$(R_1+R_2+R_{C1})$ $\qquad\qquad$ a =R_2/(R_1+R_2)

Choose BC107 transistor with h_{fe}= 200

$\quad$ Let V_{cc}=12V, R_1=2.2KΩ , R_2=1.2KΩ

$\quad$ Set UTP = V^1 — 0.1 $\longrightarrow$ $\quad$ 2.2= V^1 — 0.1 $\longrightarrow$ $\qquad$ V_1= 2.3V

$\quad$ But V^1= (12X15)/(2.2+1.5+R_{C1}) $\longrightarrow$ $\qquad$ RC1=4.12KΩ= 4KΩ

$\quad$ $R_c{}^{th}$ = (4X 10^3(2.2+1.5))/(2.1+1.2+4.4K) = 1.97KΩ

$\quad$ a= 0.3529

$\quad$ LTP =V_2= $V_{BE(active)}$+ $(V^1-V_{\gamma2})$ .R_e/$(aR_c{}^{th}+R_e)$

$\qquad$ = 0.7+(2.3-0.6).330/(0.35X1.97K+330)

$\qquad$ = 1.21V

$\quad$ V_E=V_1-V_{BE}= 2.3-0.7 = 1.6V

$\quad$ I_{B2}= V_E/R_E(1+h_{fe}) = 1.6/330(1+200) = 0.0030A

$\quad$ I_{C2} = $h_{fe}I_{B2}$ =0.6V

$\quad$ When V_{in} < V_2, output =1V

$(V_C\text{-output})/I_{C2} = R_{C2}$ ➤ $(12-1)/0.6 = R_{C2} = 18.33\Omega$

Procedure:

1. Connect the circuit diagram as shown in fig 4.1.
2. Apply a sine wave input of 15 Vp-p amplitude and 1 KHz frequency to the circuit
3. Observe the output voltage on CRO.
4. Obtain the output voltage at which LOW to HIGH transition occurs and measure the corresponding input voltage. This input voltage is called UTP (Upper threshold point)
5. Now, Obtain the output voltage at which HIGH to LOW transition occurs and measure the corresponding input voltage. This input voltage is called LTP (Lower threshold point).
6. Compare these practical values with theoretical values.
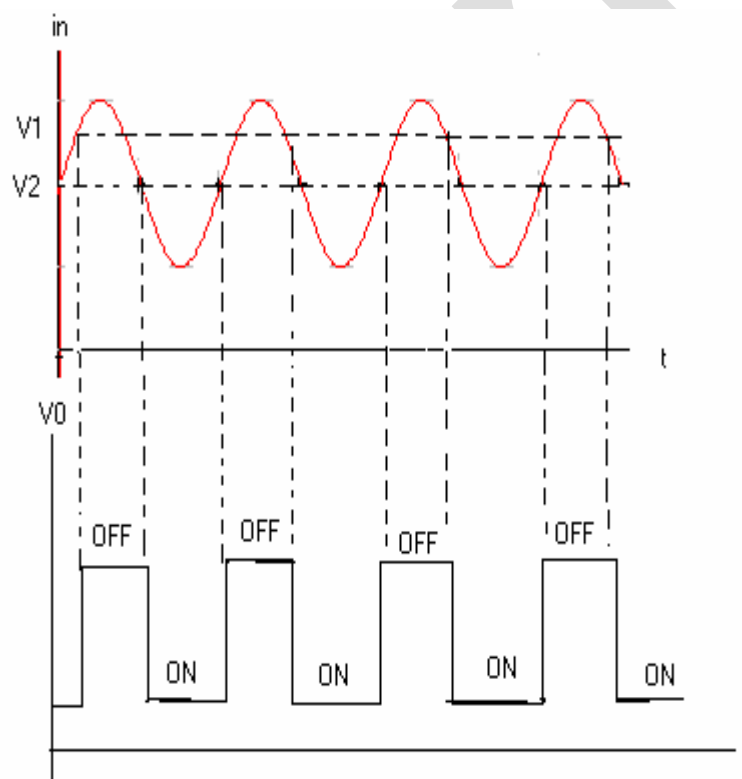
Expected Waveforms:

Fig.4.2 input & output waveforms of Schmitt Trigger

Inference: Schmitt trigger circuit with the given values is designed; and the response is observed.

Viva Questions:

1. What is Schmitt Trigger?
2. What are the applications of Schmitt Trigger?
3. Define hysteresis action?
4. Why Schmitt Trigger is called a squaring circuit?
5. Define UTP? Write its expression.
6. Define LTP? Write its expression.
7. What is the difference between a Binary and Schmitt Trigger?
8. How noise can be eliminated on a given signal using Schmitt Trigger?
9. Explain how a Schmitt Trigger converts a sine wave to a square wave?
10. A Schmitt trigger exhibits hysteresis when loop gain is ___.

Design Projects
1. Design Schmitt trigger circuit to get UTP=5V and LTP=7V for V_{CC}=15V.

Outcomes: After finishing this experiment students are able to Design Schmitt trigger circuit using transistor and they are able to find UTP and LTP.

BOOT STRAP SWEEP CIRCUIT

Pre-Lab:

1. Study the operation and working principle of Boot-strap Sweep Circuit.
2. Study the procedure for conducting the experiment in the lab.

Objectives:

1. To design a Boot-strap Sweep Circuit.
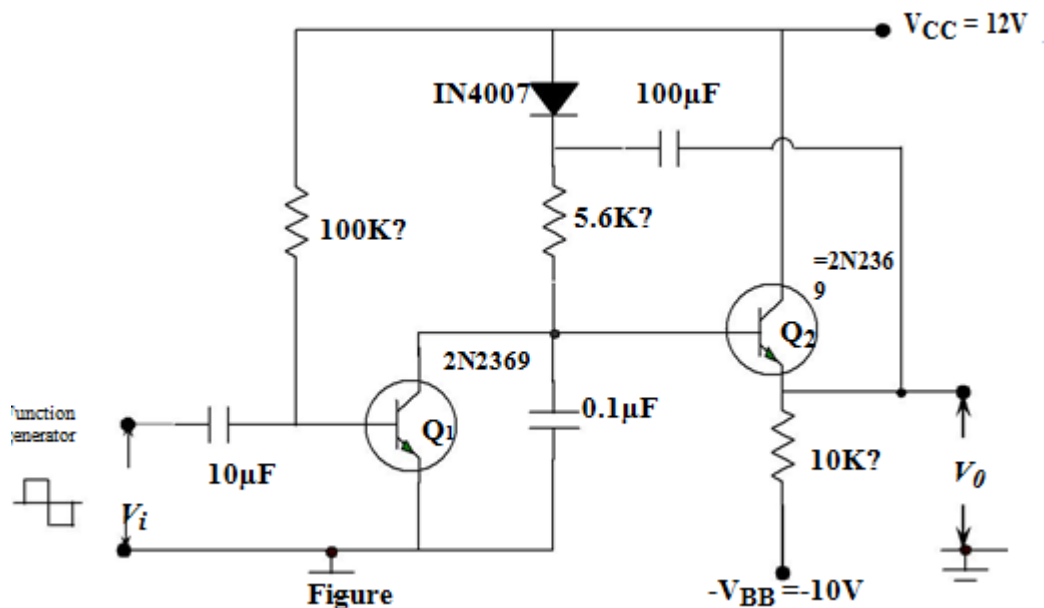2. To obtain a sweep wave form.

Components Required:

1. Resistors – 100kΩ , 5.6kΩ , 10 KΩ   - 1 each
2. Capacitors – 0.1 μ F, 10 μ F, 100μ F - 1 each
3. IN4007 Diode – 1 No.
4. 2N2369 Transistors – 2 Nos.
5. Bread Board

Apparatus Required:

a. Power supply (0V-30V)
b. CRO(1Hz-20MHz)
c. Signal generator (1Hz-1MHZ)
d. Connecting Wires.

CIRCUIT DIAGRAM

Figure

THEORY:

The input to Q1 is the gating waveform. Before the application of the gating waveform, at t = 0, transistor Q1 is in saturation. The voltage across the capacitor C and at the base of Q2 is $V_{CE(sat)}$. To ensure Q1 to be in saturation for t = 0, it is necessary that its current be at least equal to I_{CE} / h_{FE} so that $R_b < h_{fe}R$.

With the application of the gating waveform at t = 0, Q1 is driven OFF. The current I_{C1} now flow into C and assuming units gain in the emitter follower V_0 . When the sweep starts, the diode is reverse biased, as already explained above, the current through R is supplied by C1. The current V_{CC} / R through C and R now flows from base to emitter of Q2.if the output V_0 reaches the voltage VCC in a time TS / Tg, then from above we have T_S = RC.

PROCEDURE:

- ➢ Connect the circuit as shown in figure.
- ➢ Apply the square wave or rectangular wave form at the input terminals.
- ➢ Connect the CRO at output terminals now plug the power card into line switch on and observe the power indication.
- ➢ As mentioned in circuit practical calculation. Observe and record the output waveforms from CRO and compare with theoretical values.

EXPECTED WAVEFORMS :
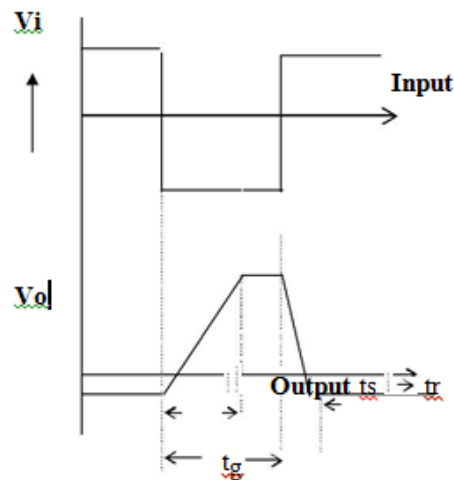
Conclusion:

Conclusions can be made on sweep time Ts and retrace time T_R and sweep voltage Vs of the sweep waveform theoretically and practically and also made on if the output waveform of the Bootstrap are identical with the theoretical wave forms or not.

VIVA QUESTIONS:

1. Define a Voltage time base generator, a current time base generator and a linear time base generator.
2. What is the relation between the slope error, displacement error and transmission error?
3. What are the various methods of generating time base wave-form?

4. Which amplifier is used in Boot-strap time base generator?
5. Which type of sweep does a bootstrap time-base generator produce?
6. What is the gain of the amplifier used in Bootstrap time base generator?
7. What is retrace time? Write the formula for the same for Bootstrap time base generator.
8. What is the formula for sweep amplitude in Bootstrap time base generator?
9. To have less flatness time of sweep signal, then the gate signal time has to be __.
10. A Bootstrap sweep circuit employs __ type of feedback.
   <u>Design problem:</u>
   1. Design Boot-strap Sweep Circuit with sweep amplitude of 8V, with sweep interval of 1ms neglect flyback time and e_s=0.25.
   2. Design Boot-strap Sweep Circuit with sweep amplitude of 15V, with sweep interval of 2ms neglect flyback time and e_s=0.1.

Outcomes: After finishing this experiment students are able to Design Boot-strap sweep circuit and able to generate a sweep voltage waveform.

Design Experiment

GENERATION OF DIFFERENT TYPES OF WAVEFORMS FROM BASIC SINUSOIDAL
WAVEFORM